Application Notes: AN_SY7060

0.7V Minimum Input and 5.25V Maximum Output Synchronous Boost Converter

General Description

SY7060 is a high efficiency, low input voltage, step-up synchronous boost converter designed for single-cell or dual-cell alkaline, NiMH, or NiCd battery-powered applications. It can receive an input voltage as low as 0.7V. It adopts NMOS for the main switch and PMOS for the synchronous switch.

Ordering Information

SY7060 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY7060AHC	SOT-363(SC70)	----

Features

- Typical 0.7V minimum input voltage
- Adjustable output voltage from 1.8V to 5.25V
- 18uA quiescent current
- Pass-through function during shutdown
- Output over-voltage protection
- Low $R_{DS(ON)}$ (main switch/synchronous switch) at 3.3V output: 0.45/0.80ohm
- Typical 400mA peak current limit
- Typical fixed 750nS off time
- Maximum output current
  ---50mA@0.9VIN and 3.3V_{OUT}
  ---100mA@1.8VIN and 3.3V_{OUT}
- Compact SOT-363(SC70)

Applications

- Battery powered applications
- Consumer and portable medical products
- Personal care products
- Smart Phones

Typical Applications

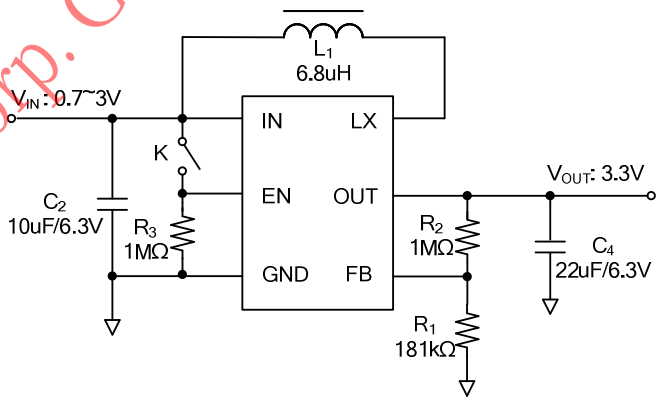
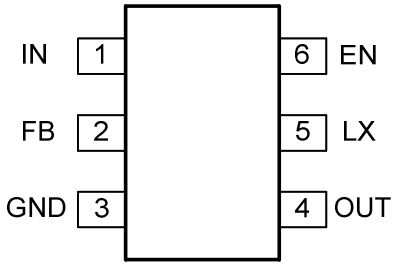


Figure 1. Schematic Diagram

Pinout (top view)



(SOT-363)

Top mark: **GY*xyz*** (Device code: GY, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	1	Input pin. Decouple this pin to GND pin with 4.7uF ceramic cap.
FB	2	Feedback pin. Connect a resistor R1 between OUT and FB, and a resistor R2 between FB and GND to program the output voltage. V_{OUT}=0.505V*(R2/R1+1)
GND	3	Ground pin.
OUT	4	Output pin. Decouple this pin to GND pin with two 10uF ceramic caps.
LX	5	Inductor node. Connect an inductor between IN pin and LX pin.
EN	6	Enable pin. Pull it high to turn on. Do not float.

Absolute Maximum Ratings (Note 1)

All Pins to GND ---------- 5.5V
Power Dissipation, P_D @ T_A = 25°C SOT-363 ---------- 0.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 161°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN,OUT ---------- 0.7V to 5.0V
EN ---------- 0V to V_{OUT}+0.3V
All other pins ---------- 0-5.0V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =1.2V, V_{OUT}=3.3V, I_{OUT}=10mA, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		0.7		5.0	V
Minimum V_{IN} at start-up		V_{START}			0.75		V
Output Voltage Range		V_{OUT}		1.8		5.25	V
Quiescent Current	V_{IN}	IQ	Io=0mA,V_{EN}=V_{IN}=1.2V, V_{OUT}=3.3V		0.5	0.9	µA
	V_{OUT}				18		
Shut Down Current		I_{SHDN}	V_{EN}=0V, V_{IN}=1.2V, V_{OUT}>V_{IN}			1	µA
EN Rising Threshold		V_{ENH}		0.7			V
EN Falling Threshold		V_{ENL}				0.3	V
Low Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT}=3.3V		0.45		Ω
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT}=3.3V		0.80		Ω
Main FET Current Limit		I_{LIM1}			400		mA
Reference Voltage		V_{REF}		0.490	0.505	0.520	V
Synchronous FET On Time		T_{OFF}			750		nS
Thermal Shutdown Temperature		T_{SD}			150		℃
Thermal Shutdown Hysteresis		T_{HYS}			20		℃
Output Over Voltage Protection		V_{OVP}			6		V
Under Voltage Lockout Threshold For Turn Off		V_{UVLO}			0.65		V

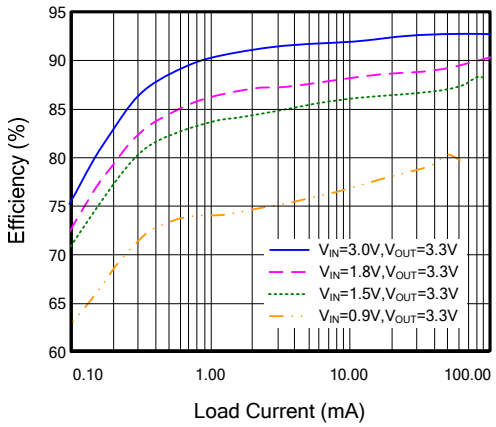
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

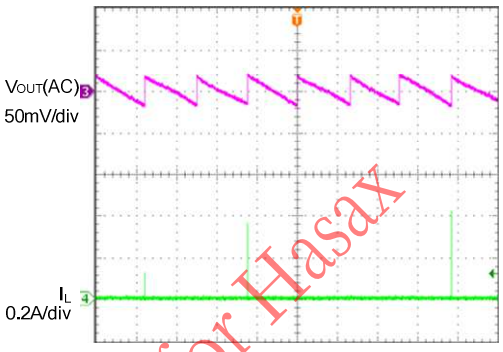
Typical Performance Characteristics

Efficiency vs. Load Current



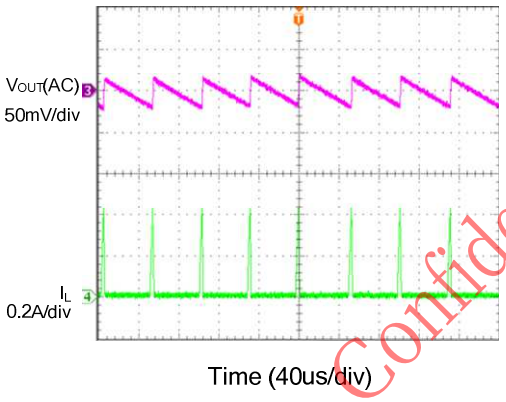
Output Ripple

(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=0)



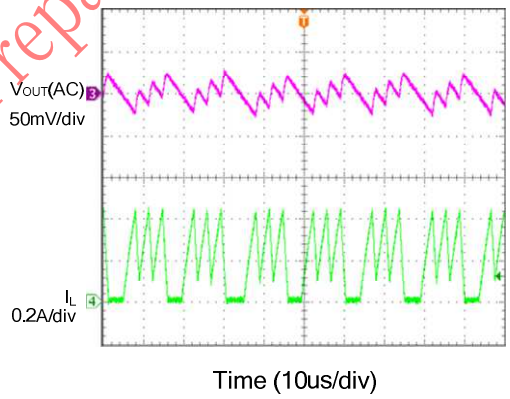
Output Ripple

(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=5mA)



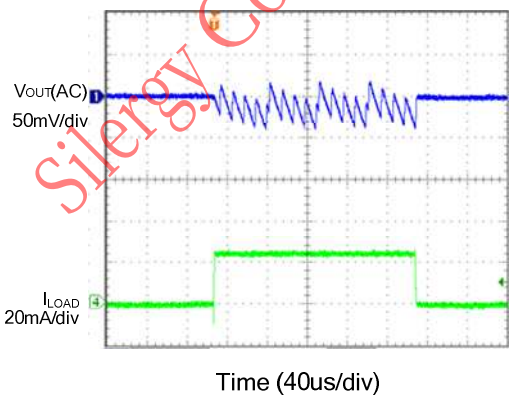
Output Ripple

(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=50mA)



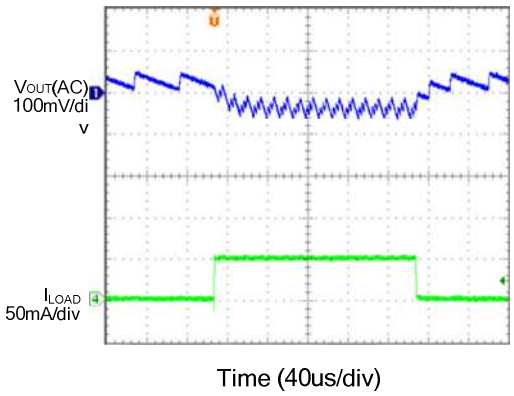
Load Transient

(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=0~25mA)



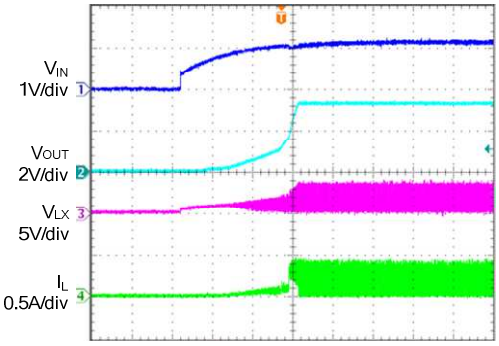
Load Transient

(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=5~50mA)



Startup from V_{IN}

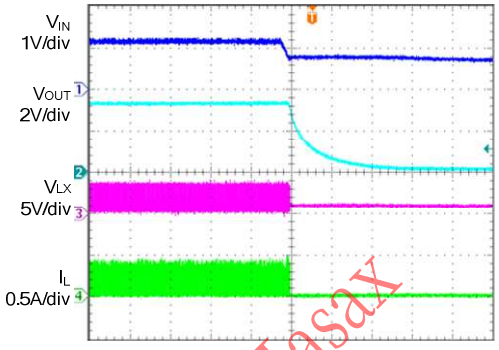
(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=50mA)



Time (2ms/div)

Shutdown from V_{IN}

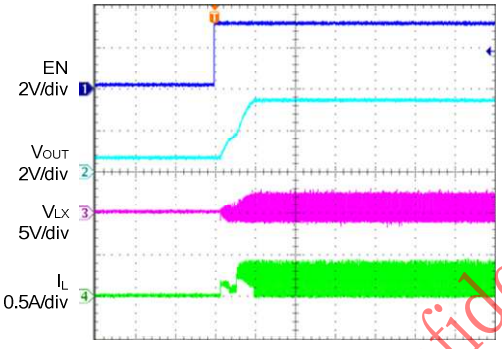
(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=50mA)



Time (2ms/div)

Startup from Enable

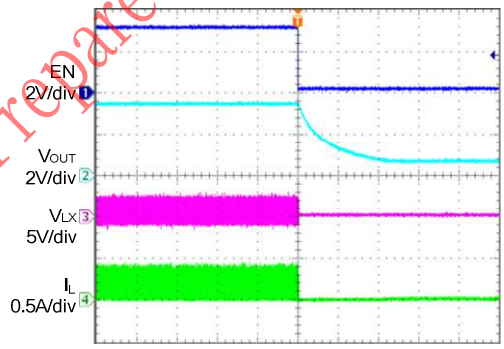
(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=50mA)



Time (1ms/div)

Shutdown from Enable

(V_{IN}=1.2V, V_{OUT}=3.3V, I_O=50mA)



Time (1ms/div)

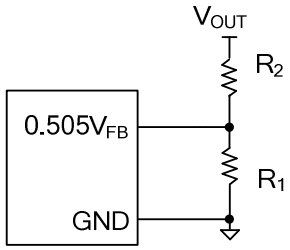
Applications Information

SY7060 is a high efficiency, low input voltage, step-up synchronous boost converter designed for single-cell or dual-cell alkaline, NiMH, or NiCd battery-powered applications. It adopts NMOS for the main switch and PMOS for the synchronous switch.

Feedback resistor dividers R1 and R2:

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. If V_{OUT} is 3.3V, R2=1Meg is chosen, using following equation, then R1 can be calculated to be 181k:

$$R_1 = \frac{0.505V}{V_{OUT} - 0.505V} \times R_2$$



Input capacitor CIN:

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 10uF low ESR ceramic capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit.

Output capacitor COUT:

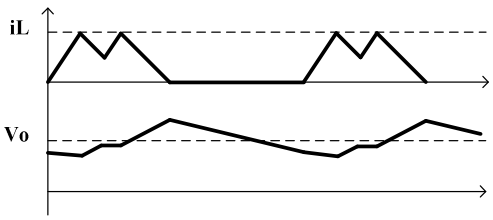
The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than 10uF capacitance.

Inductor L:

SY7060 controls output voltage directly through FB pin. And the typical peak current limit is about 400mA. If inductor current reaches the peak current limit preset value, IC will turn off the low side FET and turn on the high side FET. After the fixed off time delay, IC will turn off high side FET and turn on low side FET again. If the FB pin voltage reaches the reference voltage, IC will go into sleep mode for the low quiescent current purpose design.

If the inductor is designed large, IC can afford more output current. But the output ripple will be large. So we need to optimize the inductor design for the different cell battery input applications.

For the detailed application schematic, please refer to our BOM list proposal solutions.



Recommended PCB Layout:

For the best efficiency and minimum noise problems, we should place the following components close to the IC: CIN, COUT， L, R1 and R2.

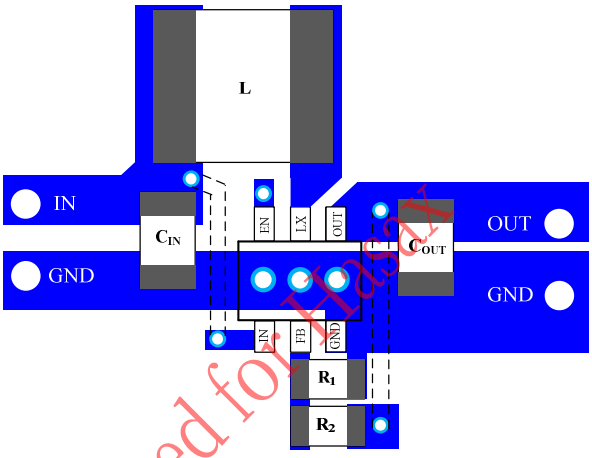
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) COUT must be close to Pins OUT and GND. The loop area formed by COUT and GND must be minimized.

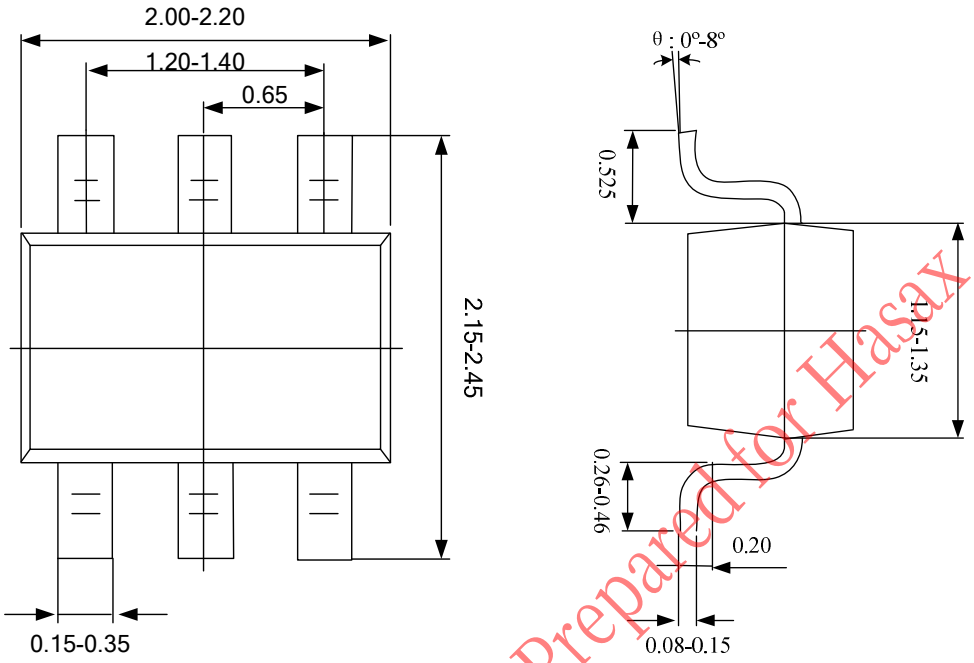
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) Feedback resistor R1, R2, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

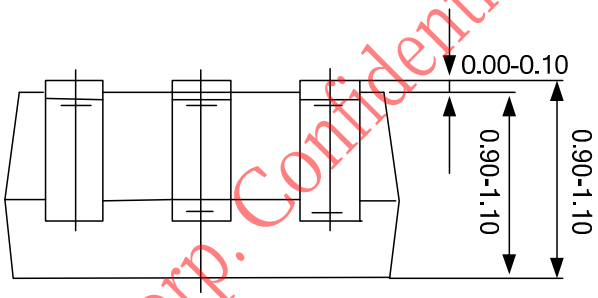
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.



SOT-363(SC70) Package outline



Recommended Pad Layout



Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

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