Application Note: AN_SY7219

High Current Step Up Regulator

General Description

SY7219 is a high efficiency, current-mode control Boost DC to DC regulator with an integrated 65mΩ $R_{DS(ON)}$ N-channel MOSFET. The OFF time and the peak current limit can be programmed for more applications.

Features

- Internal 9A switch
- Low $R_{DS(ON)}$ for internal switch: 65mΩ
- Programmable peak current limit
- Programmable constant OFF time
- Maximum voltage rating of internal switch 36V
- Internal softstart limiting the inrush current
- RoHS Compliant and Halogen Free
- Compact package: DFN3×3-10

Ordering Information

SY7219 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7219DBC	DFN3×3-10	----

Applications

- Industry control system
- Battery power system

Typical Applications

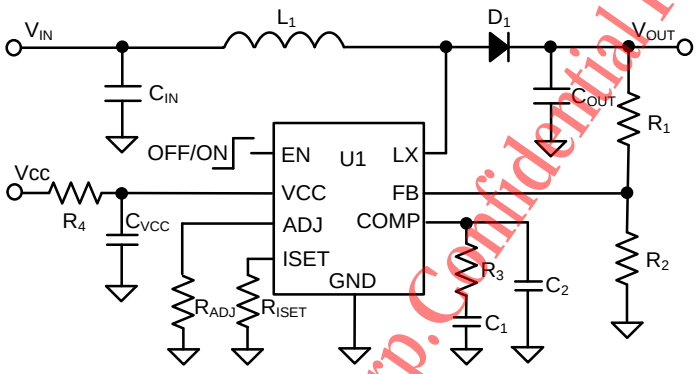


Figure 1. Schematic Diagram

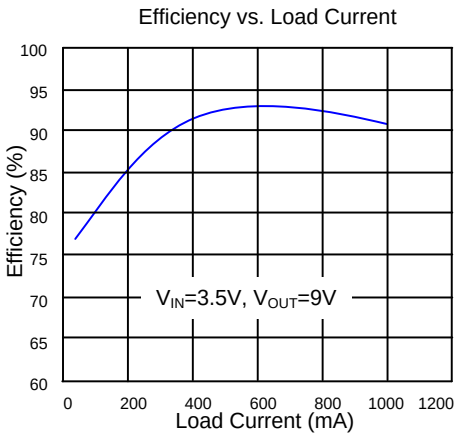
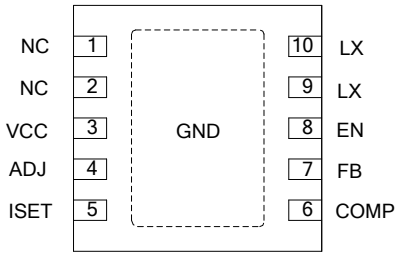


Figure 2. Efficiency vs. Load Current

Pinout (top view)

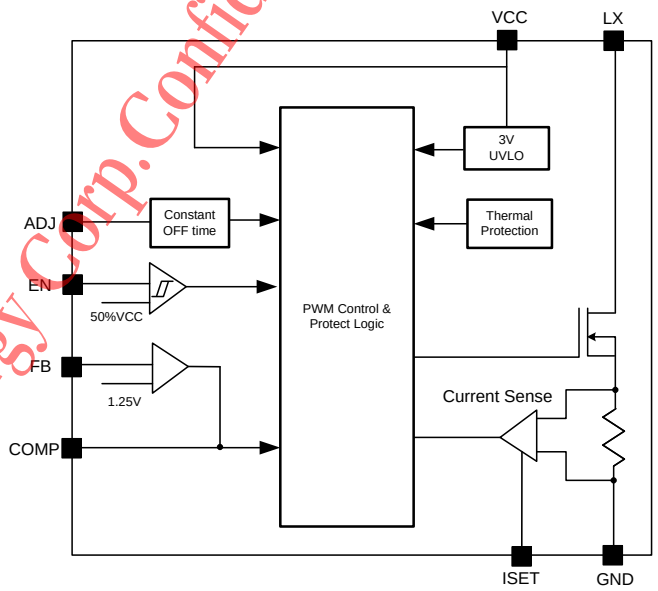


(DFN3×3-10)

Top Mark: GV*xyz* (Device code:GV, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
VCC	3	Power supply pin.
ADJ	4	Connect a resistor to ground to program the turn off time.
ISET	5	Connect a resistor to ground to program the current limit point of the internal MOSFET.
COMP	6	Compensation pin. Connect RC network between this pin and ground to program the best transient response.
FB	7	Output Feedback Pin. The reference voltage is 1.25V. If the voltage on FB pin is higher than the reference voltage by 5%, the OVP is triggered.
EN	8	Enable control pin. Connect this pin to VCC by a 1kΩ resistor recommended.
LX	9,10	Switching node. Connect this pin to switching node of the inductor.
GND	Exposed pad	Ground pin

Block Diagram



Absolute Maximum Ratings (Note 1)

LX ---- 36V
All other pins ---- 5.5V
Power Dissipation, P_D @ T_A = 25℃ DFN3X3-10 ---- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---- 38℃/W
θ_{JC} ---- 8℃/W
Junction Temperature Range ---- 125℃
Lead Temperature (Soldering, 10 sec.) ---- 260℃
Storage Temperature Range ---- -65℃ to 150℃
Dynamic LX voltage in 50ns duration ---- 39V to GND-4V

Recommended Operating Conditions (Note 3)

LX----30V
EN, VCC----5.5V
All other pins ----3V
Junction Temperature Range ---- -40℃ to 125℃
Ambient Temperature Range ---- -40℃ to 85℃

Electrical Characteristics

(V_{CC} = 5.0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC Input Voltage Range	V_{CC}		3		5.5	V
VCC Rising UVLO Threshold	$V_{UVLO,UP}$				3	V
VCC UVLO Hysteresis	$V_{UVLO,HYS}$			0.4		V
Quiescent Current	I_Q	V_{FB}=1.3V		380		μA
Shut Down Current	Is	V_{CC}=5V, V_{EN}=0V		1		μA
NFET $R_{DS(ON)}$	$R_{DS(ON)}$			65		mΩ
Maximum Peak Current limited	I_{SM}	R_{ISET}=75kΩ	8	9		A
OFF Time	T_{OFF}	R_{ADJ}=200kΩ	1.75	2.0	3.25	μs
EN Rising Threshold	V_{ENH}		2.7			V
EN Falling Threshold	V_{ENL}				0.8	V
Minimum ON Time	$T_{ON,MIN}$			100		ns
Feedback Voltage	V_{FB}		1.225	1.25	1.275	V
FB Input Current	I_{FB}	V_{FB}=3V	-50		50	nA
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Recovery Hysteresis	T_{HYS}			15		℃

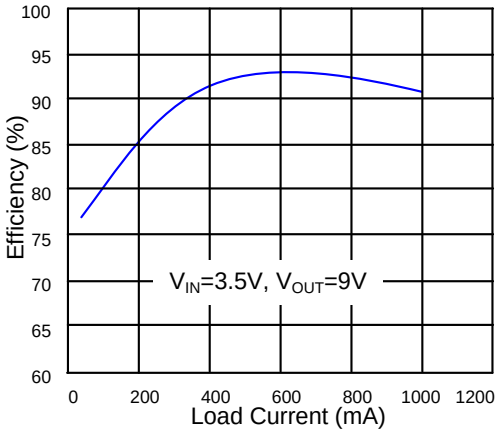
Note 1: Stresses listed beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

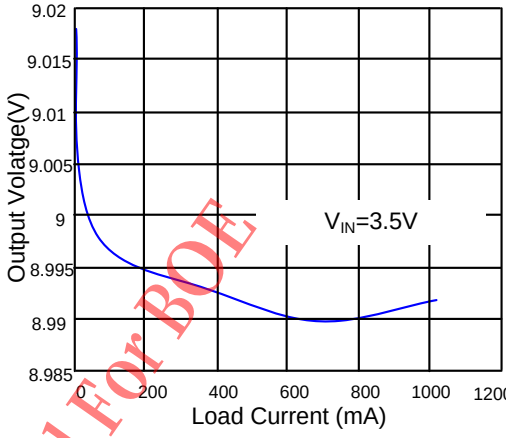
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

Efficiency vs. Load Current

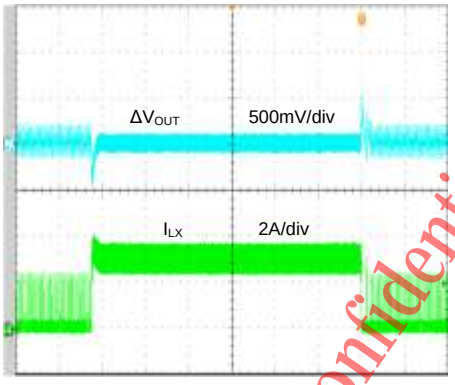


Load Regulation



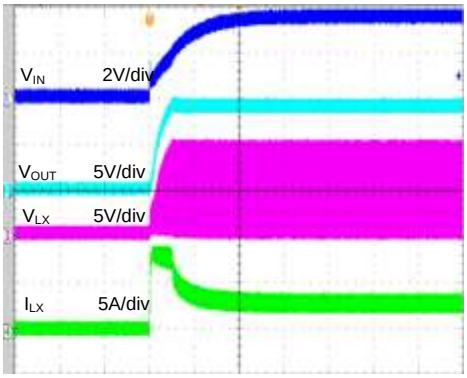
Load Transient

(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=0.1~1A)



Startup from V_{IN}

(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)

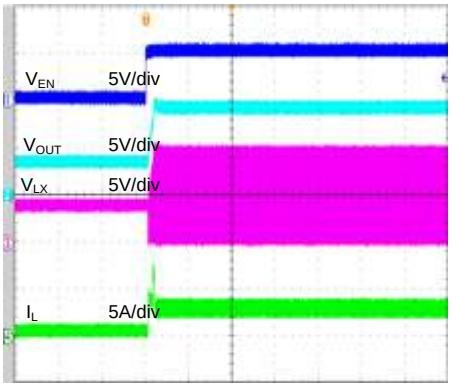


Shutdown from V_{IN}

(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)

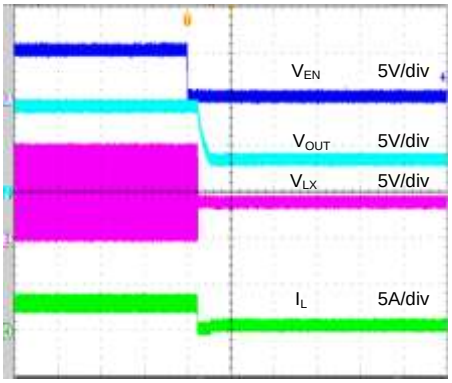
EN ON

(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)



EN OFF

(V_{IN}=3.5V, V_{OUT}=9V,I_{OUT}=1A)



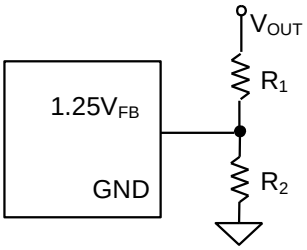
Time(800us/div)

Applications Information

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = (R_1 \times 1.25V) / (V_{OUT} - 1.25V)$$



Current limit Setting resistor R_{ISET}:

Current limit can be programmed by adjusting external resistor R_{ISET} connected to ISET:

$$R_{ISET} = \frac{680A}{I_{SM}} \times k\Omega$$

Programmable constant off time

OFF time can be programmed by adjusting external resistor R_{ADJ} connected to ADJ pin:

$$R_{ADJ} = \frac{T_{OFF}}{10ns} \times k\Omega$$

Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{(V_{OUT} - V_{IN}) \times T_{OFF}}{2\sqrt{3} \times L}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the L_1 and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, L_1 and GND pins. In this case a 10uF low ESR ceramic is recommended.

VCC capacitor C_{VCC}:

The VCC capacitor must be close to the VCC and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{VCC}, and VCC/GND pins. In this case a 2uF low ESR ceramic is recommended.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 35V rating and more than two pcs 10uF capacitor.

Boost inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{IN}}{V_{OUT}} \times \frac{(V_{OUT} - V_{IN}) \times T_{OFF}}{I_{OUT,MAX} \times 40\%}$$

where T_{OFF} is set by R_{ADJ} and $I_{OUT,MAX}$ is the maximum load current.

The SY7219 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > (\frac{V_{OUT}}{V_{IN}}) \times I_{OUT\_MAX} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times F_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low will shut down the device. During the shut down mode, the SY7219 shut down current drops to lower than 1μA. Driving the EN pin high will turn on the IC again.

Diode Selection

Schottky diode is a good choice for high efficiency operation because of its low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than maximum input current. And the average current rating of the diode must be higher than the output current.

Layout Design:

The layout design of SY7219 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{VCC}, L_1, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

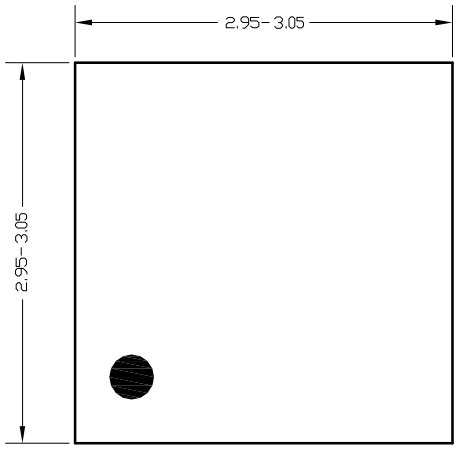
2) C_{OUT} must be close to D_1, Pin LX and Pin GND. The loop area formed by C_{OUT} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

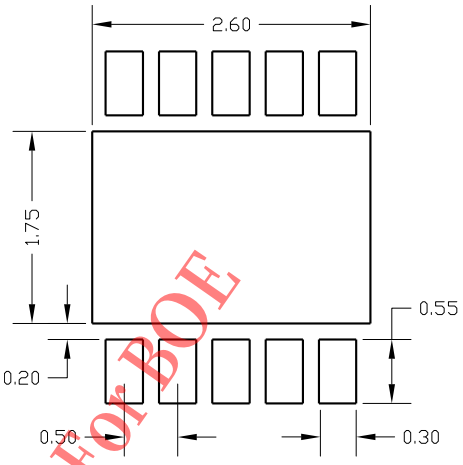
4) The components R_1 and R_2, and the trace connected to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) The VCC capacitor must be close to the VCC and GND pins

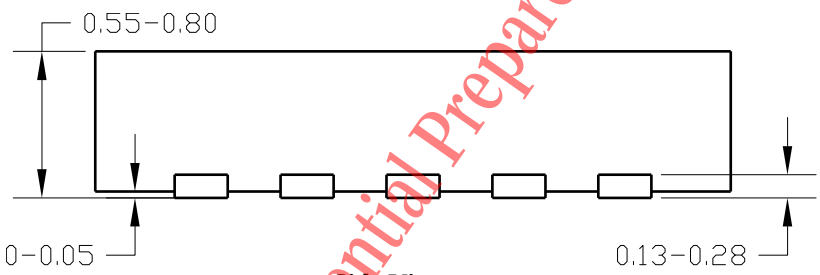
DFN3x3-10 Package outline



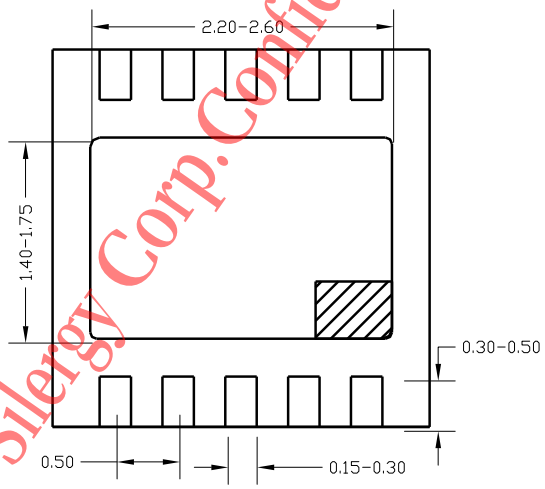
Top View

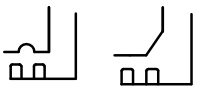


PCB layout (recommended)



Side View





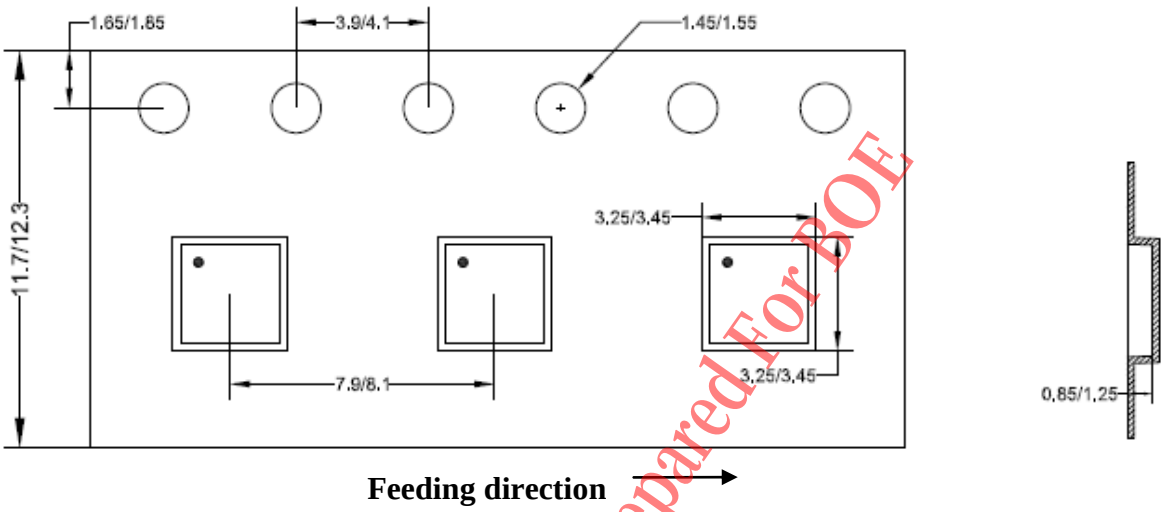
Detail A
Pin1 identifier: two options

Bottom View

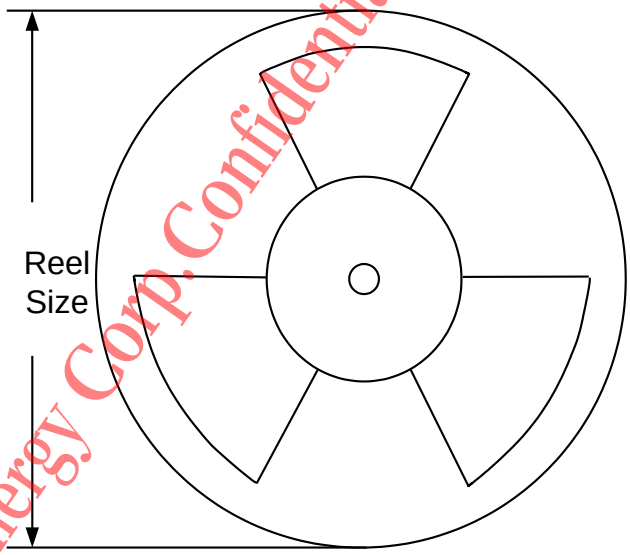
Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

Taping & Reel Specification

1. DFN3x3 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	12	8	13"	400	400	5000

3. Others: NA

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