Application Note: SY80004

21µA Ultra Low I_Q, 2.2MHz Synchronous Step Down Regulator

General Description

The SY80004 is a high efficiency 2.2MHz synchronous step down DC/DC regulator capable of delivering up to 4A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss.

The SY80004 is in a space saving, low profile DFN1.5×1.5-6 package.

Ordering Information

SY80004 □(□□□)
- □□□: Package Code
- □: Optional Spec Code

Ordering Number	Package Type	Note
SY80004DQD	DFN1.5×1.5-6	4A

Features

- 2.5V to 5.5V Input Voltage Range
- Ultra-Fast Load Transient Speed
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 38mΩ /30mΩ
- High Switching Frequency 2.2MHz Minimizes the External Components
- ±1% Feedback or Output Voltage Accuracy (Full Temperature Range)
- PFM Mode for Light Load Efficiency
- 21µA Operating Quiescent Current
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Output Auto Discharge Function
- Power Good Indicator
- Auto Recovery for SCP/OVP/OTP Protection
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.5×1.5-6

Applications

- Portable Electronics
- Industrial PC
- Smart Phone

Typical Applications

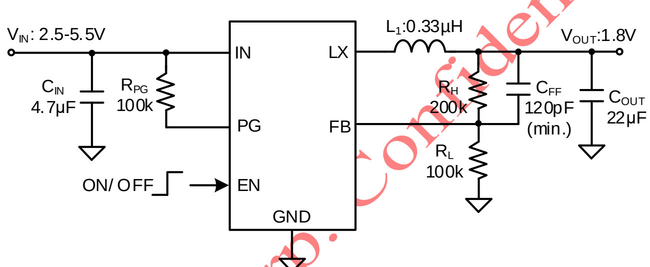


Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V_{OUT} (V)	L(µH)	C_{OUT} (µF) 10	22	44
1.2	0.33		☆	√
	0.47		√	√
1.8	0.33		☆	√
	0.47		√	√
2.5	0.47		☆	√
	0.68		√	√

Note: '☆' means recommended for most applications.

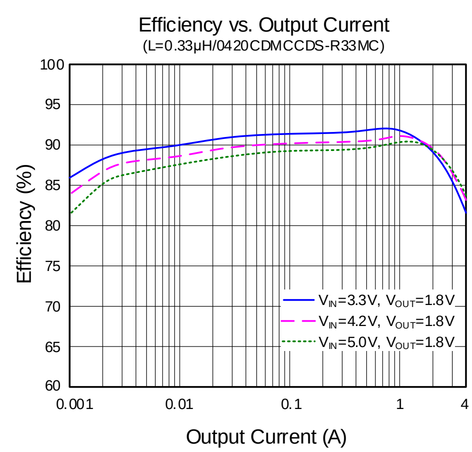
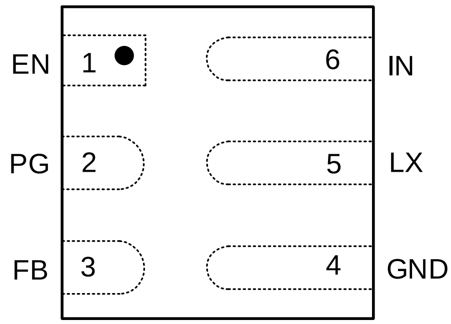


Figure2. Efficiency vs. Output Current

Pinout (top view)



(DFN1.5×1.5-6)

Top Mark: **f9*xyz*** (Device code: **f9**; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not leave it floating.
PG	2	Power good indicator. Power good indicator (open drain output). Low if the V_{FB} < 92% or the V_{FB}>109% of V_{REF}; high otherwise. Connect a pull-up resistor to the input.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
GND	4	Power ground pin.
LX	5	Inductor pin. Connect this pin to the switching node of inductor.
IN	6	Input pin. Decouple this pin to the GND pin with at least a 4.7μF ceramic capacitor.

Block Diagram

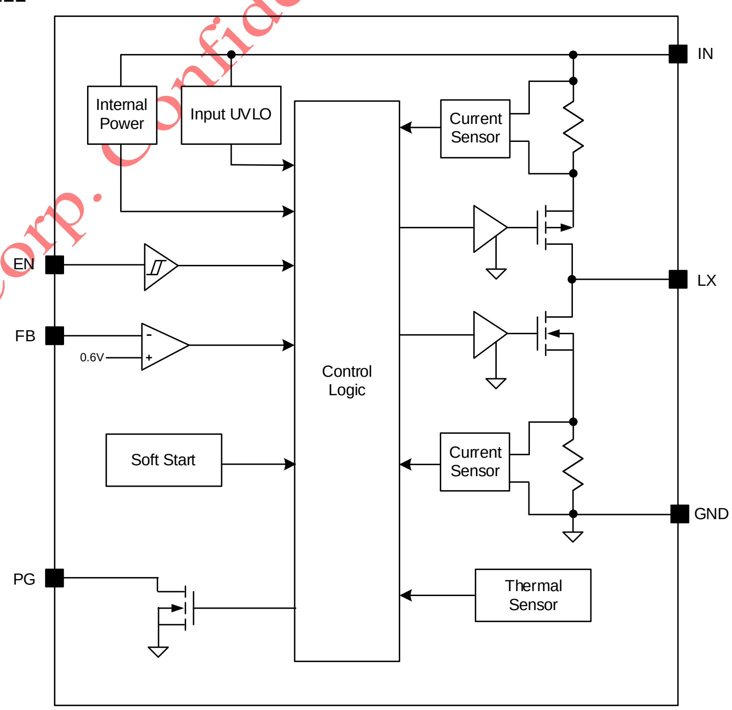


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage---------- -0.3V to 6.0V
FB, EN, PG Voltage---------- -0.3V to V_{IN} + 0.6V
LX Voltage---------- -0.3V (*1) to 6.0V (*2)
Power Dissipation, P_D @ T_A = 25°C ---------- 1.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 62°C/W
θ_{JC} ---------- 8°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage Tested Down to -3V <20ns
(*2) LX Voltage Tested Up to +7V <20ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_J=-40°C~125°C, and V_{IN} = 2.5V to 5.5V. Typical values are at T_J=25°C and V_{IN}=5V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}	V_{IN} falling	2.1	2.2	2.3	V
Input UVLO Hysteresis	V_{HYS}			160		mV
Quiescent Current	I_Q	V_{FB}=105%×V_{REF}		21		µA
Shutdown Current	I_{SHDN}	V_{EN}=0V, T_A=25°C		0.05	0.5	µA
Feedback Reference Voltage	V_{REF}	I_{OUT}=1A, CCM	0.594	0.6	0.606	V
Output Voltage Load Regulation (Note 4)	ΔV_{LDR}	I_{OUT}=0.5A to 4A, V_{OUT}=1.8V		0.1		%/A
Output Discharge FET R_{ON}	R_{DIS}	V_{EN}=0V		8		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			38		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			30		mΩ
EN Input Voltage High	$V_{EN,H}$		1.0			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
EN Leakage Current	$I_{EN,LKG}$	EN=high		0.01		µA
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		92		%
		V_{FB} rising, PG from low to high		95.5		%
		V_{FB} rising, PG from high to low		109		%
		V_{FB} falling, PG from low to high		105		%
Power Good Delay	$t_{PG,R}$	PG from low to high		100		µs
	$t_{PG,F}$	PG from high to low		20		µs
Power Good Output Low	$V_{PG,L}$	I_{PG}=1mA			0.4	V
PG Leakage Current	$I_{PG,LKG}$	V_{PG}=5V		0.01		µA
Min ON Time (Note 4)	$t_{ON,MIN}$			50		ns
Maximum Duty Cycle (Note 4)	D_{MAX}		100			%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft-start Time	t_{SS}	from EN high to 95% of V_{OUT} nominal, T_A=25°C		1.75		ms
Switching Frequency	f_{SW}	I_{OUT}=1A, V_{OUT}=1.8V		2.2		MHz
Top FET Current Limit	$I_{LMT, TOP}$		5			A
Bottom FET Current Limit	$I_{LMT, BOT}$		4			A
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (Note 4)	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A=25°C on a 6cm×6cm size 2-oz two-layer Silergy Evaluation Board.

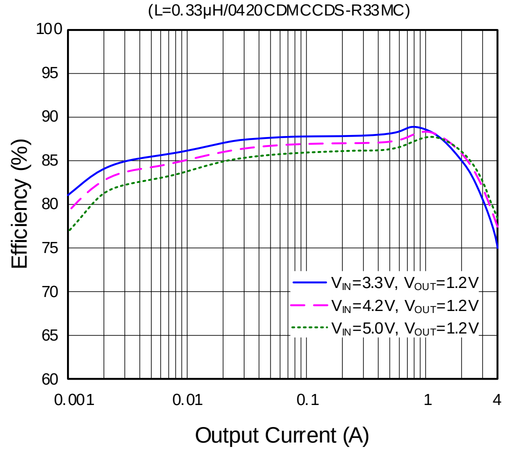
Note 3: The device is not guaranteed to function outside its operating condition.

Note 4: Guaranteed by design.

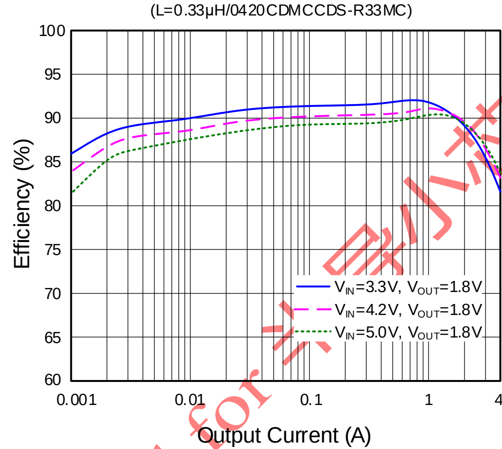
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, L=0.33μH, C_{OUT}=2×10μF, unless otherwise specified.)

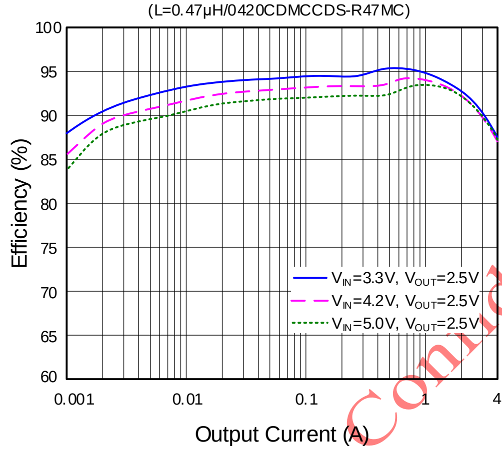
Efficiency vs. Output Current
(L=0.33μH/0420CDMCCDS-R33MC)



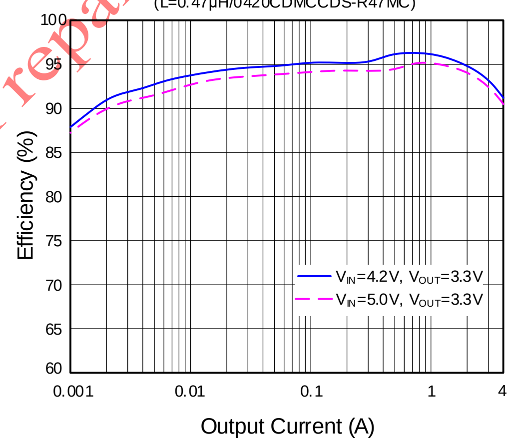
Efficiency vs. Output Current
(L=0.33μH/0420CDMCCDS-R33MC)



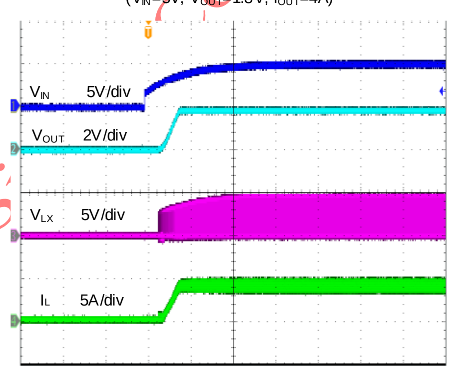
Efficiency vs. Output Current
(L=0.47μH/0420CDMCCDS-R47MC)



Efficiency vs. Output Current
(L=0.47μH/0420CDMCCDS-R47MC)

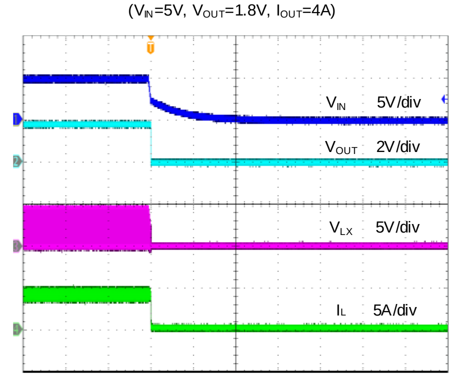


Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



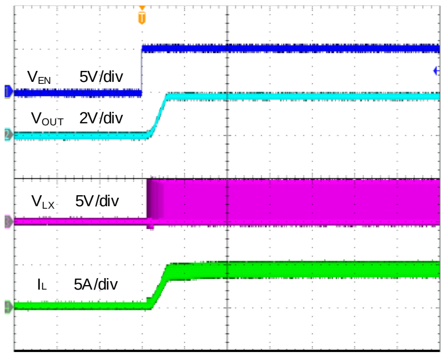
Time (4ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



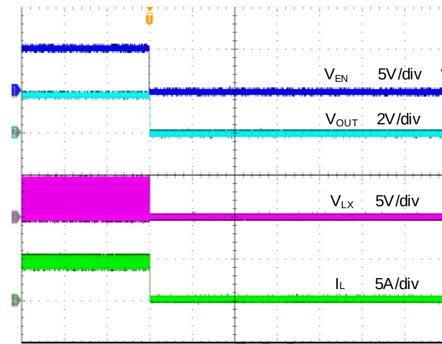
Time (4ms/div)

Startup from EN
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



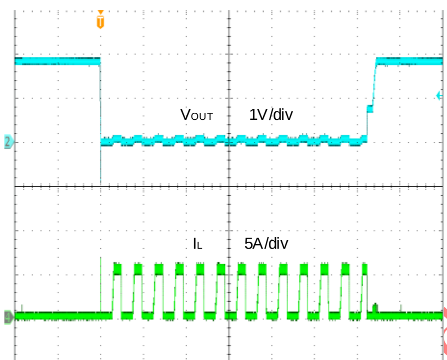
Time (4ms/div)

Shutdown from EN
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



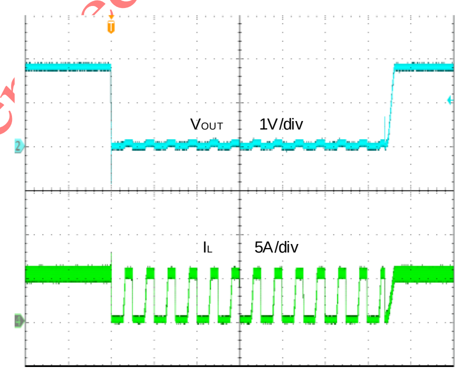
Time (4ms/div)

Short Circuit Protection
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A~short)



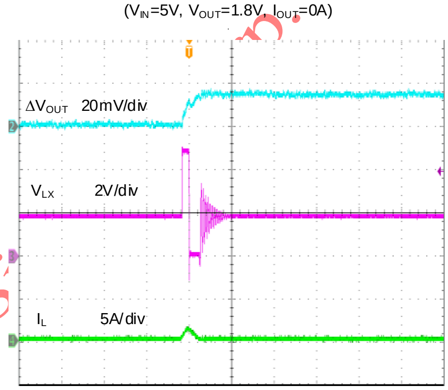
Time (10ms/div)

Short Circuit Protection
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A~short)



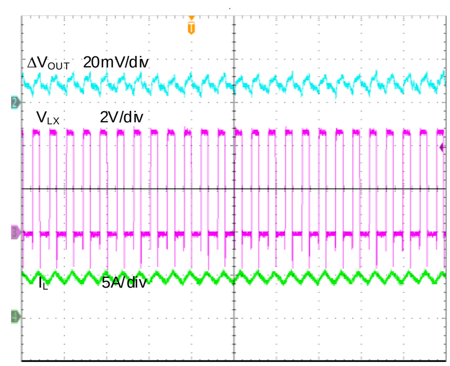
Time (10ms/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



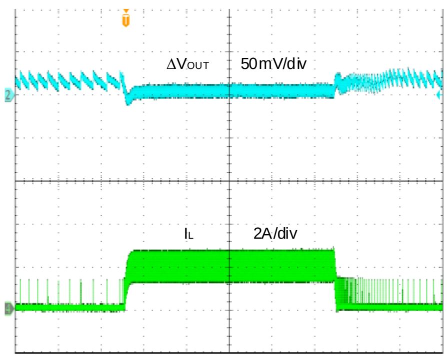
Time (1μs/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



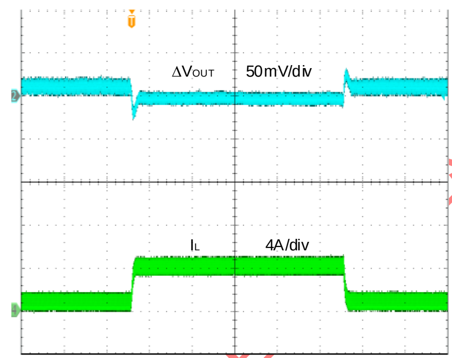
Time (1μs/div)

Load Transient
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0~2A)



Time (100μs/div)

Load Transient
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.4~4A)



Time (100μs/div)

Operation

The SY80004 is a high efficiency 2.2MHz synchronous step-down DC/DC regulator capable of delivering up to 4A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY80004 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads.

The SY80004 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection.

Low output voltage ripple, small external inductor and capacitor sizes are achieved with 2.2MHz switching frequency.

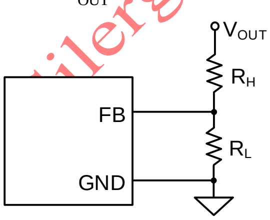
Applications Information

Because of the high integration in the SY80004, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted application specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 1.8V, R_H = 100kΩ is chosen, then using following equation, R_L can be calculated to be 49.9kΩ:

$$R_L = \frac{0.6V}{V_{OUT} - 0.6V} R_H$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor with 6.3V rating should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 4.7μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and more than 2×10μF capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY80004 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<25mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor

The ripple base control strategy needs very little C_{OUT} to confirm stability. Too large inductor and C_{OUT} will lead to unstability. The recommended inductance and output capacitance is shown as below.

Inductance vs. Output Capacitance Selection Table (Note 5)

L (µH)	C_{OUT} (µF)					
	22	44	88	120	180	220
0.33	Note 6	√	√	√	√	√
0.47	√	√	√	√	√	√
0.68	√	√	√	√	×	×

Note 5: Tested with 120pF feedforward capacitor.
Note 6: Only suitable for V_{OUT}<2.0V application.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycles, since even at very low duty cycles, the switching frequency can be reduced as needed once the on-time is close to the minimum on time, to always ensure a proper operation.

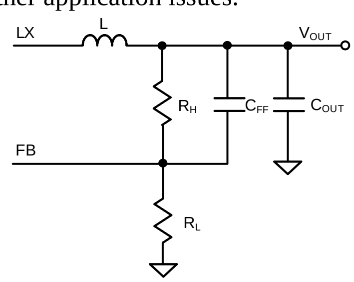
The device will enter 100% dropout mode if the output voltage is very close to the input voltage, while the top FET is constantly turned on, the bottom FET is turned off.

Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be high-impedance. Otherwise, it is pulled low. PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ~100kΩ).

Load Transient Considerations

The SY80004 integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor with more than 120pF capacitance in parallel with R_H may further speed up the load transient responses and is thus highly recommended, otherwise it may result in other application issues.



OCP and UVP Protection Method

TheSY80004 adopts cycle by cycle current limitation for both HS FET and LS FET. If the high side power FET current gets higher than the peak current limit threshold, the high side power FET will turn off and the low side power FET will turn on. If the low side FET current gets higher than the valley current limit threshold, the low side FET will keep turning on until low side FET current decreases below the valley current limit threshold. So, both peak and valley current are limited. If the load current continues to increase in these conditions, the output voltage will drop. When the output voltage falls below 33% of the regulation level, UVP will be triggered and the IC will operate in hic-cup mode. The hic-cup on time and hic-cup off time ratio is 1:1. If the hard short is removed, the IC will return to normal operation.

Layout Design

The layout design of the SY80004 is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN}, L, R_H, R_L and C_{FF}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Place some vias in GND copper for heat sinking too.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_H and R_L, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) The feedback sampling point should be connected with C_{OUT} rather than the inductor output terminal.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

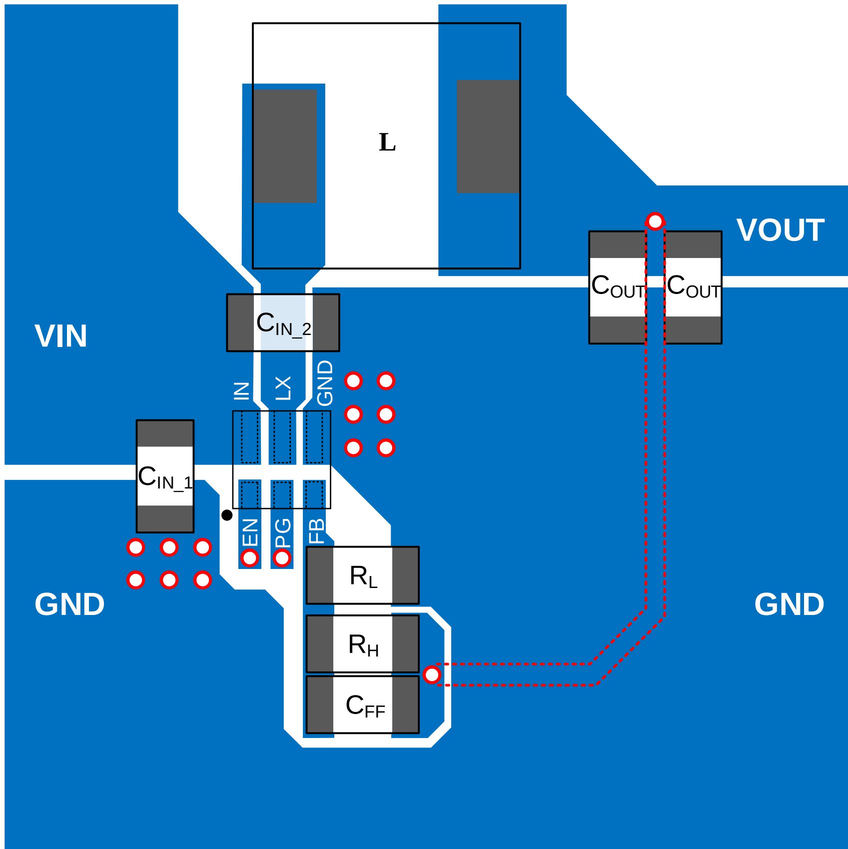
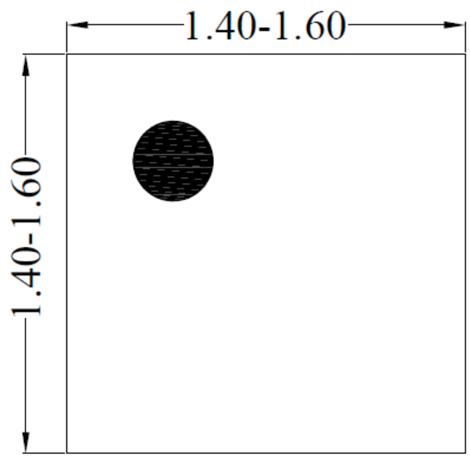
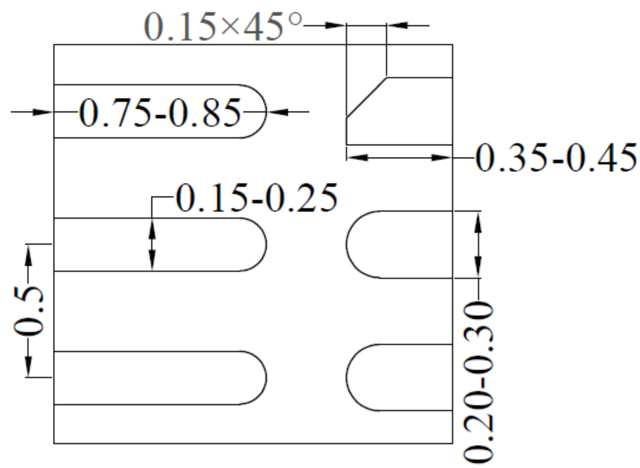


Figure4. PCB Layout Suggestion

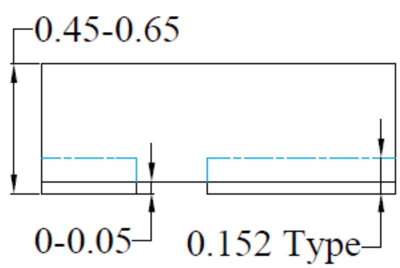
DFN1.5x1.5-6 Package Outline



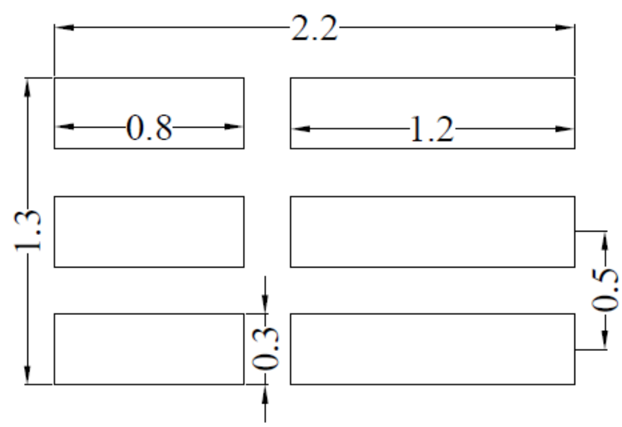
Top View



Bottom View



Front View



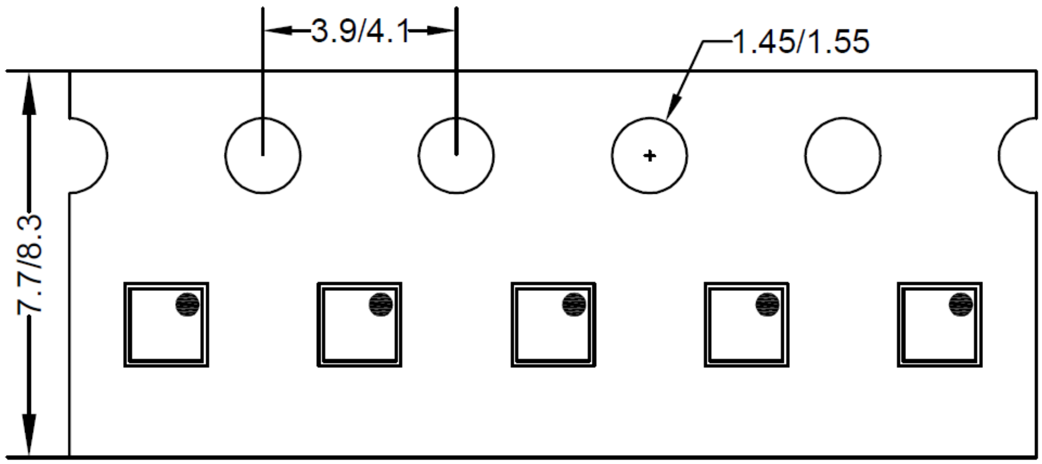
Recommended PCB layout
(only for reference)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

Taping & Reel Specification

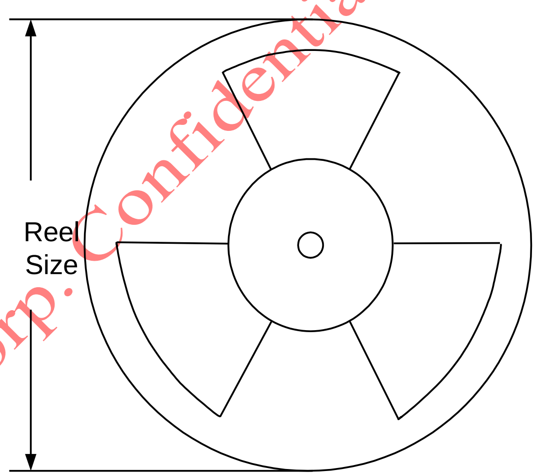
1. Taping orientation

DFN1.5×1.5



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.5×1.5	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov.17, 2022	Revision 0.9A	Update the Package outline (page 11)
Dec.14, 2021	Revision 0.9	Initial Release

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