Application Note: SY8823

Ultra Low Quiescent Current, 2.0MHz, 3.5A Synchronous Step Down Regulator

General Description

SY8823 is a high efficiency ultra low quiescent current, 2.0MHz synchronous step-down DC-DC regulator IC capable of delivering up to 3.5A output current.

SY8823 operates over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss.

Ordering Information

SY8823 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY8823QUC	QFN2x1.5-8	3.5A

Features

- Input voltage range: 2.5V to 5.5V
- 2.0 MHz switching frequency
- 3.5A maximum output current
- Peak current mode control for the fast transient speed
- 100% drop out function
- Typical 18uA quiescent current
- Low $R_{DS(ON)}$ for internal switches (PFET/NFET): 55mΩ/35mΩ
- Hic-cup mode protection for hard short condition
- RoHS Compliant and Halogen Free
- Compact package: QFN2x1.5-8

Applications

- Set Top Box
- Net PC
- Mini-Notebook PC
- Access Point Router

Typical Applications

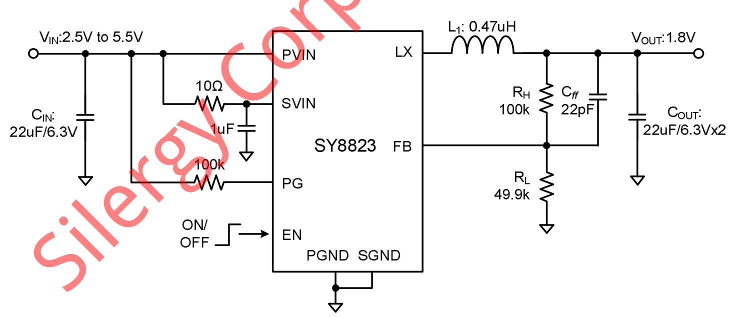


Figure 1. Schematic Diagram

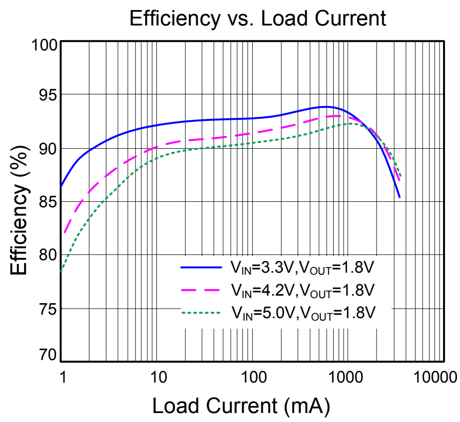
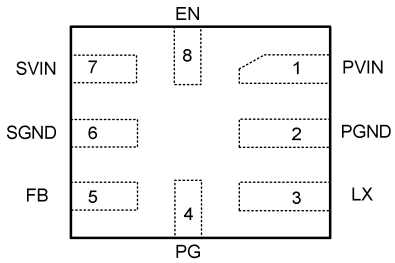


Figure 2. Efficiency Figure

Pinout (top view)



Part Number	Package type	Top Mark①
SY8823QUC	QFN2x1.5-8	**VP***xyz*

*Note①: **x=year code, y=week code, z= lot number code.***

Pin Name	Pin Number	Pin Description
PVIN	1	Supply voltage for power circuit. Decouple this pin to ground with at least 22uF ceramic cap.
PGND	2	Power ground pin.
LX	3	Inductor pin. Connect this pin to the switching node of inductor
PG	4	Power good indicator (Open drain output). Low if the output < 90% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.6V*(1+R_H/R_L).
SGND	6	Signal ground pin.
SVIN	7	Supply voltage for control circuit. Decouple this pin to ground with at least 1uF ceramic cap.
EN	8	Enable input pin. Integrated 4MΩ pull down resistor.

Absolute Maximum Ratings (Note 1)

All pins -- 6V
Power Dissipation, P_D @ T_A = 25°C QFN2x1.5-8---1W
Package Thermal Resistance (Note 2)
θ_{JA} --- 100°C/W
θ_{JC} --- 15°C/W
Junction Temperature Range --- 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C
Dynamic LX voltage in 10ns duration --- -4V to +7V

Recommended Operating Conditions (Note 3)

Supply Input Voltage -- 2.5V to 5.5V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range --- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 0.47uH, C_{OUT} = 22uF, T_A = 25°C, unless otherwise specified)

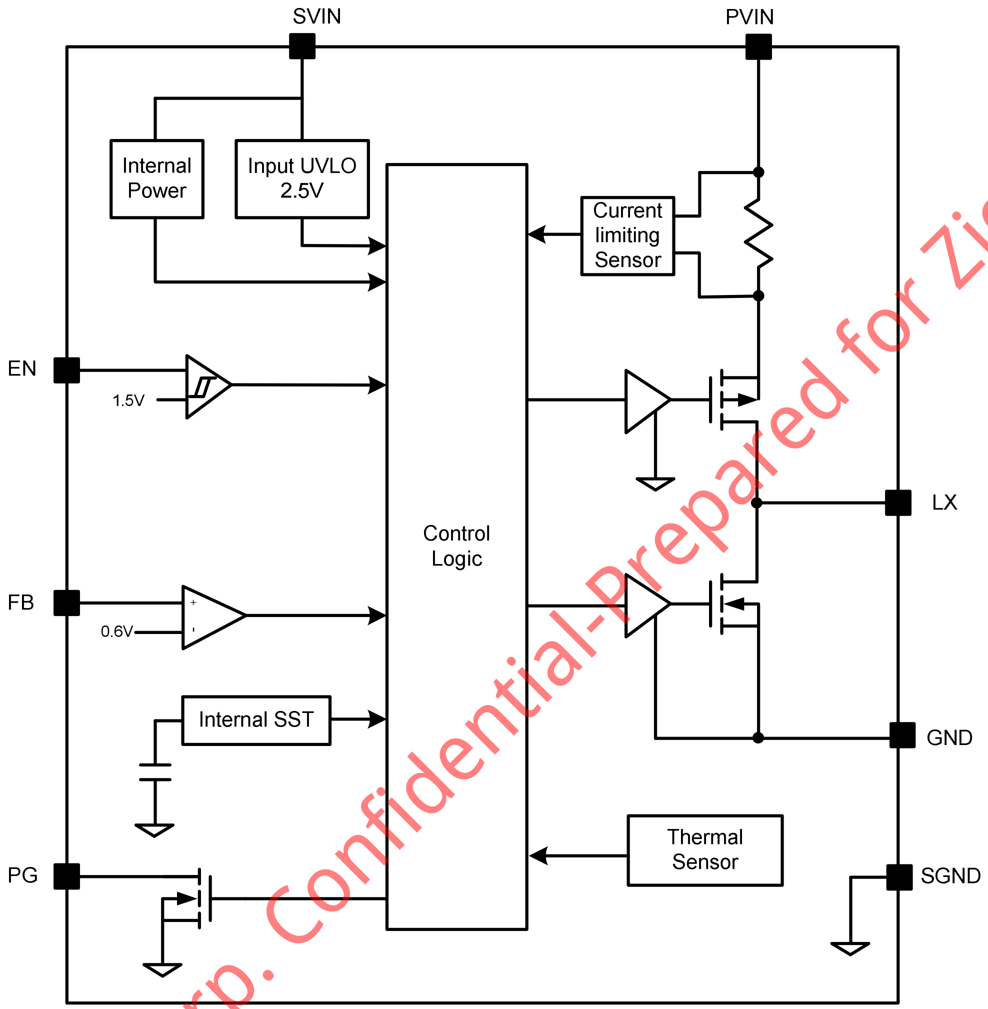
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=$V_{REF}\cdot$ 105%		18		µA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	µA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
PFET RON	$R_{DS(ON),P}$		30	55	80	mΩ
NFET RON	$R_{DS(ON),N}$		15	35	55	mΩ
Peak Current Limit	I_{LIM}		4.5		7.5	A
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.5	V
UVLO hysteresis	V_{HYS}			0.15		V
Oscillator Frequency	F_{OSC}	I_{OUT}=500mA		2		MHz
PGOOD Under-voltage Threshold	$V_{FB,LV}$			0.55		V
Short Circuit Protection Threshold	V_{SCP}			0.26		V
Min ON Time				80		ns
Soft Start time	T_{SS}			1		ms
Output Discharge Switch On Resistance	R_{DSC}			50		Ω
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

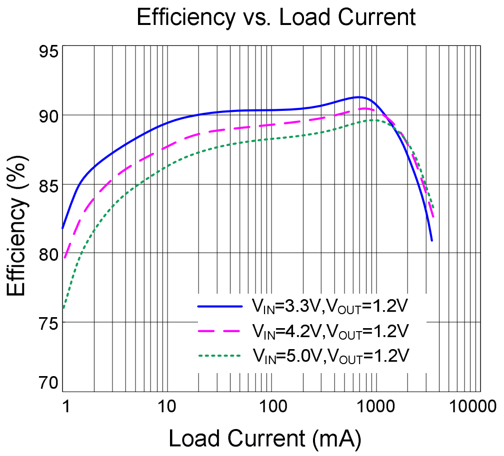
Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

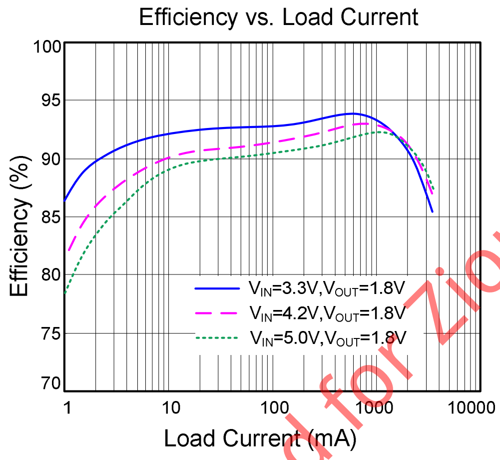
Note 3: The device is not guaranteed to function outside its operating conditions.

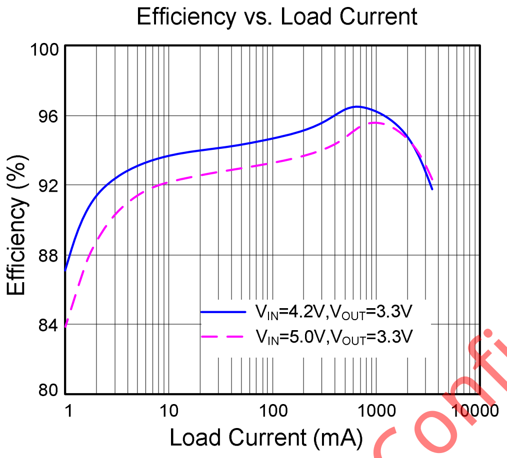
Block Diagram

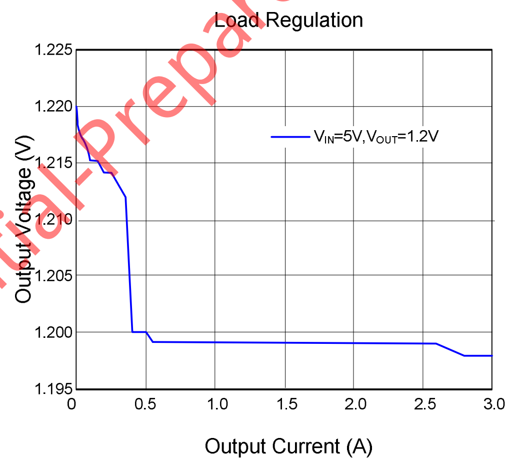


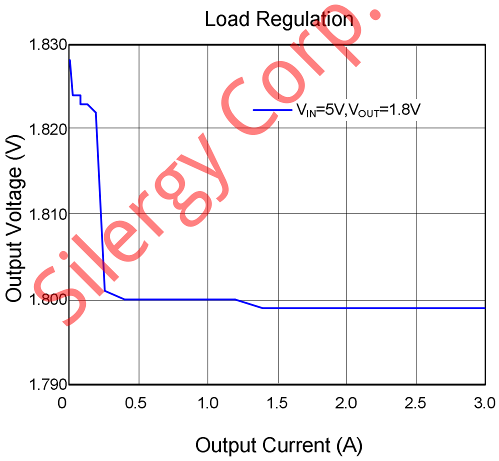
Typical Performance Characteristics

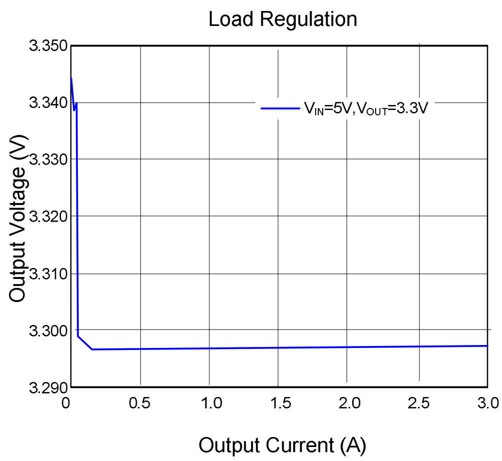




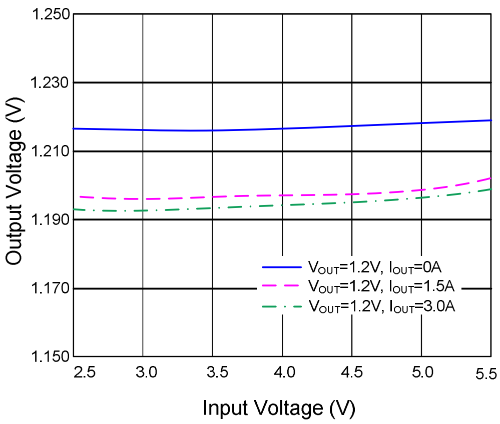






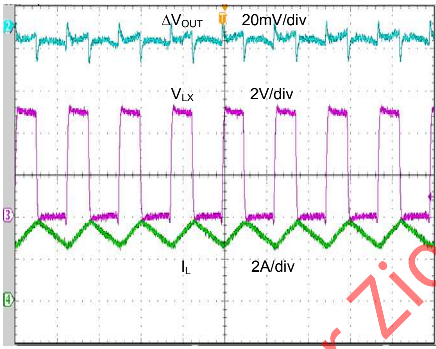


Line Regulation



Output Ripple

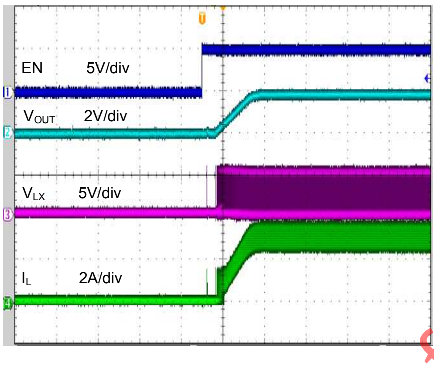
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.5A)



Time (400ns/div)

Startup from Enable

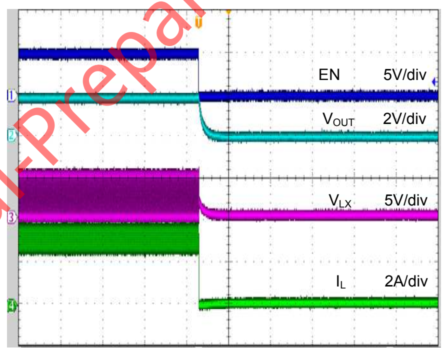
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.5A)



Time (800μs/div)

Shutdown from Enable

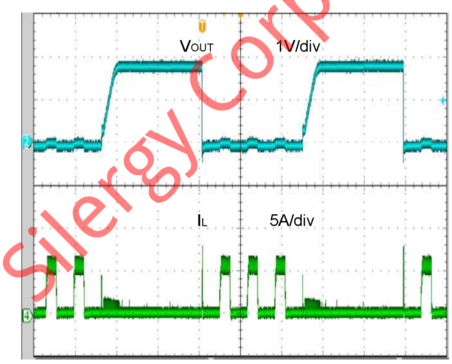
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.5A)



Time (200μs/div)

Short Circuit Protection

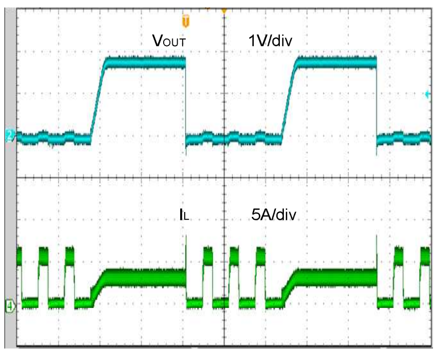
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ Short)



Time (2ms/div)

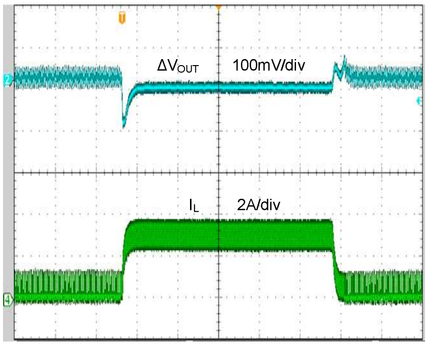
Short Circuit Protection

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=3.5A ~ Short)



Time (2ms/div)

Load Transient
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.3 ~ 3.5A)



Time (100μs/div)

Operation

SY8823 is an ultra low quiescent current synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching losses and conduction losses. With low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC achieves a higher efficiency with high switching frequency to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

SY8823 senses the output voltage conditions for the fault protection. If the DC output voltage is about 3% over the regulation level, both switches turn off and remain in the off state. If the DC output voltage is below 42% of the regulation level, the IC will enter hic-up short protection mode. When the output voltage is below 42% of the regulation, the frequency is folded back to 25% of the normal frequency and the current limit is decreased to 55% of the normal current limit to prevent the inductor current runaway and to reduce the power dissipation within the IC under true short circuit conditions.

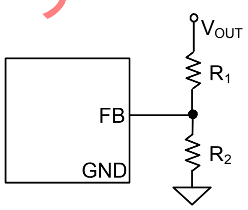
Applications Information

Because of the high integration in SY8823, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback resistor divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=100k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6}(\Omega)$$



Input capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}\ (A)$$

This formula has a maximum at $V_{IN}=2\times V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$.

With the maximum load current at 3.5A, a typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the PVIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, PVIN and GND pins.

A 1μF ceramic capacitor needs to be added across SVIN and GND.

Output capacitor C_{OUT}

Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and more than two pcs 22μF capacitors.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN\_MAX})}{F_{SW} \times I_{OUT\_MAX} \times 40\%}(H)$$

Where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY8823 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown, the SY8823 shutdown current drops to lower than 0.1µA, Driving the EN pin high (>1.5V) will turn on the IC again.

Power Good Indication

PG is an open-drain output pin. Connect an above 100k pull-up resistor to V_{IN}. PG pin will output high after the output voltage exceeds 90% of normal output voltage.

Load Transient Considerations:

SY8823 integrates the compensation components to achieve good stability and fast transient responses. Adding a 10pF~22pF ceramic capacitor in parallel with R_1 may further speed up the load transient responses.

Layout Design:

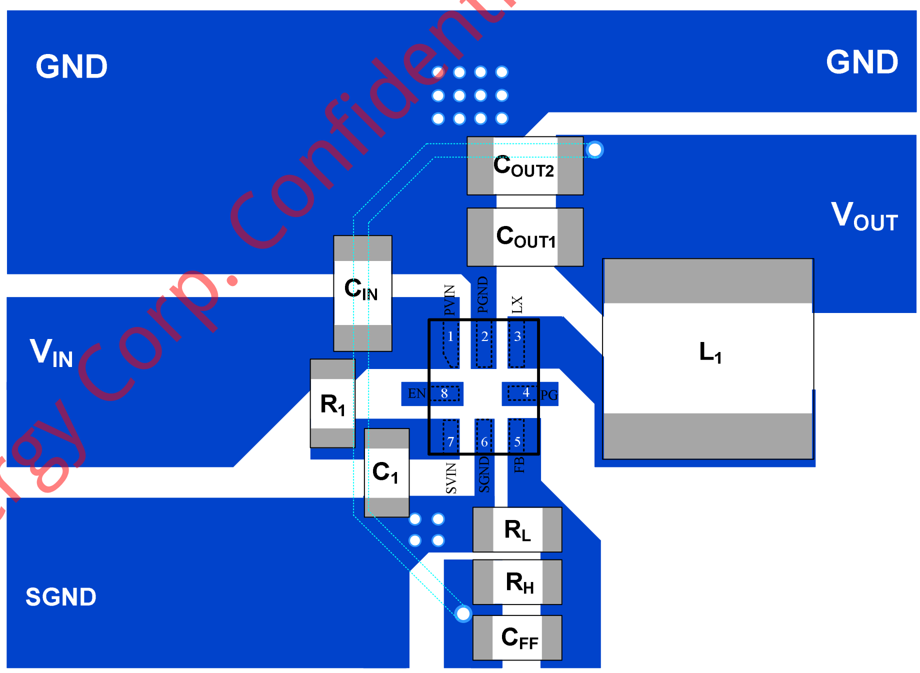
To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, L, R_L, R_H, C_{FF}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance

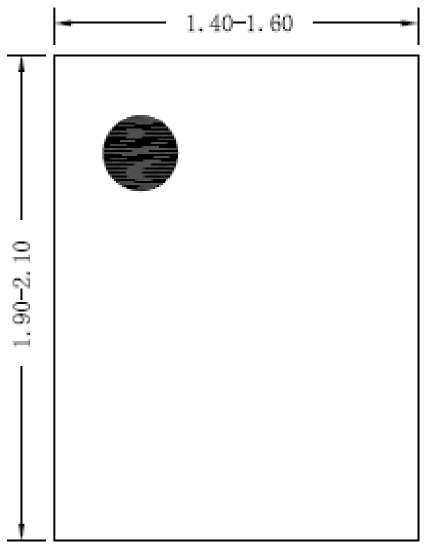
2) The decoupling capacitor of PVIN and SVIN must be placed as close as possible to the pins. The loop area formed by the capacitors and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

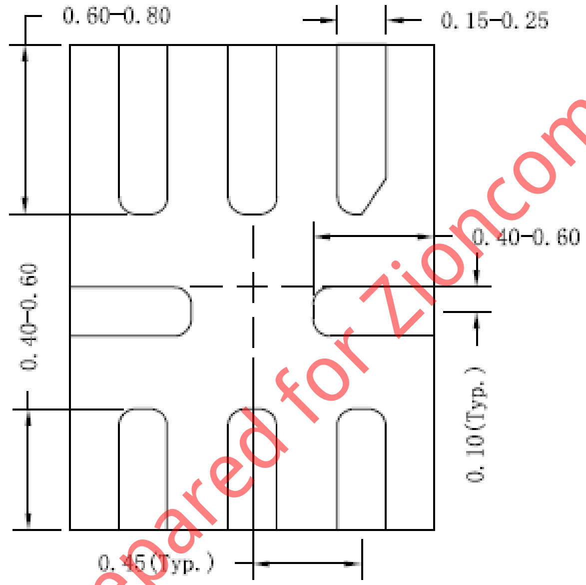
4) The components R_L, R_H and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.



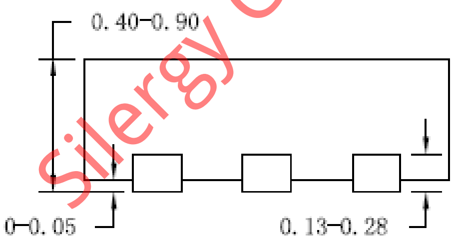
QFN2x1.5-8 Package Outline Drawing



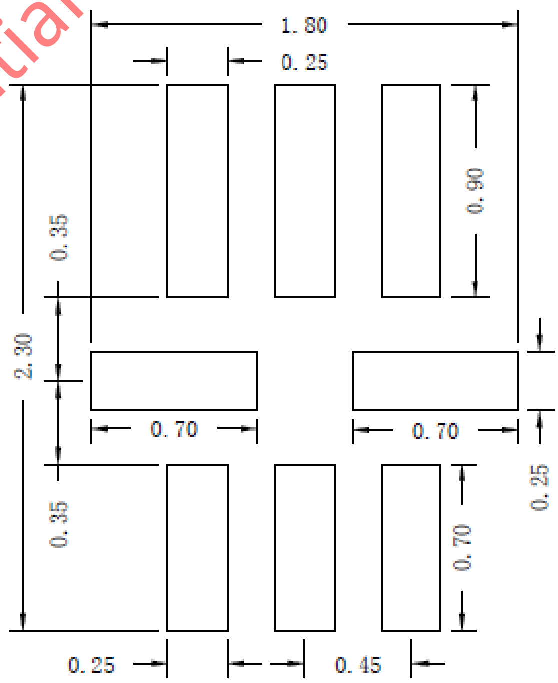
Top View



Bottom View



Side View

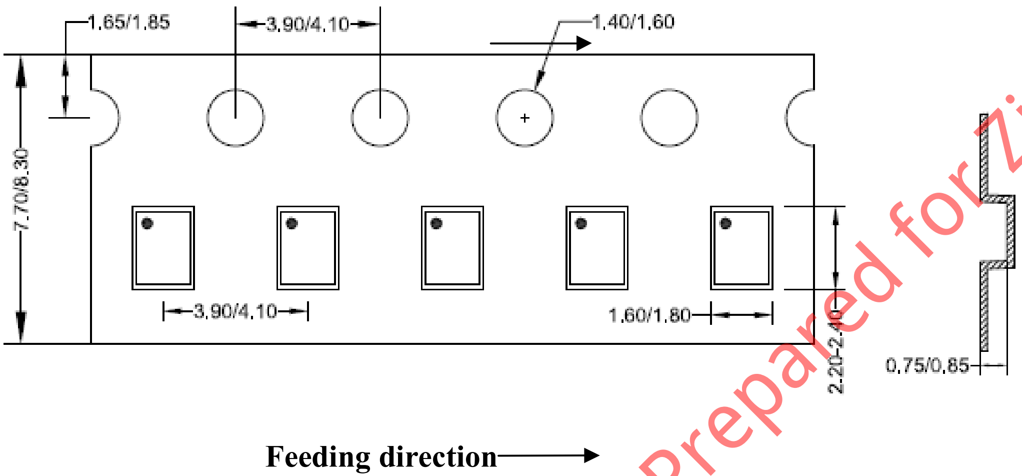


Recommended PCB layout
(Reference only)

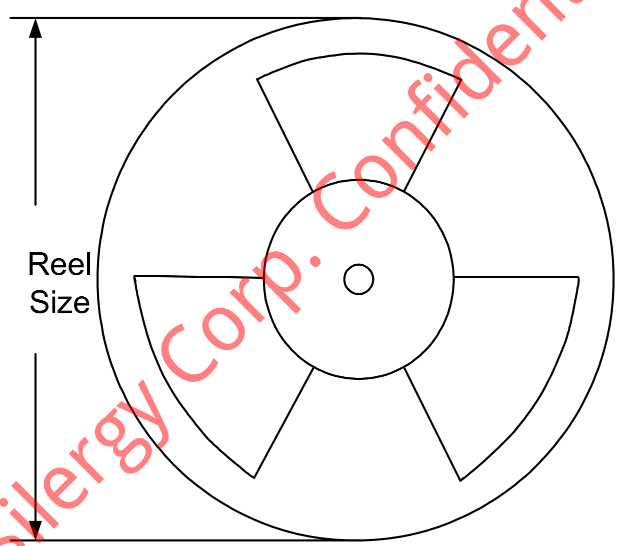
Notes: All dimension in millimeter and exclude mold flash & metal burr

Taping & Reel Specification

1. QFN2x1.5 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2x1.5	8	4	7	400	160	3000

3. Others: NA