Si554

REVISION D

QUAD FREQUENCY VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO) 10 MHZ TO 1.4 GHZ

Features

- Available with any-rate output frequencies from 10–945 MHz and selected frequencies to 1.4 GHz
- Four selectable output frequencies
- 3rd generation DSPLL® with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

Ordering Information:

See page 9.

Applications

- SONET/SDH
- xDSL
- 10 GbE LAN / WAN
- Low jitter clock generation
- Optical modules
- Clock and data recovery

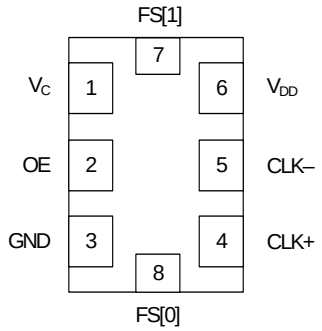
Description

The Si554 quad-frequency VCXO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a very low jitter clock for all output frequencies. The Si554 is available with any-rate output frequency from 10 to 945 MHz and selected frequencies to 1400 MHz. Unlike traditional VCXOs, where a different crystal is required for each output frequency, the Si554 uses one fixed crystal frequency to provide a wide range of output frequencies. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si554 IC-based VCXO is factory-configurable for a wide variety of user specifications including frequency, supply voltage, output format, tuning slope, and temperature stability. Specific configurations are factory-programmed at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

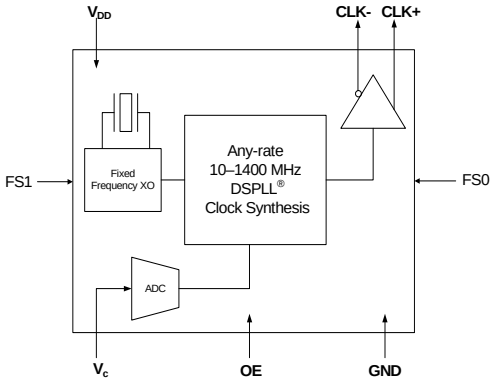
Pin Assignments:

See page 8.

(Top View)



Functional Block Diagram



1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	I_{DD}	Output enabled				mA
		LVPECL	—	120	130	
		CML	—	108	117	
		LVDS	—	99	108	
		CMOS	—	90	98	
		Tristate mode	—	60	75	mA
Output Enable (OE) and Frequency Select FS[1:0][2]		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	V
Operating Temperature Range	T_A		–40	—	85	ºC

Notes:
1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 9 for further details.
2. OE and FS[1:0] pins include a 17 kΩ resistor to VDD.

Table 2. V_C Control Voltage Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope[1,2,3]	K_V	10 to 90% of V_{DD}	—	33 45 90 135 180 356	—	ppm/V
Control Voltage Linearity[4]	L_{VC}	BSL	–5	±1	+5	%
		Incremental	–10	±5	+10	%
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V_C Input Impedance	Z_{VC}		500	—	—	kΩ
Nominal Control Voltage	V_{CNOM}	@ f_O	—	$V_{DD}/2$	—	V
Control Voltage Tuning Range	V_C		0		V_{DD}	V

Notes:
1. Positive slope; selectable option by part number. See Section 3. "Ordering Information" on page 9.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. K_V variation is ±10% of typical values.
4. BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope determined with V_C ranging from 10 to 90% of V_{DD}.

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency[1,2,3]	f_O	LVDS/CML/LVPECL	10	—	945	MHz
		CMOS	10	—	160	MHz
Temperature Stability[1,4]		T_A = –40 to +85 °C	–20 –50 –100	— — —	+20 +50 +100	ppm
Absolute Pull Range[1,4]	APR		±12	—	±375	ppm
Aging		Frequency drift over first year.	—	—	±3	ppm
		Frequency drift over 15 year life.	—	—	±10	
Power up Time[5]	t_{OSC}		—	—	10	ms
Settling Time After FS[1:0] Change	t_{FRQ}	Both FS[1] and FS[0] changing simultaneously	—	—	20	ms

Notes:
1. See Section 3. "Ordering Information" on page 9 for further details.
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
3. Nominal output frequency set by $V_{CNOM} = V_{DD}/2$.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to f_O (to within ±1 ppm of f_O).

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option[2]	V_O	2.5/3.3 V option mid-level	—	V_{DD} – 1.30	—	V
		1.8 V option mid-level	—	V_{DD} – 0.36	—	V
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V_{PP}
		1.8 V option swing (diff)	0.35	0.425	0.50	V_{PP}
CMOS Output Option[3]	V_{OH}	I_{OH} = 32 mA	0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}	I_{OL} = 32 mA	—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C_L = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V_{DD}/2	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF

Table 5. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2,3] for $F_{OUT} \geq 500$ MHz	ϕ_J	Kv = 33 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.26	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 45 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.27	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 90 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.32	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 135 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.40	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.27	—	
		Kv = 180 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.49	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.28	—	
		Kv = 356 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.87	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.33	—	

Notes:

1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with V_C=1.65V, V_{DD}=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for $F_{OUT} \geq 250$ MHz, 20 MHz for 50 MHz $\leq F_{OUT}$ <250 MHz, 2 MHz for 10 MHz $\leq F_{OUT}$ <50 MHz.

Table 5. CLK± Output Phase Jitter (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2,3,4,5] for F_{OUT} of 125 to 500 MHz	ϕ_J	Kv = 33 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.37	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.33	—	
		Kv = 45 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.37	0.4	ps
		50 kHz to 80 MHz (OC-192)	—	0.33	—	
		Kv = 90 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.43	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.34	—	
		Kv = 135 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.50	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.34	—	
		Kv = 180 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.59	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.35	—	
		Kv = 356 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	1.00	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.39	—	

Notes:

1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with V_C=1.65V, V_{DD}=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for $F_{OUT} \geq$ 250 MHz, 20 MHz for 50 MHz $\leq F_{OUT}$ <250 MHz, 2 MHz for 10 MHz $\leq F_{OUT}$ <50 MHz.

Table 5. CLK± Output Phase Jitter (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2,5] for F_{OUT} 10 to 160 MHz CMOS Output Only	ϕ_J	Kv = 33 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.63	—	ps
		50 kHz to 20 MHz	—	0.62	—	
		Kv = 45 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.63	—	ps
		50 kHz to 20 MHz	—	0.62	—	
		Kv = 90 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.67	—	ps
		50 kHz to 20 MHz	—	0.66	—	
		Kv = 135 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.74	—	ps
		50 kHz to 20 MHz	—	0.72	—	
		Kv = 180 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.83	—	ps
		50 kHz to 20 MHz	—	0.8	—	
		Kv = 356 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	1.26	—	ps
		50 kHz to 20 MHz	—	1.2	—	

Notes:
1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with V_C=1.65V, V_{DD}=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for $F_{OUT} \geq$ 250 MHz, 20 MHz for 50 MHz $\leq F_{OUT}$ <250 MHz, 2 MHz for 10 MHz $\leq F_{OUT}$ <50 MHz.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J_{PER}	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	ps

***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

Table 7. CLK± Output Phase Noise (Typical)

Offset Frequency	74.25 MHz 90 ppm/V LVPECL	491.52 MHz 45 ppm/V LVPECL	622.08 MHz 135 ppm/V LVPECL	Units
100 Hz	–87	–75	–65	dBc/Hz
1 kHz	–114	–100	–90	
10 kHz	–132	–116	–109	
100 kHz	–142	–124	–121	
1 MHz	–148	–135	–134	
10 MHz	–150	–146	–146	
100 MHz	n/a	–147	–147	

Table 8. Environmental Compliance

The Si554 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016
Moisture Sensitivity Level	J-STD-020, MSL 1
Contact Pads	J-STD-020, MSL 1

Table 9. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	ºC
Supply Voltage, 1.8 V Option	V_{DD}	–0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V_{DD}	–0.5 to +3.8	V
Input Voltage (any input pin)	V_I	–0.5 to V_{DD} + 0.3	V
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2000	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	ºC
Soldering Temperature Time @ T_{PEAK} (Pb-free profile)[2]	t_P	20–40	seconds

Notes:

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from www.silabs.com/VCXO for further information, including soldering profiles.

2. Pin Descriptions

(Top View)

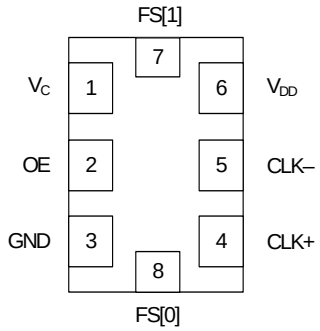


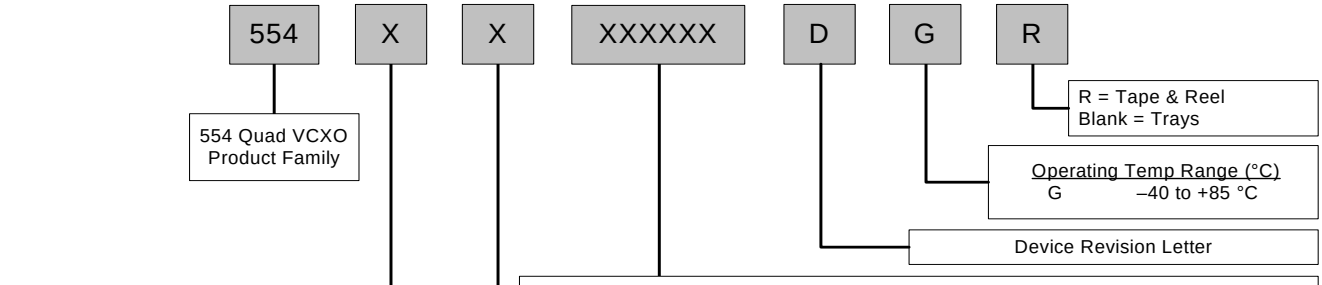
Table 10. Si554 Pin Descriptions

Pin	Name	Type	Function
1	V_C	Analog Input	Control Voltage
2	OE*	Input	Output Enable (Polarity = High): 0 = clock output disabled (outputs tri-stated) 1 = clock output enabled
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK– (N/A for CMOS)	Output	Complementary Output (N/C for CMOS)
6	V_{DD}	Power	Power Supply Voltage
7	FS[1]*	Input	Frequency Select MSB
8	FS[0]*	Input	Frequency Select LSB

***Note:** FS[1:0] and OE include a 17 kΩ pullup resistor to V_{DD}. Output Enable polarity selectable at time of order. See Section 3. "Ordering Information" on page 9 for details on frequency select and OE polarity ordering options.

3. Ordering Information

The Si554 supports a variety of options including frequency, temperature stability, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si554 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si554 VCXO series is supplied in an industry-standard, RoHS-compliant, lead-free, 8-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.



6-digit Frequency Designator Code

Four unique frequencies can be specified within the following bands of frequencies: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz. A six digit code will be assigned for the specified combination of frequencies. Codes > 000100 refer to XOs programmed with the lowest frequency value selected when FS[1:0] = 00, and the highest value when FS[1:0] = 11. Six digit codes < 000100 refer to XOs programmed with the highest frequency value selected when FS[1:0] = 00, and the lowest value when FS[1:0] = 11.

1st Option Code

	V_{DD}	Output Format	Output Enable Polarity
A	3.3	LVPECL	High
B	3.3	LVDS	High
C	3.3	CMOS	High
D	3.3	CML	High
E	2.5	LVPECL	High
F	2.5	LVDS	High
G	2.5	CMOS	High
H	2.5	CML	High
J	1.8	CMOS	High
K	1.8	CML	High
M	3.3	LVPECL	Low
N	3.3	LVDS	Low
P	3.3	CMOS	Low
Q	3.3	CML	Low
R	2.5	LVPECL	Low
S	2.5	LVDS	Low
T	2.5	CMOS	Low
U	2.5	CML	Low
V	1.8	CMOS	Low
W	1.8	CML	Low

Note:
CMOS available to 160 MHz.

2nd Option Code

Code	Temperature Stability ± ppm (max)	Tuning Slope Kv ppm/V (typ)	Minimum APR (±ppm) for VDD @ 3.3 V	2.5 V	1.8 V
A	100	180	100	75	25
B	100	90	30	Note 6	Note 6
C	50	180	150	125	75
D	50	90	80	30	25
E	20	45	25	Note 6	Note 6
F	50	135	100	75	50
G	20	356	375	300	235
H	20	180	185	145	105
J	20	135	130	104	70
K	100	356	295	220	155
M	20	33	12	Note 6	Note 6

Notes:
1. For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Unlike SAW-based solutions which require higher higher Kv values to account for their higher temperature dependence, the Si55x series provides lower Kv options to minimize noise coupling and jitter in real-world PLL designs. See AN255 and AN266 for more information.
2. APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±25 ppm is able to lock to a clock with a ±25 ppm stability over 15 years over all operating conditions.
3. Nominal Pull range (±) = 0.5 x V_{DD} x tuning slope.
4. Nominal Absolute Pull Range (±APR) = Pull range – stability – lifetime aging
   = 0.5 x V_{DD} x tuning slope – stability – 10 ppm
5. Minimum APR values noted above include worst case values for all parameters.
6. Combination not available.

Example Part Number: 554AF000124DGR is a 5 x 7 mm Quad VCXO in an 8 pad package. Since the six digit code (000124) is > 000100, f0 is 622.08 MHz (lowest frequency), f1 is 644.53125, f2 is 657.42188, and f3 is 669.32658 MHz (highest frequency), with a 3.3 V supply, LVPECL output, and Output Enable active high polarity. Temperature stability is specified as ±50 ppm and the tuning slope is 135 ppm/V. The part is specified for a –40 to +85 C° ambient temperature range operation and is shipped in tape and reel format.

Figure 1. Part Number Convention

4. Package Outline and Suggested Pad Layout

Figure 2 illustrates the package details for the Si554. Table 11 lists the values for the dimensions shown in the illustration.

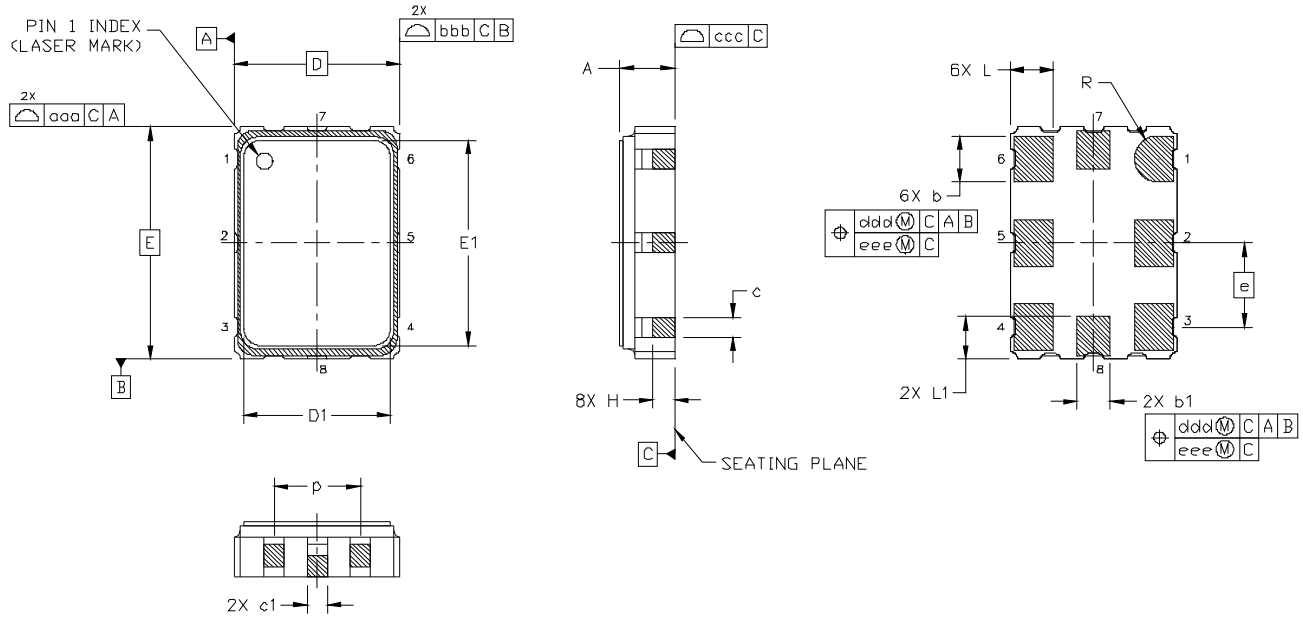


Figure 2. Si554 Outline Diagram

Table 11. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
b1	0.90	1.00	1.10
c	0.50	0.60	0.70
c1	0.30	—	0.60
D		5.00 BSC	
D1	4.30	4.40	4.50
e		2.54 BSC	
E		7.00 BSC	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	1.07	1.17	1.27
p	1.80	—	2.60
R		0.70 REF	
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10
eee	—	—	0.05

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5. 8-Pin PCB Land Pattern

Figure 3 illustrates the 8-pin PCB land pattern for the Si554. Table 12 lists the values for the dimensions shown in the illustration.

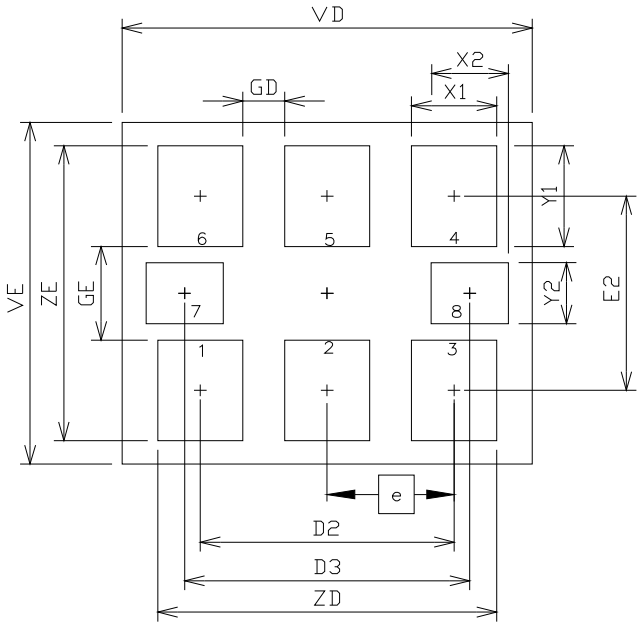


Figure 3. Si554 PCB Land Pattern

Table 12. PCB Land Pattern Dimensions (mm)

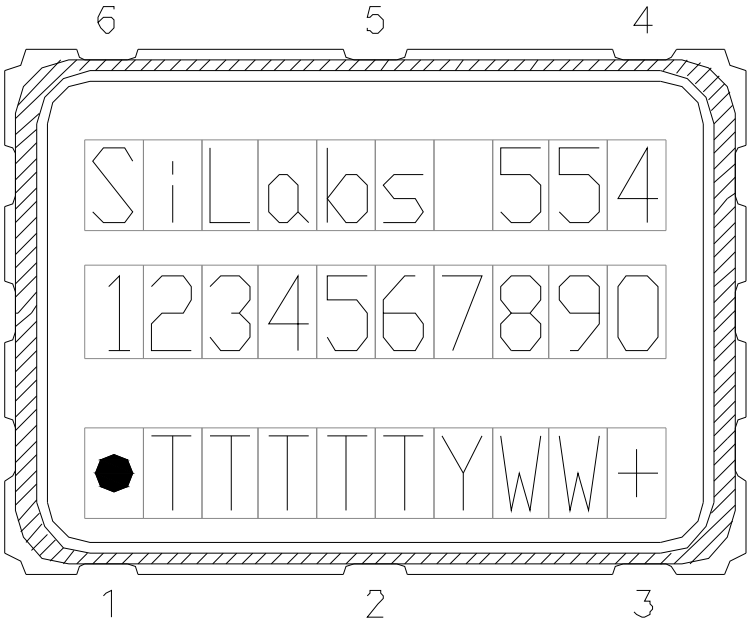
Dimension	Min	Max
D2	5.08 REF	
D3	5.705 REF	
e	2.54 BSC	
E2	4.20 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X1	1.70 TYP	
X2	1.545 TYP	
Y1	2.15 REF	
Y2	1.3 REF	
ZD	—	6.78
ZE	—	6.30

Note:

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design follows IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

6. Top Marking

6.1. Si554 Top Marking



6.2. Top Marking Explanation

Line	Position	Description
1	1–10	"SiLabs"+ Part Family Number, 554 (First 3 characters in part number)
2	1–10	Si554: Option1+Option2+Freq(7)+Temp Si554 w/ 8-digit resolution: Option1+Option2+ConfigNum(6)+Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	"+" to indicate Pb-Free and RoHS-compliant

DOCUMENT CHANGE LIST

Revision 0.6 to Revision 1.0

- Updated Table 4 on page 3.
  - Updated 2.5 V/3.3 V and 1.8 V CML output level specifications.
- Updated Table 5 on page 4.
  - Removed the words “Differential Modes: LVPECL/LVDS/CML” in the footnote referring to AN256.
  - Added footnotes clarifying max offset frequency test conditions.
  - Added CMOS phase jitter specs.
- Updated Table 9 on page 7.
  - Separated 1.8 V, 2.5 V/3.3 V supply voltage specifications.
  - Updated ESD HBM sensitivity rating.
- Updated and clarified Table 8 on page 7
  - Added “Moisture Sensitivity Level” and “Contact Pads” rows.
- Updated 6. "Top Marking" on page 12 to reflect specific marking information (previously, figure was generic).
- Updated 4. "Package Outline and Suggested Pad Layout" on page 10.
  - Added cyrstal impedance pin in Figure 2 on page 10 and Table 11 on page 10.
- Reordered spec tables and back matter to conform to data sheet quality conventions.

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