C8051F55x/56x/57x

C8051F560 DEVELOPMENT KIT USER'S GUIDE

1. Relevant Devices

The C8051F560 Development Kit is intended as a development platform for the microcontrollers in the C8051F55x/56x/57x MCU family.

- The target board included in this kit is provided with a pre-soldered **C8051F568** MCU (QFN40 package) and a **C8051F550** MCU (QFN24 package).
- Code developed on the C8051F568 can be easily ported to the other members of this MCU family.
- Refer to the C8051F55x/56x/57x data sheet for the differences between the members of this MCU family.

2. Kit Contents

The C8051F560 Development Kit contains the following items:

- C8051F560 Target Board
- C8051Fxxx Development Kit Quick-Start Guide
- AC to DC Power Adapter
- USB Debug Adapter
- Two USB Cables

3. Hardware Setup

Refer to Figure 1 for a diagram of the hardware configuration.

1. Connect the USB Debug Adapter to the **DEBUG A** connector on the target board with the 10-pin ribbon cable.
2. Connect one end of the USB cable to the USB connector on the USB Debug Adapter.
3. Verify that shorting blocks are installed on the target board as shown in Figure 5 on page 7.
4. Connect the other end of the USB cable to a USB Port on the PC.
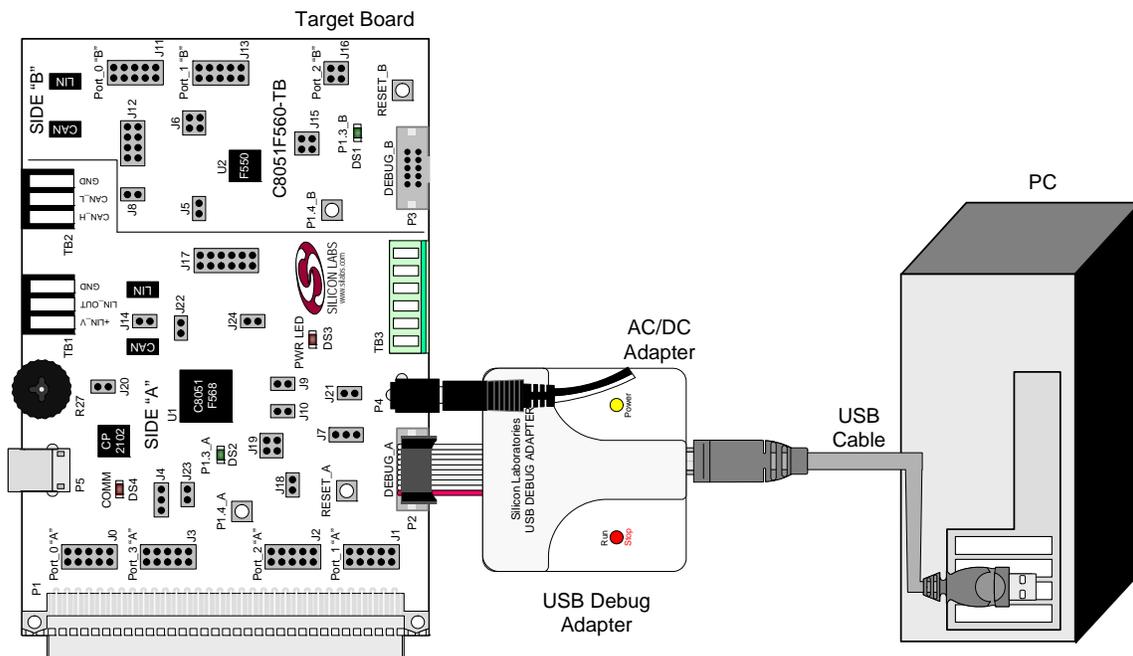5. Connect the ac/dc power adapter to power jack **P4** on the target board.

Figure 1. Hardware Setup using a USB Debug Adapter

Notes:
- Use the **Reset** icon in the IDE to reset the target when connected during a debug session.
- Remove power from the target board and the USB Debug Adapter before connecting or disconnecting the ribbon cable from the target board. Connecting or disconnecting the cable when the devices have power can damage the device and/or the USB Debug Adapter.

4. Software Setup

Simplicity Studio greatly reduces development time and complexity with Silicon Labs EFM32 and 8051 MCU products by providing a high-powered IDE, tools for hardware configuration, and links to helpful resources, all in one place.

Once Simplicity Studio is installed, the application itself can be used to install additional software and documentation components to aid in the development and evaluation process.
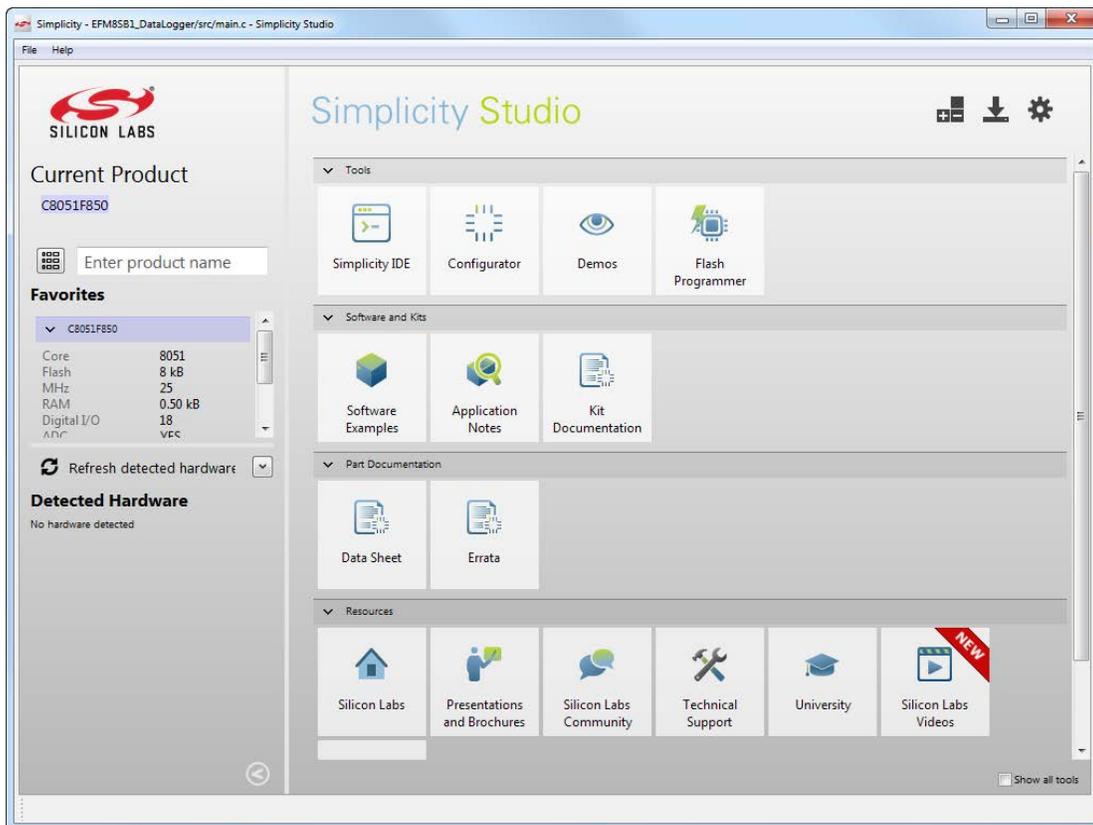
Figure 2. Simplicity Studio

The following Simplicity Studio components are required for the C8051F560 Development Kit:
- 8051 Products Part Support
- Simplicity Developer Platform

Download and install Simplicity Studio from www.silabs.com/8bit-software or www.silabs.com/simplicity-studio. Once installed, run Simplicity Studio by selecting **Start→Silicon Labs→Simplicity Studio→Simplicity Studio** from the start menu or clicking the **Simplicity Studio** shortcut on the desktop. Follow the instructions to install the software, and click **Simplicity IDE** to launch the IDE.

The first time the project creation wizard runs, the **Setup Environment** wizard will guide the user through the process of configuring the build tools and SDK selection.

In the **Part Selection** step of the wizard, select from the list of installed parts only the parts to use during

development. Choosing parts and families in this step affects the displayed or filtered parts in the later device selection menus. Choose the C8051F55x/56x/57x family by checking the **C8051F55x/56x/57x** check box. Modify the part selection at any time by accessing the **Part Management** dialog from the **Window**→**Preferences**→**Simplicity Studio**→**Part Management** menu item.

Simplicity Studio can detect if certain toolchains are not activated. If the **Licensing Helper** is displayed after completing the **Setup Environment** wizard, follow the instructions to activate the toolchain.

4.1. Running Blinky

Each project has its own source files, target configuration, SDK configuration, and build configurations such as the **Debug** and **Release** build configurations. The IDE can be used to manage multiple projects in a collection called a workspace. Workspace settings are applied globally to all projects within the workspace. This can include settings such as key bindings, window preferences, and code style and formatting options. Project actions, such as build and debug are context sensitive. For example, the user must select a project in the **Project Explorer** view in order to build that project.

To create a project based on the Blinky example:

1. Click the **Software Examples** tile from the Simplicity Studio home screen.
2. In the **Kit** drop-down, select **C8051F560 Development Kit**, in the **Part** drop-down, select **C8051F560**, and in the **SDK** drop-down, select the desired SDK. Click **Next**.
3. Select **Example** and click **Next**.
4. Under **C8051F560 Development Kit**, select **F55x-57x Blinky**, click **Next**, and click **Finish**.
5. Click on the project in the **Project Explorer** and click **Build**, the hammer icon in the top bar. Alternatively, go to **Project**→**Build Project**.
6. Click **Debug** to download the project to the hardware and start a debug session.
7. Press the **Resume** button to start the code running. The LED should blink.

8. Press the **Suspend** button to stop the code.

9. Press the **Reset the device** button to reset the target MCU.

10. Press the **Disconnect** button to return to the development perspective.

4.2. Simplicity Studio Help

Simplicity Studio includes detailed help information and device documentation within the tool. The help contains descriptions for each dialog window. To view the documentation for a dialog, click the question mark icon in the window:

This will open a pane specific to the dialog with additional details.

The documentation within the tool can also be viewed by going to **Help**→**Help Contents** or **Help**→**Search**.

4.3. CP210x USB to UART VCP Driver Installation

The Target Board includes a Silicon Labs CP210x USB-to-UART Bridge Controller. Device drivers for the CP210x need to be installed before the PC software can communicate with the MCU through the UART interface.

1. After opening Simplicity Studio for the first time, a dialog will prompt to install the CP210x drivers. Click **Yes**. The drivers can also be installed at any time by going to **Help→Install Drivers→CP210x VCP USB Drivers**.

2. Accept the license agreement and follow the steps to install the driver on the system. The installer will let you know when your system is up to date. The driver files included in this installation have been certified by Microsoft.

3. To complete the installation process, connect the included USB cable between the host computer and the USB connector (P5) on the Target Board. Windows will automatically finish the driver installation. Information windows will pop up from the taskbar to show the installation progress.

4. If needed, the driver files can be uninstalled by selecting **Windows Driver Package—Silicon Laboratories...** option in the **Programs and Features** window.

4.4. Configuration Wizard 2

The Configuration Wizard 2 is a code generation tool for all of the Silicon Labs devices. Code is generated through the use of dialog boxes for each of the device's peripherals.
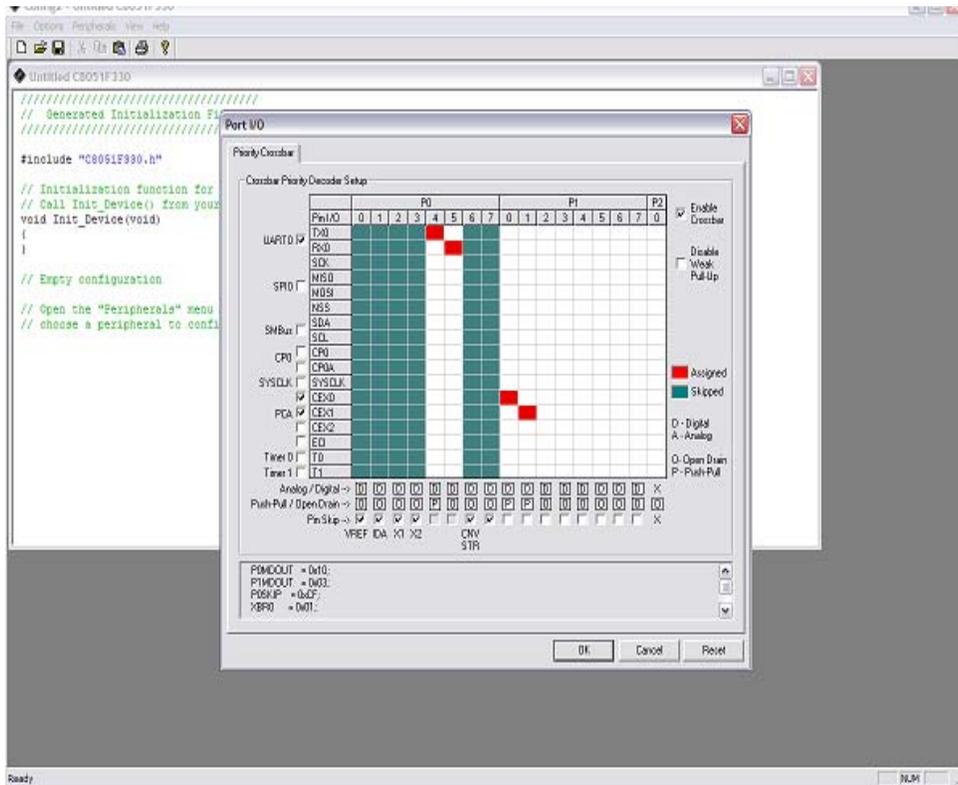

Figure 3. Configuration Wizard 2 Utility

The Configuration Wizard 2 utility helps accelerate development by automatically generating initialization source code to configure and enable the on-chip resources needed by most design projects. In just a few steps, the wizard creates complete startup code for a specific Silicon Labs MCU. The program is configurable to provide the output in C or assembly. For more information, please refer to the Configuration Wizard 2 help available under the **Help** menu in Configuration Wizard 2.

For more information, please refer to the Configuration Wizard 2 documentation. The documentation and software are available from the Downloads webpage (www.silabs.com/mcudownloads).

5. Target Board

The C8051F560 Development Kit includes a target board with a **C8051F568** (Side A) and **C8051F550** (Side B) device pre-installed for evaluation and preliminary software development. Numerous input/output (I/O) connections are provided to facilitate prototyping using the target board. Refer to Figure 4 for the locations of the various I/O connectors. Figure 5 on page 7 shows the factory default shorting block positions. A summary of the signal names and headers is provided in Table 12 on page 15.

J7	Header to choose between +5V from Debug Adapter (P2) or +5V from on-board regulator (U6)
J21	Connect V_HIGH node from TB1 LIN header to +5V regulator input for board power
P4	Power connector (accepts input from 7 to 15 VDC unregulated power adapter)
P5	USB connector (connects to PC for serial communication)
TB1	Shared LIN Connector for Side A and B MCUs for external nodes
TB2	Shared CAN Connector for Side A and B MCUs for external nodes
J0-J3	Side A: Port 0 through Port 3 headers
J4	Side A: Connects +5V net or +3.3V net to VIO of the MCU
J9, J10	Side A: External crystal enable connectors
J14	Side A: CAN Transceiver (U3) power connector
J17	Side A: Connects MCU to three separate transceivers (UART(U5), CAN(U3), and LIN(T1))
J18	Side A: Connects VIO to VIO_A_SRC which powers the R27 potentiometer, the RST_A pin pull-up, and P1.4_A Switch pull-up.
J19	Side A: Connects P1.3_A LED and P1.4_A Switch to MCU port pins
J20	Side A: Connects R27 potentiometer to port pin 1.2
J22	Side A: Connects decoupling capacitors C28 and C29 for MCU VREF (P0.0)
J23	Side A: Connects VIO_A power to External Memory Interface Latch (U8)
J24	Side A: Connects +5V net to VIO and VREGIN of the MCU
P1	Side A: 96-pin female connector
P2	Side A: DEBUG connector for Debug Adapter interface
TB3	Side A: Power supply terminal block
J5	Side B: Connects decoupling capacitors C42 and C43 for MCU VREF (P0.0)
J6	Side B: Connects +5V net to VIO and VREGIN of the MCU
J8	Side B: CAN Transceiver (U4) power connector
J11	Side B: Port 0 header
J12	Side B: Connects MCU to two separate transceivers (CAN (U4) and LIN (T2))
J13	Side B: Port 1 header
J15	Side B: Connects P1.3_B LED and P1.4_B Switch to MCU port pins
J16	Side B: Port 2 header
P3	Side B: DEBUG connector for Debug Adapter interface

Figure 4. C8051F560 Target Board with Pin Numbers

5.1. Target Board Shorting Blocks: Factory Defaults

The C8051F560 Target Board comes from the factory with pre-installed shorting blocks on many headers. Figure 5 shows the positions of the factory default shorting blocks.

Figure 5. C8051F560 Target Board Shorting Blocks: Factory Defaults

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5.2. Target Board Power Options and Current Measurement (J4, J6, J7, J24, P4, TB1)

The MCUs on the C8051F560 Target Board are powered from a +5 V net. The +5 V net is connected to the headers J4 and J24 (Side A) and J6 (Side B). Shorting blocks can be put on each header to connect the 5V net to the VREGIN and VIO pins on the two MCUs. With the shorting blocks removed, a source meter can be used across the headers to measure the current consumption of the MCU.

The +5 V net on the target board has three possible sources:

1. 12V dc power using the ac to dc power adapter (P4)
2. 5V dc USB VBUS power from PC via the USB Debug Adapter (DEBUG_A)
3. 12V dc power from the LIN external header (TB1)

5.2.1. Using the AC to DC Power Adapter as the Target Board Power Source (P4, J7)

The default configuration of the target board uses the ac to dc power adapter as the source. The 12 V from the adapter is regulated to +5 V using an LDO regulator (U6). The output of the regulator is connected to the +5 V net of the target board through the J7 header. A shorting block should be installed on pins J7[2-3] for this purpose. The +5V net powers the MCUs directly.

5.2.2. Using the USB Debug Adapter as the Target Board Power Source (J7)

The target board can use +5 V provided by the USB Debug Adapter. To enable this source, a shorting block should be installed on pins J7[1-2]. With this shorting block, the output of the LDO regulator (U6) is disconnected from the +5 V net of the target board, and the SER_PWR node is connected to +5 V.

Note: The USB Debug Adapter does not provide the necessary peak power for the CAN transceivers to operate. One of the 12 V dc sources is recommended for CAN transceiver operation.

5.2.3. Using an External +12V LIN Source as the Target Board Power Source (J7, TB1)

The two 12V power sources (LIN and ac to dc power adapter) are ORed together using reverse-biased diodes (Z1 and Z2) and connected to the input of the LDO regulator (U6). The output of the regulator is connected to the +5 V net of the target board through the J7 header. A shorting block should be installed on pins J7[2-3] for this purpose. The +5V net powers the MCUs directly.

5.3. System Clock Sources (J9, J10)

5.3.1. Internal Oscillators

The C8051F568 and C8051F550 devices installed on the target board feature a factory-calibrated, programmable high-frequency internal oscillator (24 MHz base frequency, ±0.5%), which is enabled as the system clock source on reset. After reset, the internal oscillator operates at a frequency of 187.5 kHz by default but may be configured by software to operate at other frequencies. The on-chip crystal is accurate for CAN and LIN master communications and in many applications an external oscillator is not required. However, if you wish to operate the C8051F568 device (Side A) at a frequency not available with the internal oscillator, an external crystal may be used. Refer to the C8051F55x/56x/57x data sheet for more information on configuring the system clock source.

5.3.2. External Oscillator Options

The target board is designed to facilitate the installation of an external crystal. Remove shorting blocks at headers J9 and J10 and install the crystal at the pads marked Y1. Install a 10 MΩ resistor at R2 and install capacitors at C6 and C7 using values appropriate for the crystal you select. If you wish to operate the external oscillator in capacitor or RC mode, options to install a capacitor or an RC network are also available on the target board. R2, R3, C6, and C7 are located on the back side of the board, near the Side A MCU. Populate C6 for capacitor mode, and populate R3 and C6 for RC mode. Refer to the C8051F55x/56x/57x data sheet for more information on the use of external oscillators.

5.4. Switches and LEDs (J15, J19)

Two push-button switches are provided on the target board for each MCU. Switch RESET_A is connected to the RST pin of the C8051F568. Switch RESET_B is connected to the RST pin of the C8051F550. Pressing RESET_A puts the C8051F568 device into its hardware-reset state, and similarly for RESET_B and the C8051F550 MCU. Switches P1.4_A and P1.4_B are connected to the MCU's general purpose I/O (GPIO) pins through headers. Pressing either one of these switches generates a logic low signal on the port pin. Remove the shorting block from the header to disconnect these switches from the port pins. See Table 1 for the port pins and headers corresponding to each switch.

Four LEDs are provided on the target board to serve as indicators. The red LED labeled PWR LED indicates presence of power to the target board. The second red LED labeled COMM indicates if the CP2102 USB-to-UART bridge is recognized by the PC. The green LED on Side A is labeled with a port pin name and is connected to a C8051F568 GPIO pin through a header. Remove the shorting block from the header to disconnect the LED from the port pin. Similarly, a second green LED on Side B is connected to the C8051F550 through another header. See Table 1 for the port pins and headers corresponding to each LED.

Table 1. Target Board I/O Descriptions

Description	I/O	Header(s)
RESET_A	Reset (Side A)	none
RESET_B	Reset (Side B)	none
P1.4_A Switch	P1.4 (Side A)	J19[1–2]
P1.4_B Switch	P1.4 (Side B)	J15[1–2]
P1.3_A LED	P1.3 (Side A)	J19[3–4]
P1.3_B LED	P1.3 (Side B)	J15[3–4]
Red LED (PWR)	Power	none
Red LED (COMM)	COMM Active	none

5.5. Target Board Debug Interfaces (P2 and P3)

The debug connectors P2 (DEBUG_A) and P3 (DEBUG_B) provide access to the debug (C2) pins of the C8051F568 and C8051F550. The debug connectors are used to connect the Serial Adapter or the USB Debug Adapter to the target board for in-circuit debugging and Flash programming. Table 2 shows the DEBUG pin definitions.

Table 2. DEBUG Connector Pin Descriptions

Side A - C8051F568		Side B - C8051F550	
Pin #	**Description**	**Pin #**	**Description**
1	Not Connected	1	Not Connected
2, 3, 9	GND (Ground)	2, 3, 9	GND (Ground)
4	P4.0_C2D_A	4	P2.1_C2D_B
5	RST_A (Reset)	5	RST_B (Reset)
6	P4.0_A	6	P2.1_B
7	RST/C2CK_A	7	RST/C2CK_B
8	Not Connected	8	Not Connected
10	USB Power (+5VDC from P2)	10	Not Connected

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5.6. Serial Interface (P5, J17)

A USB-to-UART bridge circuit (U5) and USB connector (P5) are provided on the target board to facilitate serial connections to UART0 of the C8051F568 (Side A). The Silicon Labs CP2102 USB-to-UART bridge provides data connectivity between the C8051F568 and the PC via a USB port. The TX and RX signals of UART0 may be connected to the CP2102 by installing shorting blocks on header J17. The shorting block positions for connecting each of these signals to the CP2102 are listed in Table 3. To use this interface, the USB-to-UART device drivers should be installed as described in Section C8051F560.

Table 3. Serial Interface Header (J17) Description

Header Pins	UART0 Pin Description
J17[3–4]	UART_TX (P0.4_A)
J17[1–2]	UART_RX (P0.5_A)

5.7. CAN Interface and Network (J8, J12, J14, J17, TB2)

Both MCUs on the target board are connected to CAN transceivers (U3, U4) through headers. The port pins assigned to the CAN peripheral on each MCU are P0.6 (CAN_TX) and P0.7 (CAN_RX). The C8051F568 (Side A) is connected to U3 through the J17 header and the C8051F550 (Side B) is connected to U4 through the J12 header. The two CAN transceivers are connected to each other and form a CAN network. Other external devices can be connected to the CAN network through the TB2 interface. The shorting block positions for connecting the MCUs to the CAN transceivers are listed in Table 4. The pin connections for the external CAN devices are listed in Table 5. The CAN transceivers are powered by the +5VREG node and connected through J8 and J14 headers.

Table 4. CAN Interface Headers (J17 and J12) Description

Header Pins	CAN0 Pin Description
J17[5–6]	CAN_TX (P0.6_A)
J17[7–8]	CAN_RX (P0.7_A)
J12[7–8]	CAN_TX (P0.6_B)
J12[5–6]	CAN_RX (P0.7_B)

Table 5. TB2 External CAN Interface Header Description

Pin #	Pin Description
1	GND
2	CAN_L
3	CAN_H

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5.8. LIN Interface and Network (J12, J17, J21, TB1)

Both MCUs on the target board are connected to LIN transceivers through headers. These headers assume that the MCU's crossbars are configured to put the LIN TX and RX pins on port pins P1.0 and P1.1 respectively. See the C8051F55x/56x/57x data sheet for crossbar configuration. The C8051F568 (Side A) is connected to the T1 transceiver through the J17 header and the C8051F550 (Side B) is connected to the T2 transceiver through the J12 header. The two LIN transceivers are connected to each other and form a LIN network. Other external devices can be connected to the LIN network through the TB1 interface. The TB1 interface also provides the option for connecting an external power source so that all LIN transceivers can use the same source voltage. This source voltage can also be used to power the target board. If an external voltage source is not provided, the LIN transceivers use the 12V provided through the P4 power adapter connector. See Section 5.2. for more power option details. The shorting block positions for connecting the MCUs to the LIN transceivers are listed in Table 6. The pin connections for the external LIN devices are listed in Table 7.

Table 6. LIN Interface Headers (J12 and J17) Description

Header Pins	LIN0 Pin Description
J17[9–10]	LIN_TX (P1.0_A)
J17[11–12]	LIN_RX (P1.1_A)
J12[3–4]	LIN_TX (P1.0_B)
J12[1–2]	LIN_RX (P1.1_B)

Table 7. TB1 External LIN Interface Header Description

Pin #	Pin Description
1	GND
2	LIN_OUT
3	+LIN_V

Header J21 connects the P4 power-adapter supply to the V_HIGH node, which is used as the power source for the LIN transceivers (T1, T2). The shorting block on header J21 can be removed to force the LIN transceivers to use the voltage supply externally supplied on the +LIN_V pin on the TB1 header.

5.9. Port I/O Connectors (J0-J3 and J11, J13, J16)

Each of the parallel ports of the C8051F568 (Side A) and C8051F550 (Side B) has its own 10-pin header connector. Each connector provides a pin for the corresponding port pins 0-7, +5 V VIO, and digital ground. The same pin-out is used for all of the port connectors.

Table 8. Port I/O Connector Pin Description (J0-J3, J11, J13)

Pin #	Pin Description
1	Pn.0
2	Pn.1
3	Pn.2
4	Pn.3
5	Pn.4
6	Pn.5
7	Pn.6
8	Pn.7
9	+5V (VIO)
10	GND (Ground)

Port 2 on the C8051F550 (Side B) MCU has only two pins and has a reduced header.

Table 9. Port I/O Connector Pin Description (J16)

Pin #	Pin Description
1	Pn.0
2	Pn.1
3	+5V (VIO)
4	GND (Ground)

5.10. Voltage Reference (VREF) Connectors (J5 and J22)

The VREF connectors can be used to connect the VREF pin from the MCU (P0.0) to external 0.1 µF and 4.7 µF decoupling capacitors. The C8051F568 (Side A) device is connected to the capacitors through the J22 header and the C8051F550 (Side B) device connects to its own set of capacitors through J5.

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5.11. Expansion Connector (P1)

The 96-pin expansion I/O connector P1 is used to connect daughter boards to the main target board. P1 provides access to many C8051F568 signal pins. Pins for VREGIN, VDD, VIO, and 3.3V are also available. See Table 10 for a complete list of pins available at P1.

The P1 socket connector is manufactured by Hirose Electronic Co. Ltd, part number PCN13-96S-2.54DS, Digi-Key part number H7096-ND. The corresponding plug connector is also manufactured by Hirose Electronic Co. Ltd, part number PCN10-96P-2.54DS, Digi-Key part number H5096-ND.

Table 10. P1 Pin Listing

Pin #	Description	Pin #	Description	Pin #	Description
A-1	+3.3V	B-1	GND	C-1	N/C
A-2	N/C	B-2	N/C	C-2	N/C
A-3	N/C	B-3	N/C	C-3	N/C
A-4	N/C	B-4	N/C	C-4	N/C
A-5	N/C	B-5	N/C	C-5	N/C
A-6	N/C	B-6	N/C	C-6	N/C
A-7	N/C	B-7	N/C	C-7	N/C
A-8	N/C	B-8	N/C	C-8	N/C
A-9	N/C	B-9	N/C	C-9	N/C
A-10	N/C	B-10	P0.7_A	C-10	P0.6_A
A-11	P0.5_A	B-11	P0.4_A	C-11	P_0.3_A
A-12	P_0.2_A	B-12	P0.1_A	C-12	P0.0_A
A-13	P3.7_A	B-13	P3.6_A	C-13	P3.5_A
A-14	P3.4_A	B-14	P3.3_A	C-14	P3.2_A
A-15	P3.1_A	B-15	P3.0_A	C-15	P3.7_A_L
A-16	P3.6_A_L	B-16	P3.5_A_L	C-16	P3.4_A_L
A-17	P3.3_A_L	B-17	P3.2_A_L	C-17	P3.1_A_L
A-18	P3.0_A_L	B-18	P2.7_A	C-18	P2.6_A
A-19	P2.5_A	B-19	P2.4_A	C-19	P2.3_A
A-20	P2.2_A	B-20	P2.1_A	C-20	P2.0_A
A-21	P1.7_A	B-21	P1.6_A	C-21	P1.4_A
A-22	P1.2_A	B-22	P1.3_A	C-22	P1.5_A
A-23	P1.1_A	B-23	P1.0_A	C-23	N/C
A-24	P4.0_C2D_A	B-24	N/C	C-24	N/C
A-25	$\overline{\text{RST\_A}}$	B-25	GND	C-25	N/C
A-26	GND	B-26	N/C	C-26	N/C
A-27	N/C	B-27	N/C	C-27	N/C
A-28	N/C	B-28	N/C	C-28	N/C
A-29	VIO_A	B-29	VDD_A	C-29	VREGIN_A
A-30	N/C	B-30	N/C	C-30	N/C
A-31	N/C	B-31	N/C	C-31	N/C
A-32	N/C	B-32	AGND	C-32	N/C

The Silicon Labs add-on boards designed to interface to the 96-pin interface are primarily designed to operate at 3.3 V and to use a non-multiplexed external memory interface. When interfacing to a +3.3 V add-on board, it is recommended to put the shorting block on J4[2-3] to connect VIO of the C8051F568 to +3.3 V instead of the default +5 V. The C8051F560 target board also includes an 8-bit latch (U8) for use with the multiplexed mode of the

external memory interface. The output pins of the latch are connected to the 96-pin header and include an _L suffix in the pin name.

5.12. Potentiometer (J20)

The C8051F568 (Side A) device has the option to connect port pin P1.2 to a 10K linear potentiometer (R27). The potentiometer is connected through the J20 header. The potentiometer can be used for testing the analog-to-digital (ADC) converter of the MCU.

5.13. Power Supply I/O (Side A) (TB3)

All of the C8051F568 target device's supply pins are connected to the TB3 terminal block. Refer to Table 11 for the TB3 terminal block connections.

Table 11. TB3 Terminal Block Pin Descriptions

Pin #	Description
1	VIO_A
2	VREGIN_A
3	VDD_A
4	VDDA_A
5	GNDA_A
6	GND

5.14. Alternate Power Supply Headers (J18, J21)

The C8051F560 Target Board includes two headers that allow for alternate power sources and power measurement. Header J18 connects the VIO voltage supplied to the Side A MCU to other peripherals on the board, such as the P1.4_A push-button switch pull-up, and the R27 potentiometer source. To enable current measurement, the shorting block on J18 can be removed so that the VIO_A node only powers the VIO pin on the MCU. Another voltage source will need to be applied to the VIO_SRC node to power the other peripherals.

5.15. C2 Pin Sharing

On the C8051F568 (Side A) and the C8051F550 (Side B), the debug pins C2CK and C2D are shared with the pins RST and P4.0/P2.1 respectively. The target board includes the resistors necessary to enable pin sharing which allow the pin–shared pins to be used normally while simultaneously debugging the device. See Application Note "AN124: Pin Sharing Techniques for the C2 Interface" at www.silabs.com for more information regarding pin sharing.

5.16. Target Board Pin Assignment Summary

Some GPIO pins of the C8051F568 MCU can have an alternate fixed function. For example, pin 38 on the C8051F568 MCU is designated P0.4, and can be used as a GPIO pin. Also, if the UART0 peripheral on the MCU is enabled using the crossbar registers, the TX signal is routed to this pin. This is shown in the "Alternate Fixed Function" column. The "Target Board Function" column shows that this pin is used as TX on the C8051F560 Target Board. The "Relevant Headers" column shows that this signal is routed to pin 3 of the J17 header and pin 5 of the J1 header. More details can be found in the C8051F55x/56x/57x data sheet. Some of the GPIO pins of the C8051F568 have been used for various functions on the target board. All pins of the Side A MCU also connect to the 96-pin (P1) expansion connector which is not explicitly listed below. Table 12 summarizes the C8051F568 MCU pin assignments on the target board, and also shows the various headers associated with each signal.

Table 12. C8051F560 Target Board Pin Assignments and Headers

MCU Pin Name	Pin#	Primary Function	Alternate Fixed Function	Target Board Function	Relevant Headers
P0.0	8	P0.0	VREF	VREF	J0[1], J22[1]
P0.1	1	P0.1	CNVSTR	CNVSTR	J0[2]
P0.2	40	P0.2	XTAL1	XTAL1	J0[3]*, J9[2]
P0.3	39	P0.3	XTAL2	XTAL2	J0[4]*, J10[2]
P0.4	38	P0.4	UART_TX	TX_MCU	J0[5], J17[3]
P0.5	37	P0.5	UART_RX	RX_MCU	J0[6], J17[1]
P0.6	36	P0.6	CAN_TX	CAN_TX	J0[7], J17[5]
P0.7	35	P0.7	CAN_RX	CAN_RX	J0[8], J17[7]
P1.0	34	P1.0		LIN_TX	J1[1], J17[9]
P1.1	33	P1.1		LIN_RX	J1[2], J17[11]
P1.2	32	P1.2		POTENTIOMETER	J1[3], J20[1]
P1.3	31	P1.3		LED	J1[4], J19[4]
P1.4	30	P1.4		SWITCH	J1[5], J19[2]
P1.5	29	P1.5	ALE (U8)	GPIO	J1[6]
P1.6	28	P1.6		GPIO	J1[7]
P1.7	27	P1.7		GPIO	J18
P2.0	26	P2.0		GPIO	J2[1]
P2.1	25	P2.1		GPIO	J2[2]
P2.2	24	P2.2		GPIO	J2[3]
P2.3	23	P2.3		GPIO	J2[4]
P2.4	22	P2.4		GPIO	J2[5]
P2.5	21	P2.5		GPIO	J2[6]
P2.6	20	P2.6		GPIO	J2[7]
P2.7	19	P2.7		GPIO	J2[8]
P3.0	18	P3.0		GPIO	J3[1]

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Table 12. C8051F560 Target Board Pin Assignments and Headers (Continued)

MCU Pin Name	Pin#	Primary Function	Alternate Fixed Function	Target Board Function	Relevant Headers
P3.1	17	P3.1		GPIO	J3[2]
P3.2	16	P3.2		GPIO	J3[3]
P3.3	15	P3.3		GPIO	J3[4]
P3.4	14	P3.4		GPIO	J3[5]
P3.5	13	P3.5		GPIO	J3[6]
P3.6	12	P3.6		GPIO	J3[7]
P3.7	11	P3.7		GPIO	J3[8]
P4.0_C2D	9	C2D	P4.0	GPIO	P2[4], P2[6]*
$\overline{\text{RST}}$/C2CK	10	$\overline{\text{RST}}$	C2CK	$\overline{\text{RST}}$/C2CK	P2[7], P2[5]*
VIO	2	VIO		VIO	J4[2], J18[1], TB3[1] J0-J3[9]*, J23
VREGIN	3	VREGIN		VREGIN	J24[2], TB3[2]
VDD	4	VDD		VDD	TB3[3]
VDDA	5	VDDA		VDDA	TB3[4]
GND	6	GND		GND	J0-J3[10], TB3[6]
GNDA	7	GNDA		GNDA	TB3[5]

*Note: Headers denoted by this symbol are not directly connected to the MCU pin; the connection might be via one or more headers and/or pin-sharing resistor(s). See board schematic for details.

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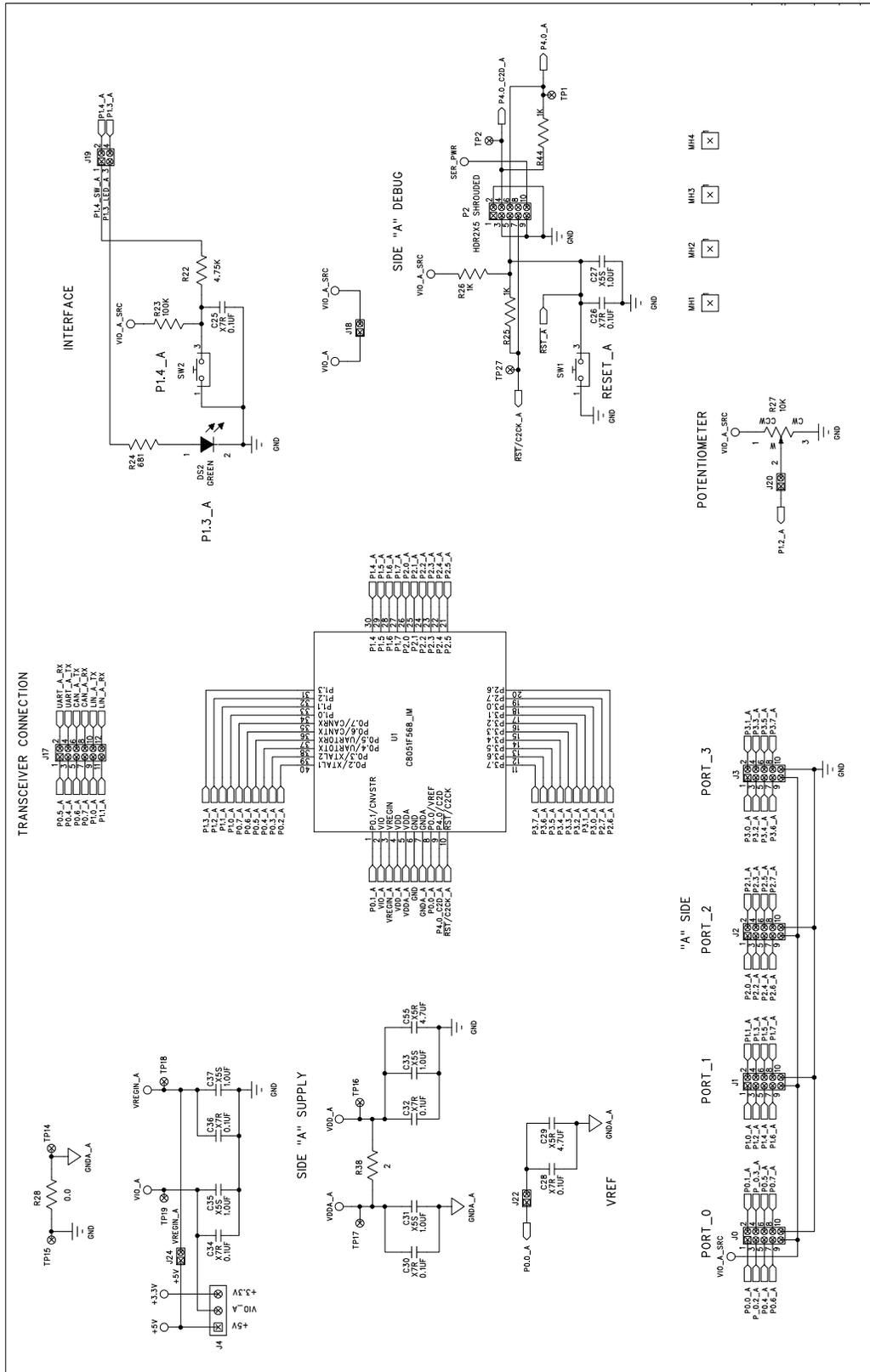
6. Schematics

Figure 6. C8051F560 Target Board Schematic (Page 1 of 4)
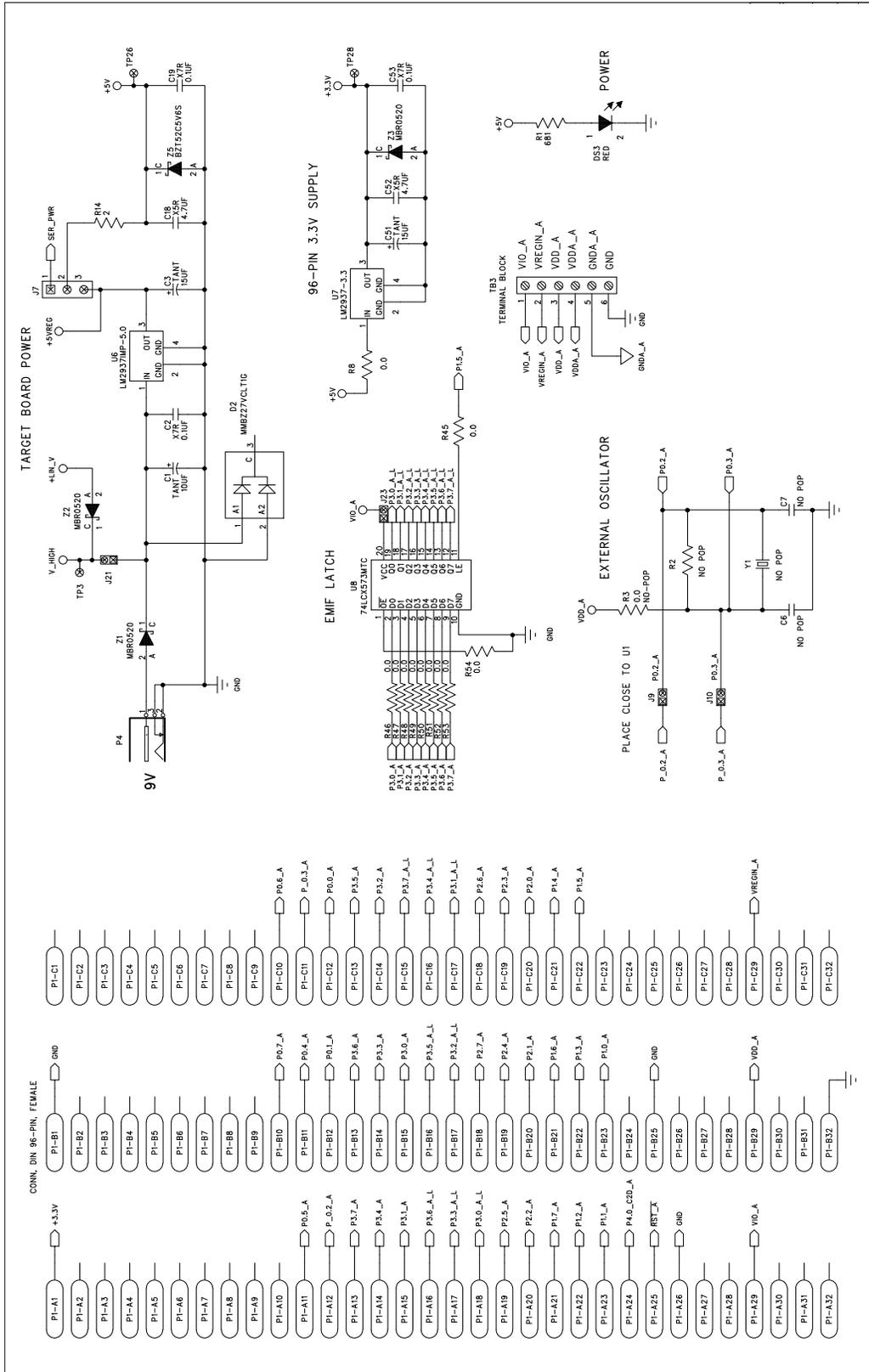
Figure 7. C8051F560 Target Board Schematic (Page 2 of 4)

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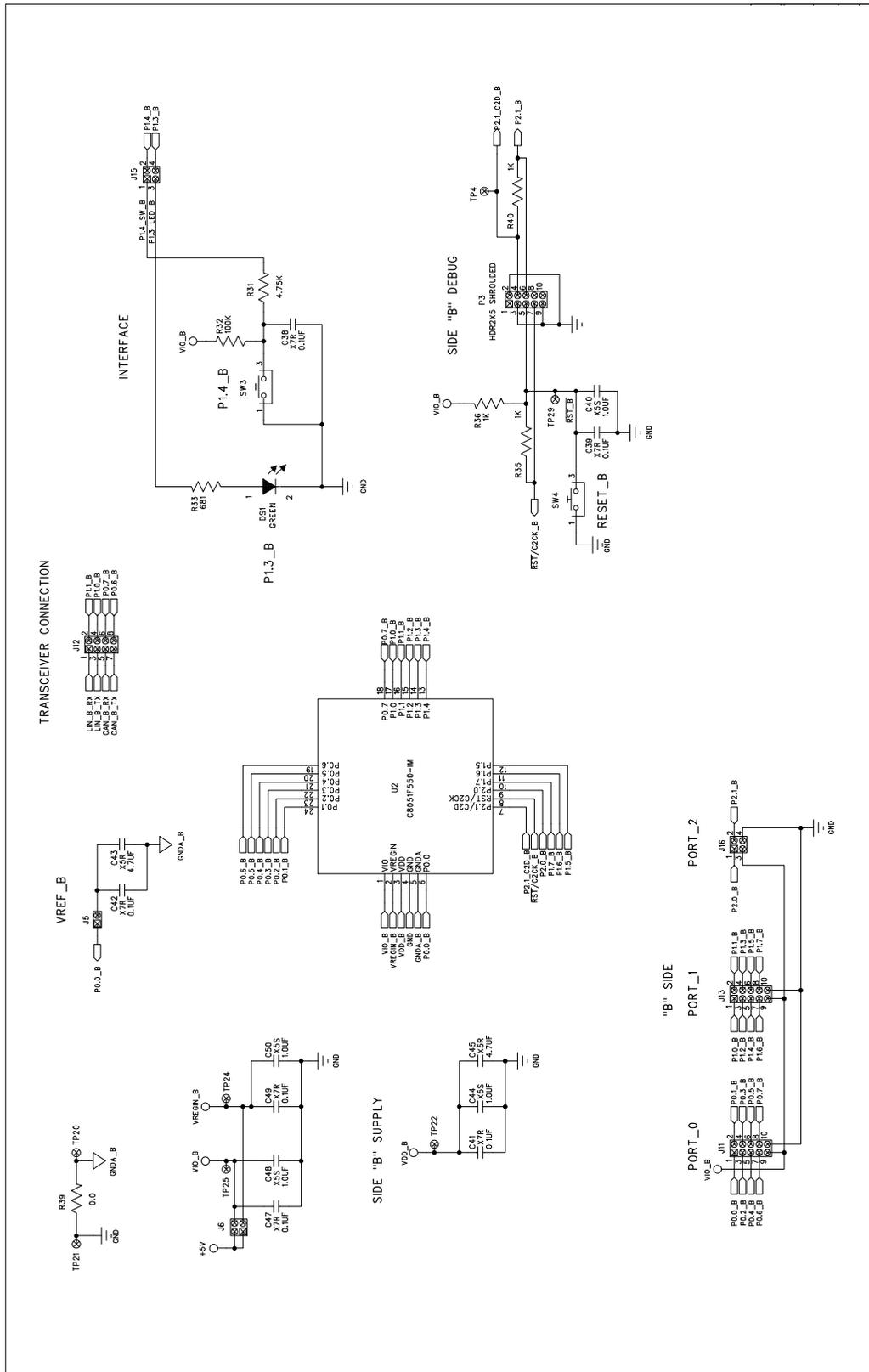
Figure 8. C8051F560 Target Board Schematic (Page 3 of 4)
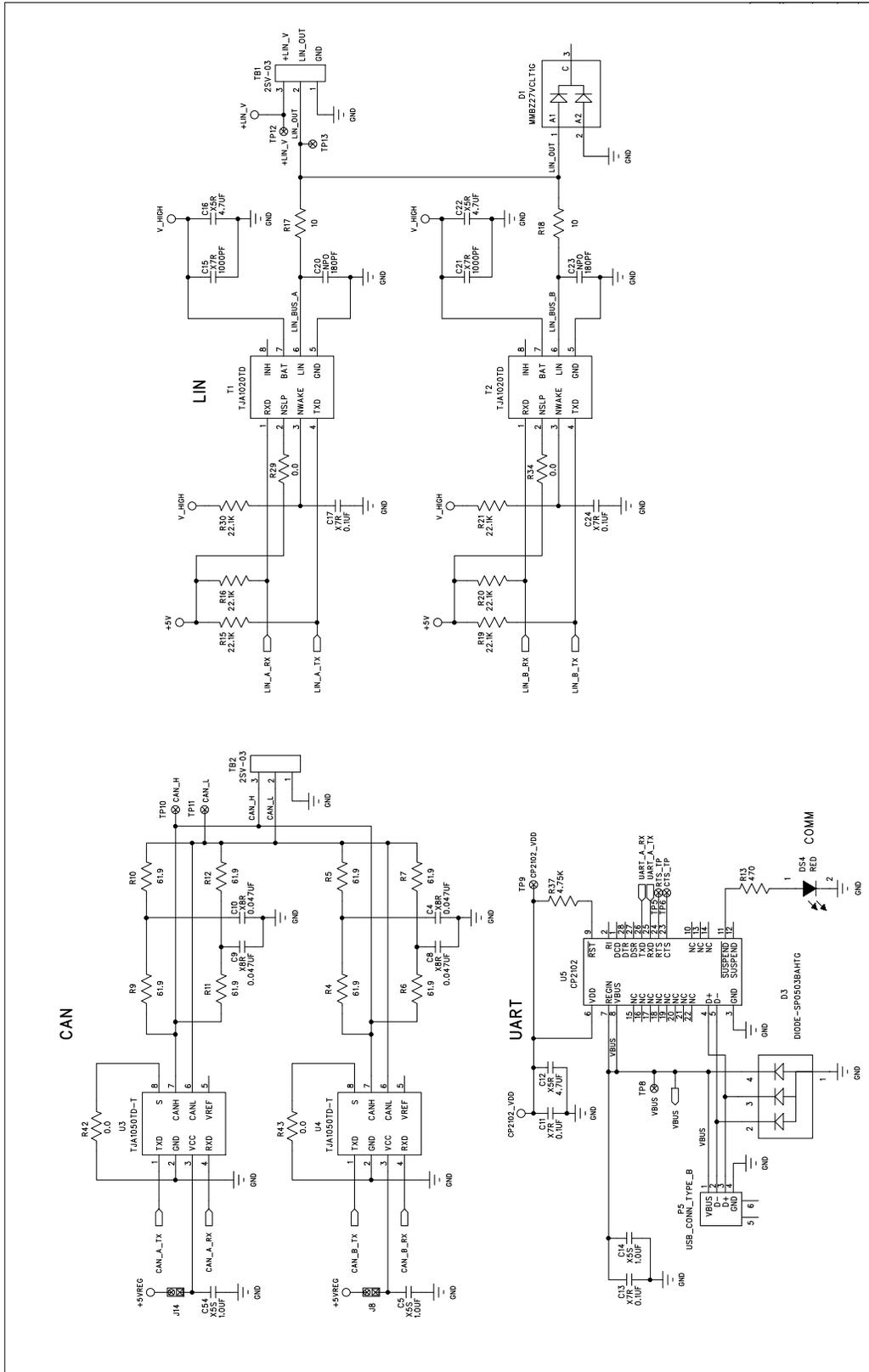
Figure 9. C8051F560 Target Board Schematic (Page 4 of 4)

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DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

Updated 4. "Software Setup," on page 2.
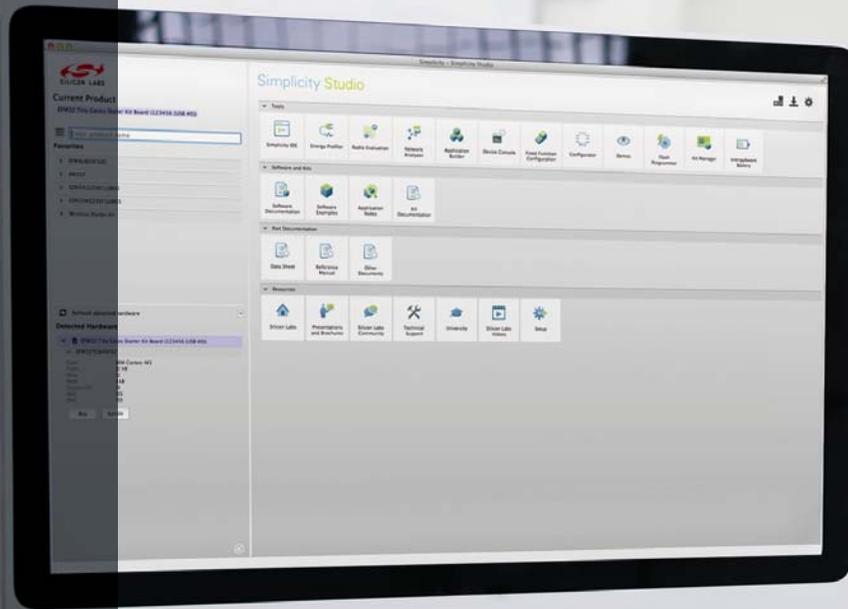
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