C8051F930-GDI

Tested Single/Dual Battery, 0.9–3.6 V, 64 kB Flash, SmaRTClock, 10-Bit ADC MCU Die in Wafer Form

Supply Voltage 0.9 to 3.6 V
- One-Cell Mode supports 0.9 to 1.8 V operation
- Two-Cell Mode supports 1.8 to 3.6 V operation
- Built-in dc-dc converter with 1.8 to 3.3 V output for use in one-cell mode
- Built-in LDO regulator allows a high analog supply voltage and low digital core voltage
- 2 built-in supply monitors (brownout detectors)

10-Bit Analog to Digital Converter
- 1LSB INL; no missing codes
- Programmable throughput up to 300 ksps
- 23 external inputs
- On-Chip Voltage Reference
- On-Chip PGA allows measuring voltages up to twice the reference voltage
- 16-bit Auto-Averaging Accumulator with Burst Mode provides increased ADC resolution
- Data dependent windowed interrupt generator
- Built-in temperature sensor

Two Comparators
- Programmable hysteresis and response time
- Configurable as wake-up or reset source
- 23 Capacitive Touch Sense inputs

6-Bit Programmable Current Reference
- Up to ± 500 µA. Can be used as a bias or for generating a custom reference voltage

On-Chip Debug
- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 to 2 system clocks
- 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

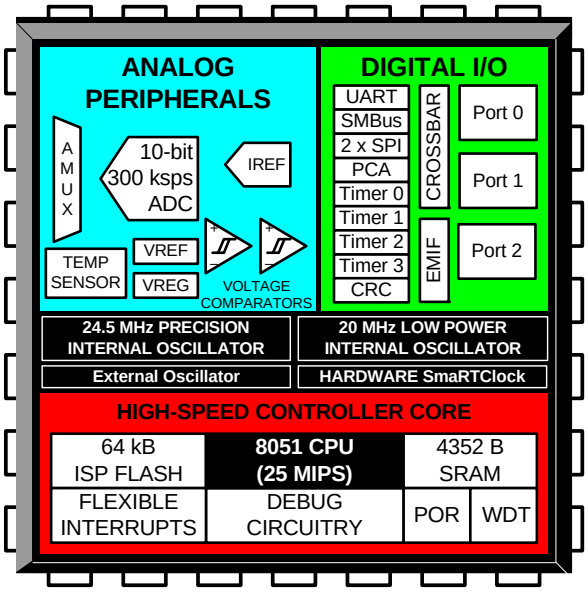
Memory
- 4352 bytes internal data RAM (256+4096)
- 64 kB Flash; In-system programmable in 1024-byte sectors--1024 bytes are reserved in the 64 kB devices

Digital Peripherals
- 24 port I/O; All 5 V tolerant with high sink current and programmable drive strength
- Hardware SMBus™ (I²C Compatible), 2 x SPI™, and UART serial ports available concurrently
- Four general purpose 16-bit counter/timer array with six capture/compare modules and watchdog timer
- Hardware SmaRTClock operates down to 0.9V and requires less than 0.5 µA supply current

Clock Sources
- Internal oscillators: 24.5 MHz, 2% accuracy supports UART operation; 20 MHz low power oscillator requires very little bias current
- External oscillator: Crystal, RC, C, or CMOS Clock
- SmaRT Clock oscillator: 32 kHz Crystal or internal self-oscillate mode
- Can switch between clock sources on-the-fly; useful in implementing various power saving modes

Temperature range: –40 to +85 °C

Full Technical Data Sheet
- C8051F93x-C8051F92x



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1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (Bytes)	SmaRTClock Real Time Clock	SMBus/I^2C	UART	Enhanced SPI	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 300ksps ADC	Programmable Current Reference	Internal Voltage Reference	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Wafer Thickness
C8051F930-G-G1DI	25	64	4352	✓	1	1	2	4	✓	24	✓	✓	✓	✓	2	✓	28.54 mil / 725 µm (no back-grind)
C8051F930-G-GDI	25	64	4352	✓	1	1	2	4	✓	24	✓	✓	✓	✓	2	✓	12 mil (backgrind)
***Note:** 1024 bytes reserved for factory use.																	

2. Pin Definitions

Table 2.1. Pin Definitions for the C8051F930-GDI

Name	Physical Pad Number	Type	Description
VBAT	6	P In	Battery Supply Voltage. Must be 0.9 to 1.8 V in single-cell battery mode and 1.8 to 3.6 V in dual-cell battery mode.
V_{DD} /	4	P In	Power Supply Voltage. Must be 1.8 to 3.6 V. This supply voltage is not required in low power sleep mode. This voltage must always be ≥ VBAT.
DC+		P Out	Positive output of the dc-dc converter. In single-cell battery mode, a 1uF ceramic capacitor is required between DC+ and DC–. This pin can supply power to external devices when operating in single-cell battery mode.
DC– /	2	P In	DC-DC converter return current path. In single-cell battery mode, this pin is typically not connected to ground.
GND		G	In dual-cell battery mode, this pin must be connected directly to ground.
GND	3	G	Required Ground.
DCEN	5	P In	DC-DC Enable Pin. In single-cell battery mode, this pin must be connected to VBAT through a 0.68 µH inductor.
		G	In dual-cell battery mode, this pin must be connected directly to ground.
$\overline{\text{RST}}$/	7	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. A 1 kΩ to 5 kΩ pullup to V_{DD} is recommended. See Reset Sources section of the C8051F93x-C8051F92x data sheet for a complete description.
C2CK		D I/O	Clock signal for the C2 Debug Interface.
P2.7/	8	D I/O	Port 2.7. This pin can only be used as GPIO. The Crossbar cannot route signals to this pin and it cannot be configured as an analog input. See Port I/O section the C8051F93x-C8051F92x data sheet for a complete description.
C2D		D I/O	Bi-directional data signal for the C2 Debug Interface.
XTAL3	11	A In	SmaRTClock Oscillator Crystal Input.
XTAL4	10	A Out	SmaRTClock Oscillator Crystal Output.

Table 2.1. Pin Definitions for the C8051F930-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.0	39	D I/O or A In	Port 0.0. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
V_{REF}		A In A Out	External V_{REF} Input. Internal V_{REF} Output. External V_{REF} decoupling capacitors are recommended. See ADC0 section of the C8051F93x-C8051F92x data sheet for details.
P0.1	38	D I/O or A In	Port 0.1. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
AGND		G	Optional Analog Ground. See ADC0 section of the C8051F93x-C8051F92x data sheet for details.
P0.2	33	D I/O or A In	Port 0.2. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
XTAL1		A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator. See Oscillator section of the C8051F93x-C8051F92x data sheet for a complete description.
P0.3	32	D I/O or A In	Port 0.3. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
XTAL2		A Out	External Clock Output. This pin is the excitation driver for an external crystal or resonator.
		D In	External Clock Input. This pin is the external clock input in external CMOS clock mode.
		A In	External Clock Input. This pin is the external clock input in capacitor or RC oscillator configurations. See Oscillator section of the C8051F93x-C8051F92x data sheet for complete details.
P0.4	31	D I/O or A In	Port 0.4. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
TX		D Out	UART TX Pin. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.

Table 2.1. Pin Definitions for the C8051F930-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.5	30	D I/O or A In	Port 0.5. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
RX		D In	UART RX Pin. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
P0.6	29	D I/O or A In	Port 0.6. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
CNVSTR		D In	External Convert Start Input for ADC0. See ADC0 section of the C8051F93x-C8051F92x data sheet for a complete description.
P0.7	28	D I/O or A In	Port 0.7. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
IREF0		A Out	IREF0 Output. See IREF section of the C8051F93x-C8051F92x data sheet for complete description.
P1.0	27	D I/O or A In	Port 1.0. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. May also be used as SCK for SPI1.
AD0		D I/O	Address/Data 0.
P1.1	26	D I/O or A In	Port 1.1. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. May also be used as MISO for SPI1.
AD1		D I/O	Address/Data 1.
P1.2	25	D I/O or A In	Port 1.2. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. May also be used as MOSI for SPI1.
AD2		D I/O	Address/Data 2.
P1.3	24	D I/O or A In	Port 1.3. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. May also be used as NSS for SPI1.
AD3		D I/O	Address/Data 3.
P1.4	21	D I/O or A In	Port 1.4. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description.
AD4		D I/O	Address/Data 4.

Table 2.1. Pin Definitions for the C8051F930-GDI (Continued)

Name	Physical Pad Number	Type	Description
P1.5 AD5	20	D I/O or A In D I/O	Port 1.5. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address/Data 5.
P1.6 AD6	19	D I/O or A In D I/O	Port 1.6. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address/Data 6.
P1.7 AD7	18	D I/O or A In D I/O	Port 1.7. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address/Data 7.
P2.0 AD8	17	D I/O or A In D I/O	Port 2.0. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address/Data 8.
P2.1 AD9	16	D I/O or A In D I/O	Port 2.1. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address/Data 9.
P2.2 AD10	15	D I/O or A In D I/O	Port 2.2. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address/Data 10.
P2.3 AD11	14	D I/O or A In D I/O	Port 2.3. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address/Data 11.
P2.4 ALE	13	D I/O or A In D O	Port 2.4. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Address Latch Enable.

Table 2.1. Pin Definitions for the C8051F930-GDI (Continued)

Name	Physical Pad Number	Type	Description
P2.5 $\overline{RD}$	12	D I/O or A In D O	Port 2.5. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Read Strobe.
P2.6 $\overline{WR}$	9	D I/O or A In D O	Port 2.6. See Port I/O section of the C8051F93x-C8051F92x data sheet for a complete description. Write Strobe.

3. Bonding Instructions

Table 3.1. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (QFN-32)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
1	Reserved*	—	–1013	614
2	1	DC–/GND	–1013	494
3	2	GND	–1013	247
4	3	VDD/DC+	–1013	92
5	4	DCEN	–1013	–91
6	5	VBAT	–1013	–315
7	6	$\overline{\text{RST}}$/C2CK	–1013	–626
8	7	P2.7/C2D	–1013	–810
9	8	P2.6/WR	–810	–1013
10	9	XTAL4	–525	–1013
11	10	XTAL3	–303	–1013
12	11	P2.5/RD	–54	–1013
13	12	P2.4/ALE	130	–1013
14	13	P2.3/AD11	286	–1013
15	14	P2.2/AD10	470	–1013
16	15	P2.1/AD9	626	–1013
17	16	P2.0/AD8	810	–1013
18	17	P1.7/AD7	1013	–810
19	18	P1.6/AD6	1013	–626
20	19	P1.5/AD5	1013	–470
21	20	P1.4/AD4	1013	–286
22	Reserved*	—	1013	–174
23	Reserved*	—	1014	–94
24	21	P1.3/AD3	1013	137

***Note:** Pins marked “Reserved” should not be connected.

Table 3.1. Bond Pad Coordinates (Relative to Center of Die) (Continued)

Physical Pad Number	Example Package Pin Number (QFN-32)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
25	22	P1.2/AD2	1013	279
26	23	P1.1/AD1	1013	477
27	24	P1.0/AD0	1013	619
28	25	P0.7/IREF0	1013	817
29	26	P0.6/CNVSTR	817	1013
30	27	P0.5/RX	619	1013
31	28	P0.4/TX	477	1013
32	29	P0.3/XTAL2	279	1013
33	30	P0.2/XTAL1	137	1013
34	Reserved*	—	–7	1013
35	Reserved*	—	–97	1013
36	Reserved*	—	–413	1013
37	Reserved*	—	–503	1013
38	31	P0.1/AGND	–626	1013
39	32	P0.0/VREF	–810	1013

***Note:** Pins marked “Reserved” should not be connected.

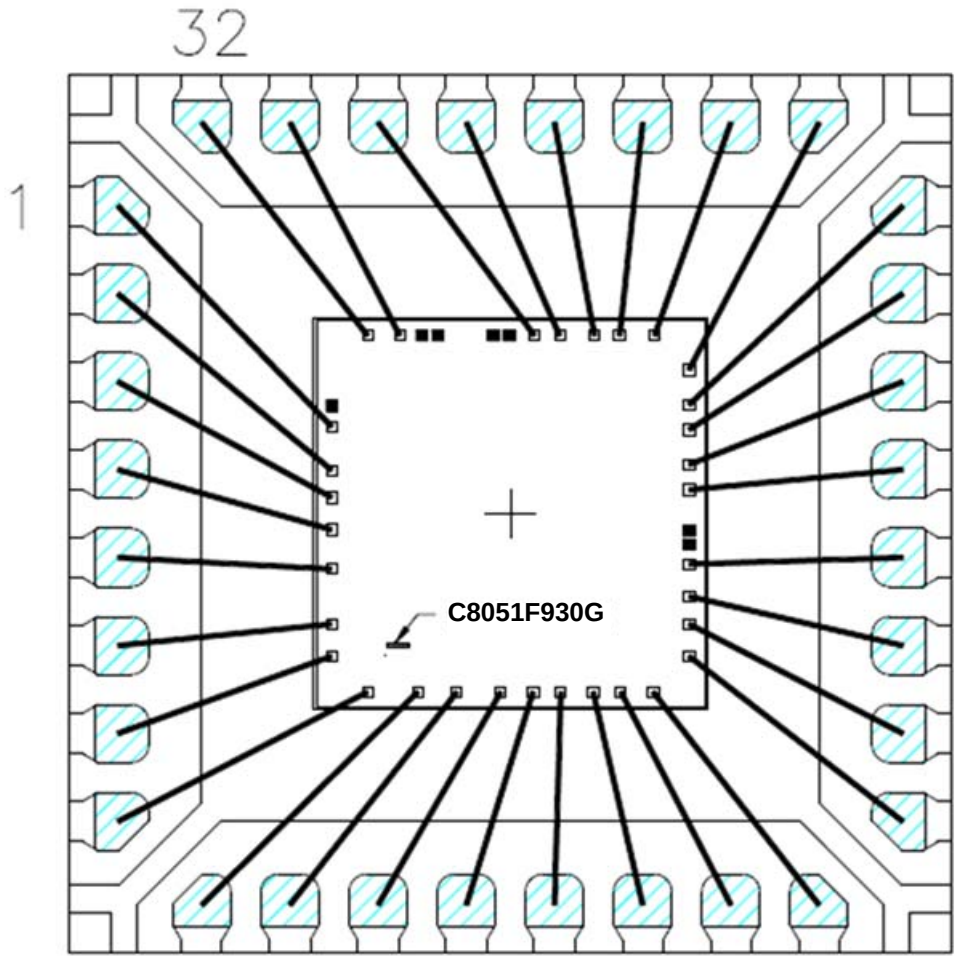


Figure 3.1. Example Die Bonding (QFN-32)

Table 3.2. Wafer and Die Information

Wafer ID	C8051F930G
Wafer Dimensions	8 in
Die Dimensions	2.28 mm x 2.28 mm
Wafer Thickness (with backgrind)	12 mil ±1 mil
Wafer Thickness (no backgrind)	28.54 mil ±1 mil, 725 µm
Wafer Identification	Notch
Scribe Line Width	80 µm
Die Per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	142 µm
***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

5. Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet this requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, backgrind or are on tape. Initial response time for FA requests that meet this requirements will be three weeks.

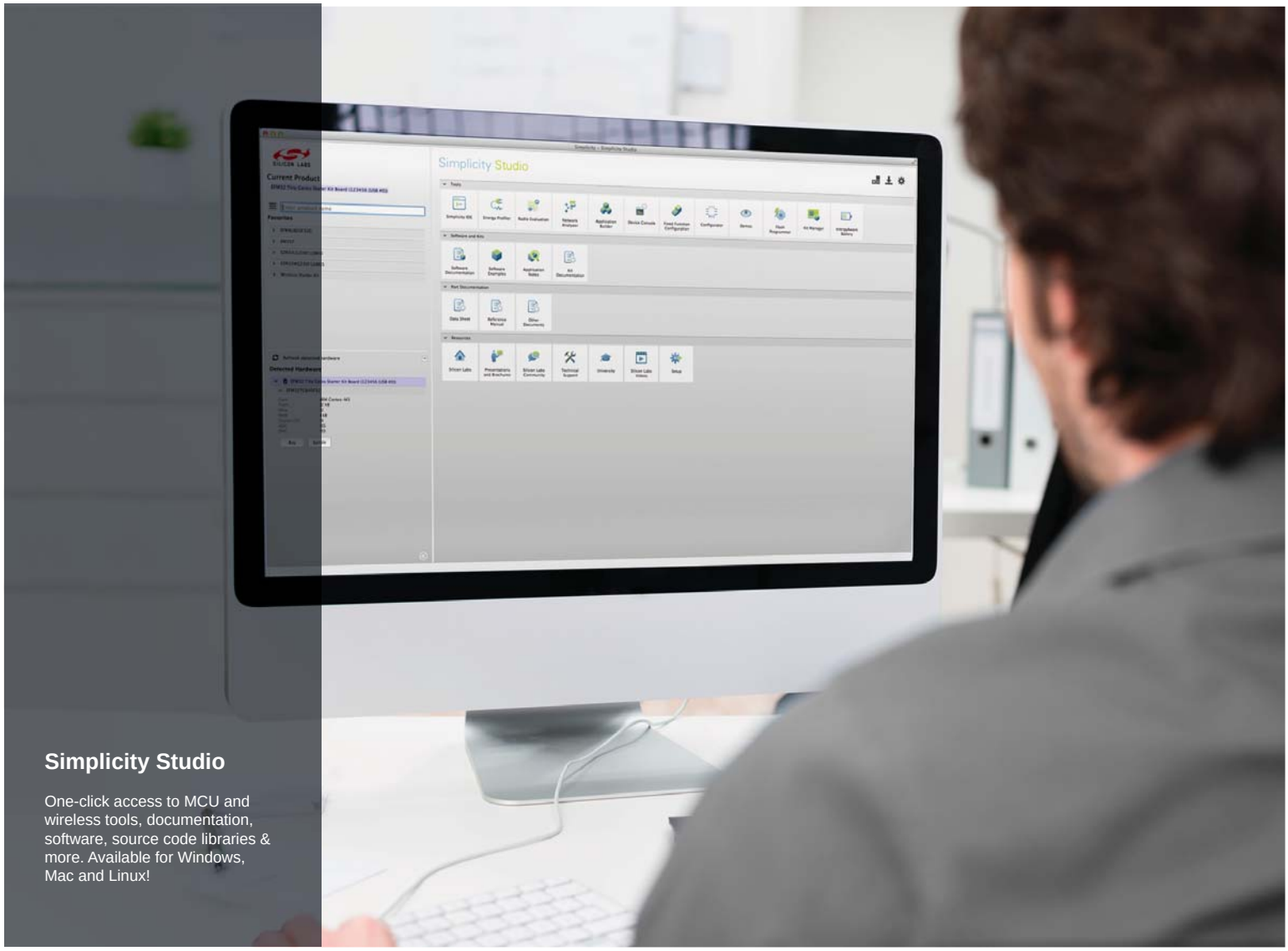
Document Change List

Revision 1.1 to Revision 1.2

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 11.

Revision 1.2 to Revision 1.3

- Replaced “C8051F930-GDI” with “C8051F930-G-GDI” (except in title).
- Updated Table 1.1 on page 2 with C8051F930-G-G1DI row.
- Updated label on Figure 3.1 on page 10 to “C8051F930G”.
- Updated Table 3.2 on page 11.
- Added “Failure Analysis (FA) Guidelines” on page 13.



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