

UG333: Class 4, 30 W EMI Compliant Isolated Evaluation Board for the Si34061

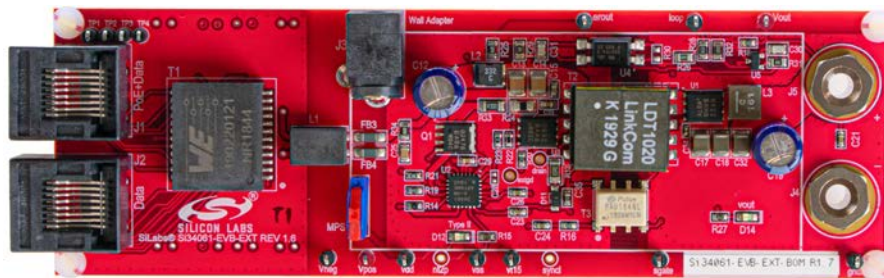
The Si34061 isolated Flyback evaluation board is a reference design for power supplies in Power over Ethernet (PoE) Powered Device (PD) applications.

The Si34061-EVB-EXT-5V maximum output is Class 4 power (30 W with isolated 5 V output).

The Si34061 IC integrates an IEEE 802.03at compatible PoE+ interface as well as a peak-current-control dc-dc controller.

KEY FEATURES

- IEEE 802.03at compatible
- High efficiency (> 90%)
- EMI compliant design
- Synchronous rectification
- High flexibility
- Integrated transient overvoltage protection
- Thermal shutdown protection
- 5x5 mm 24-pin QFN



Parameter	Condition	Specifications
Ordering part number	—	Si34061FB5VC4-KIT
PSE input voltage range	Up to Pout = 25.5 W, Connector J1	42.5 to 57 V
	Up to Pout = 12.95 W, Connector J1	37 to 57 V
Wall adapter input voltage range	Connector J3	33 to 57 V
PoE Type/Class	Type 2/Class 4	IEEE 802.3at
Output voltage/current	Connectors J4-J5	5 V / 6 A
Efficiency, end-to-end	$V_{IN} = 48$ V from wall adapter	89.7 %
Efficiency, dc-dc converter	$V_{IN} = 50$ V from PSE	91.5 %
Efficiency, end-to-end	$V_{IN} = 50$ V from PSE	89.1 %
Switching frequency	$R_{FREQ} (R14) = 95.3$ k Ω	200 kHz
Conducted EMI	EN55032, average and peak detector	Passed
Radiated EMI	EN55032 Class B	Passed

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1. Kit Description and Powering up the Si34061-EVB-EXT-5V

The Si34061-EVB-EXT-5V Flyback based evaluation board is a reference design for power supplies in Power over Ethernet (PoE+) Powered Device (PD) applications. The Si34061 device is described more completely in the data sheet and application notes.

The Si34061-EVB-EXT-5V board is shown on the cover page.

To achieve high efficiency, this board is set up with external Schottky diode bridges; however, a silicon type external diode bridge can be used as well. In that case, the CT/SP pins should be connected to the PSE (RJ45 – J1).

To compensate for the reverse leakage of Schottky type diode bridges at high temperatures, the recommended detection resistor should be adjusted to the values listed in the following table:

Table 1.1. Recommended Detection Resistor Values

External Diode Bridge	R_{DET} (R21)
Silicon Type	24.3 k Ω
Schottky Type	24.9 k Ω

Ethernet data and power are applied to the board through the RJ45 connector (J1). The Ethernet data can be obtained from J2. The design can be used in Gigabit (10/100/1000) systems as well.

Power may be applied in the following ways:

- Using any IEEE 802.3-2015-compliant, PoE-capable PSE, or
- Using a laboratory power supply unit (PSU)

Powering the PD using a PSU:

- Connecting a dc source between blue/white-blue and brown/white-brown of the Ethernet cable (either polarity), (End-span) as shown below:

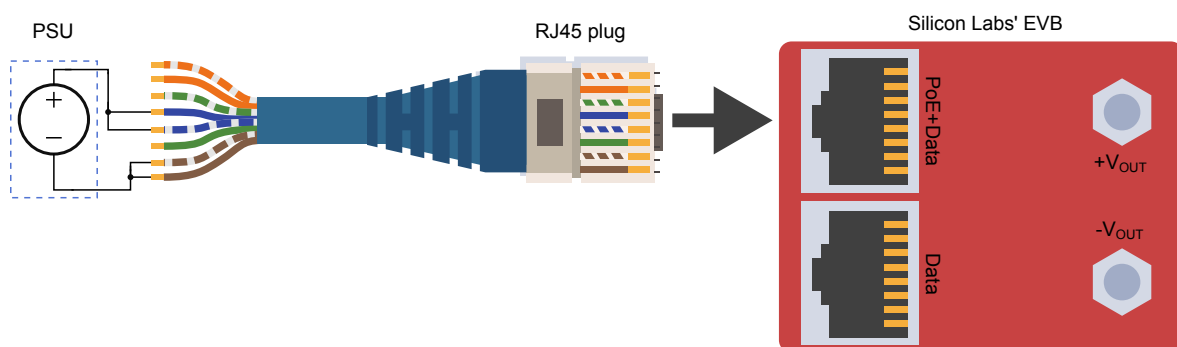


Figure 1.1. Endspan Connection Using Laboratory Power Supply

- Connecting a dc source between green/white-green and orange/white-orange of the Ethernet cable (either polarity), (Mid-span) as shown below:

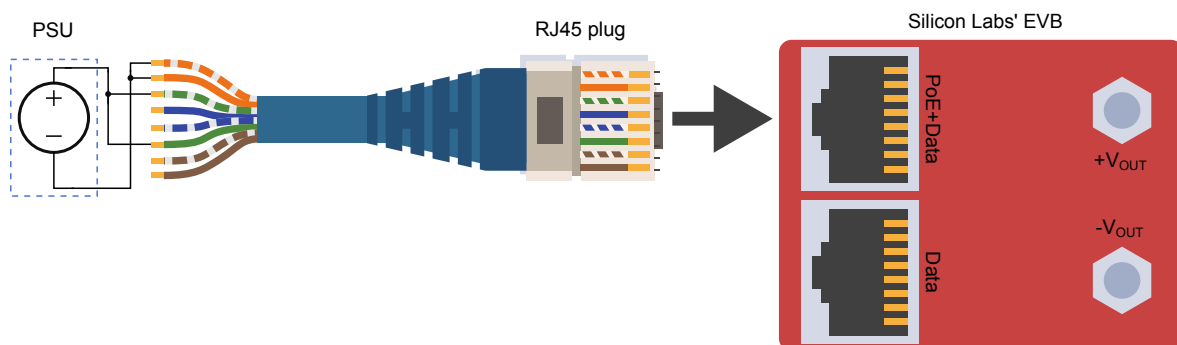


Figure 1.2. Midspan Connection Using Laboratory Power Supply

2. Si34061-EVB-EXT-5V Board Schematics

The following figure shows the input interface portion of the schematic:

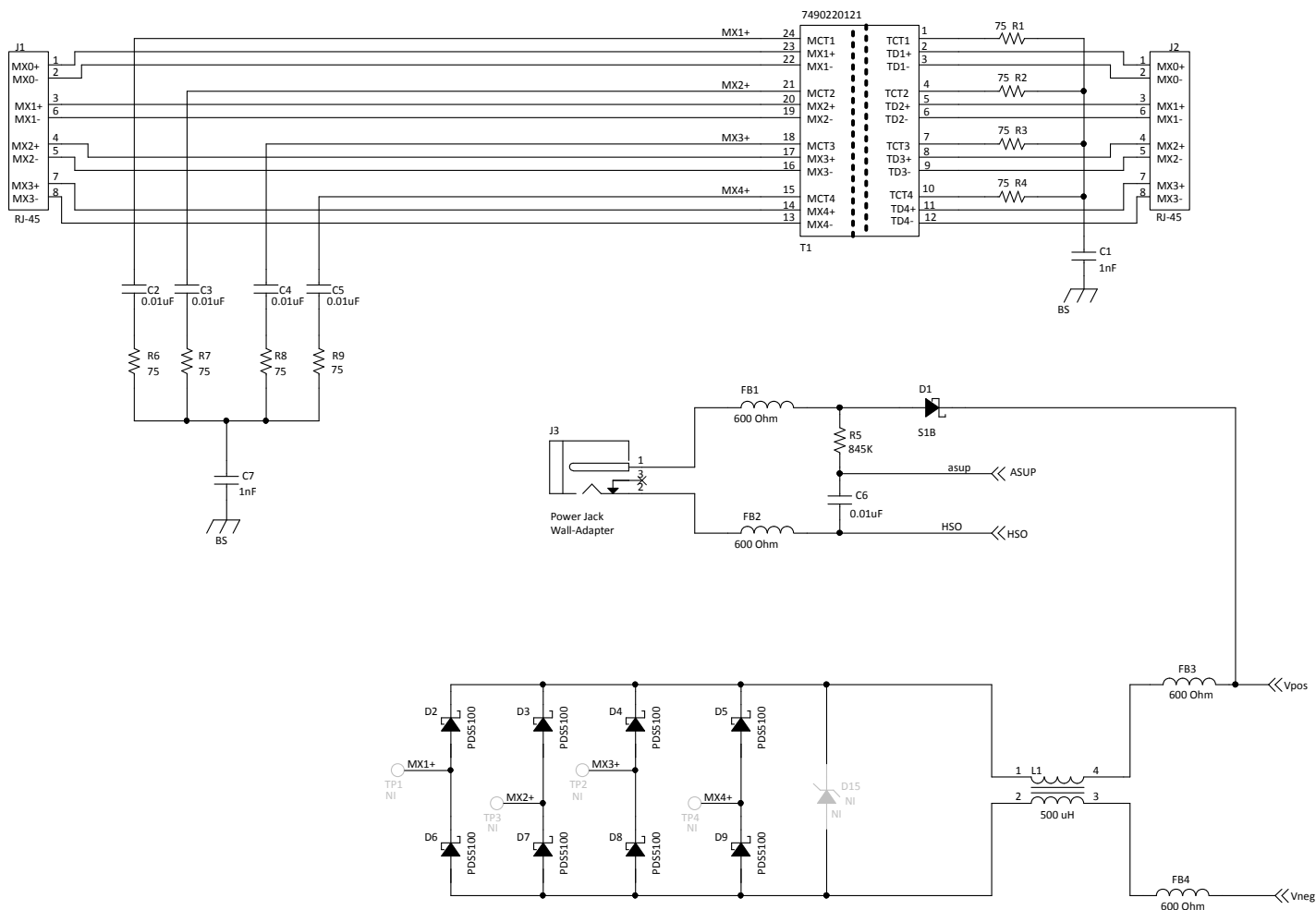


Figure 2.1. Si34061-EVB-EXT-5V Schematic: Input Interface

The Si34061 PD controller includes an integrated 100 V protection device that offers adequate protection for indoor applications and passes the IEC 61000-4-5 combination wave test (1.2/50 μ s open circuit voltage, 8/20 μ s short-circuit current) up to 4.4 kV common-mode and differentially to > 400 V.

In special installation classes where high differential and common-mode surge immunity are required, an external TVS protection device (e.g., SMDJ58A) may be installed between VNEG and VPOS to increase the surge immunity – D15.

With the external protection installed, common-mode surge immunity up to 6 kV and differential immunity up to 2 kV can be achieved.

The Si34061-EVB-EXT can also be powered from a wall adapter through connector J3. The following figure shows the dc-dc converter part of the schematic:

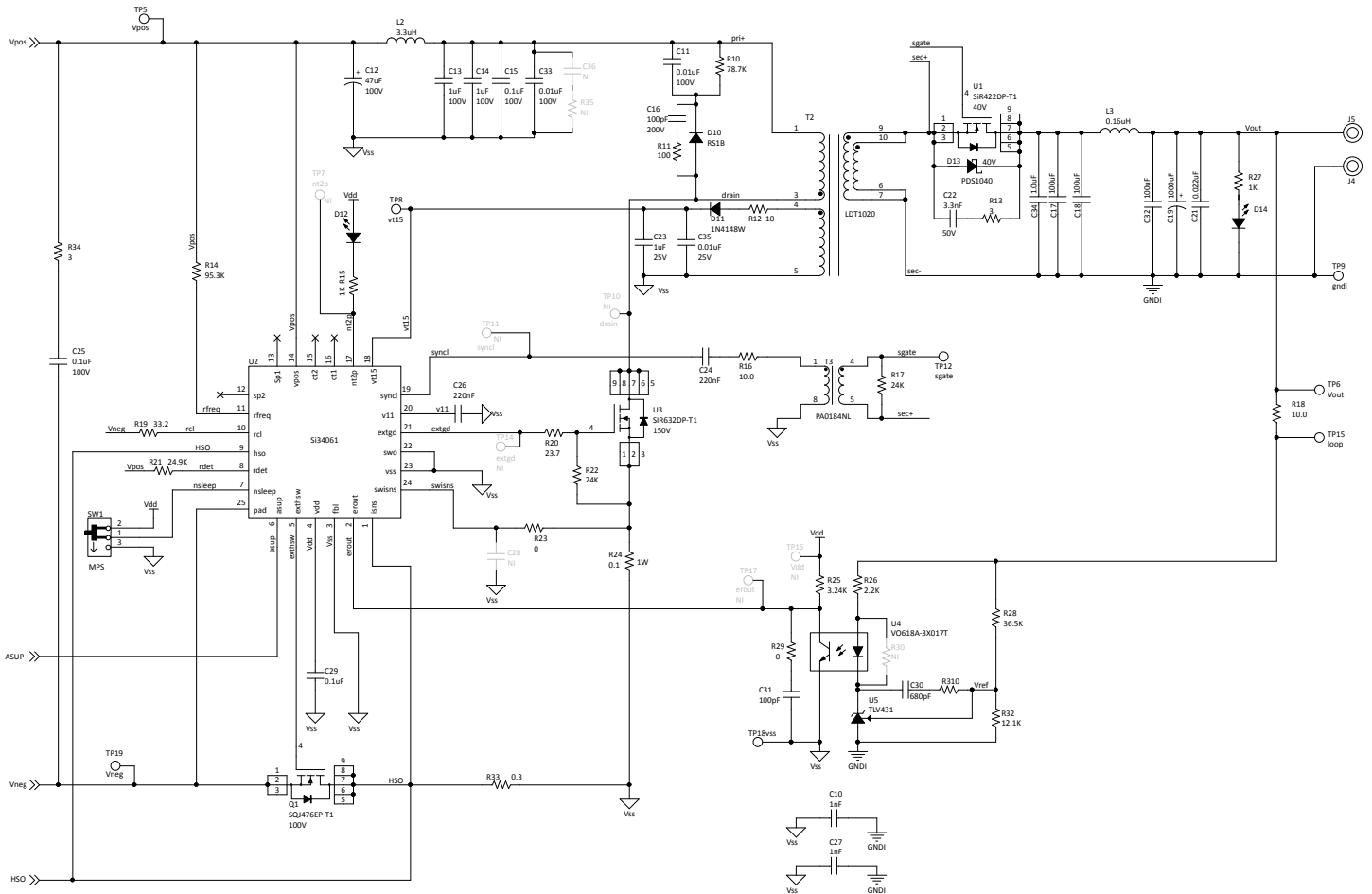


Figure 2.2. Si34061-EVB-EXT-5V Schematic: DC-DC Converter

3. Conversion Efficiency of the Si34061-EVB-EXT-5V Board

The figures below show the conversion efficiency of the Si34061-EVB-EXT-5V board with 5 V output. The charts present:

- DC-DC converter efficiency at three different input voltages: 42.5, 50, and 57 V
- End-to-end efficiency powered from a PSE at three different input voltages: 42.5, 50, and 57 V
- End-to-end efficiency powered from a 48 V wall adapter

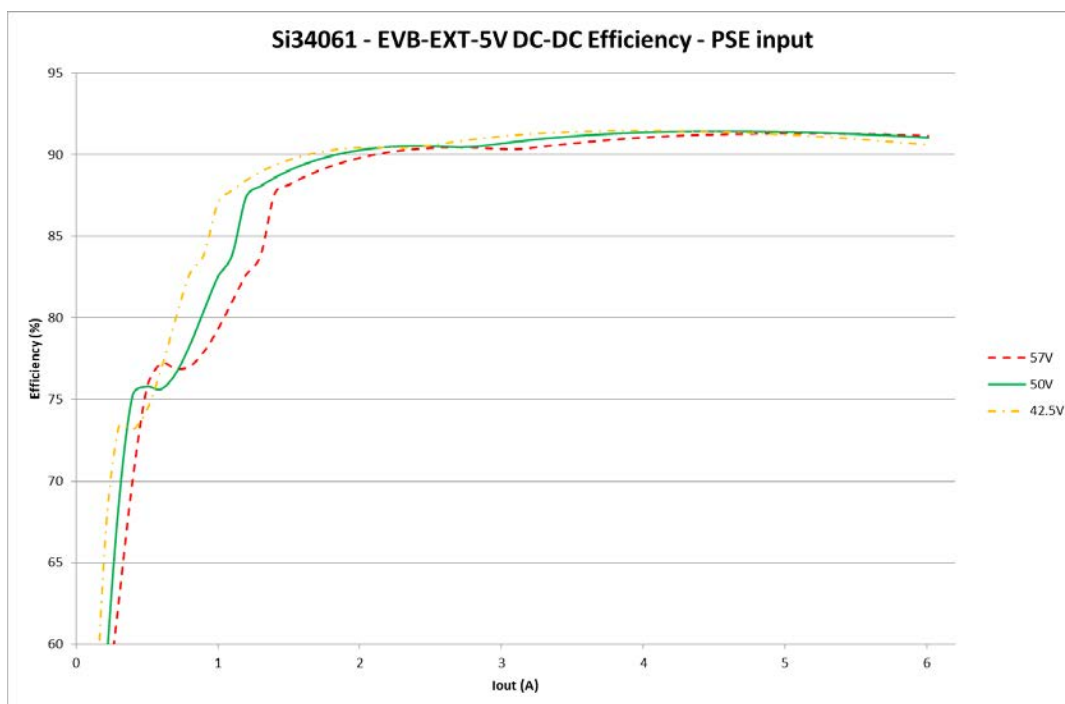


Figure 3.1. DC-DC Conversion Efficiency of the Si34061-EVB-EXT-5V with 5 V Output Powered from PSE

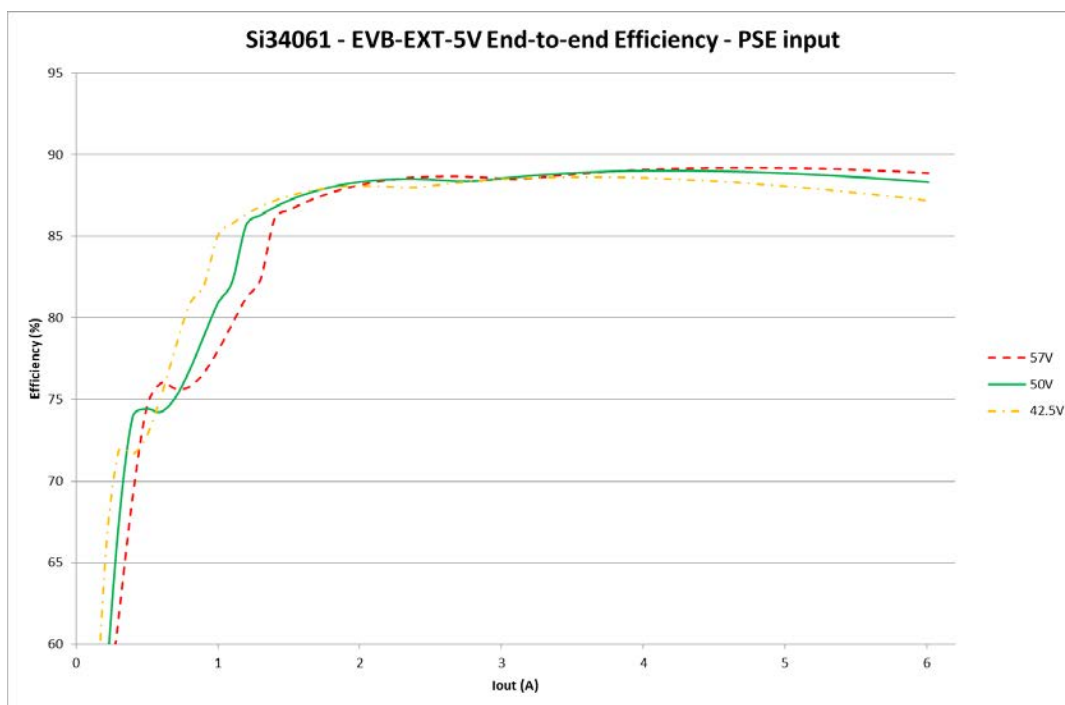


Figure 3.2. End-to-End Conversion Efficiency of the Si34061-EVB-EXT-5V with 5 V Output Powered from PSE

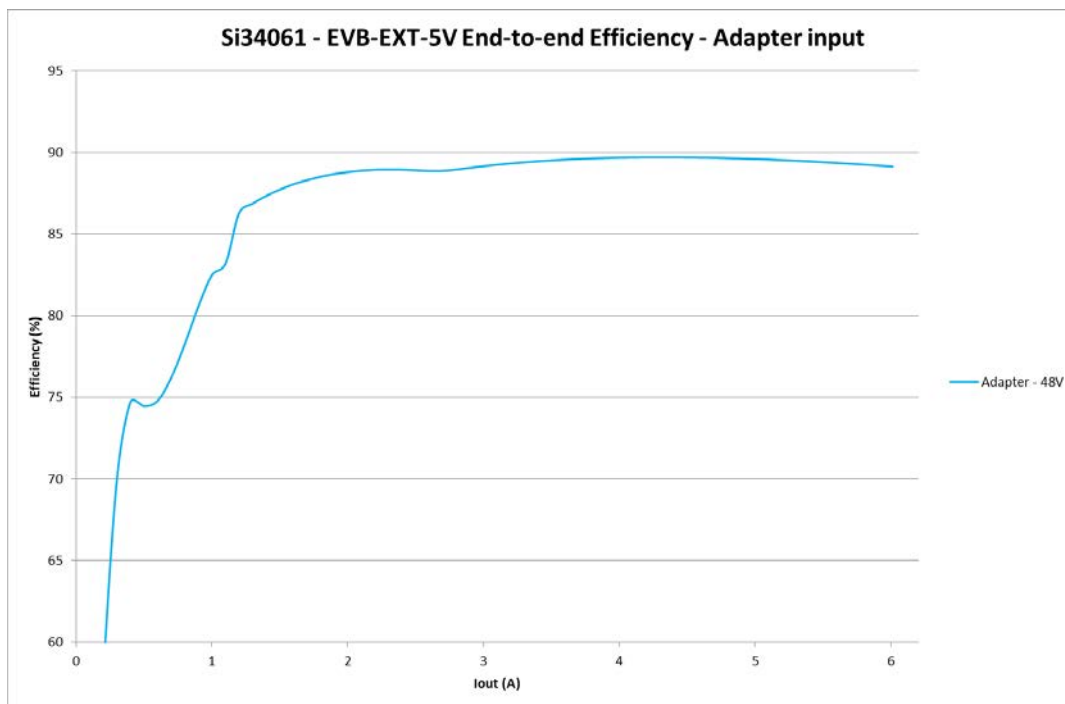


Figure 3.3. Conversion Efficiency of the Si34061-EVB-EXT-5V with 5 V Output Powered from 48 V Wall Adapter

Note: During the efficiency measurements, D12 and D14 LEDs were removed since they are merely indicators and not required parts of the design.

4. SIFOS PoE Compatibility Test Results

The PDA-300 Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at PoE Powered Devices (PDs). The following figure shows the passing SIFOS Test report of the Si34061-EVB-EXT-5V board.

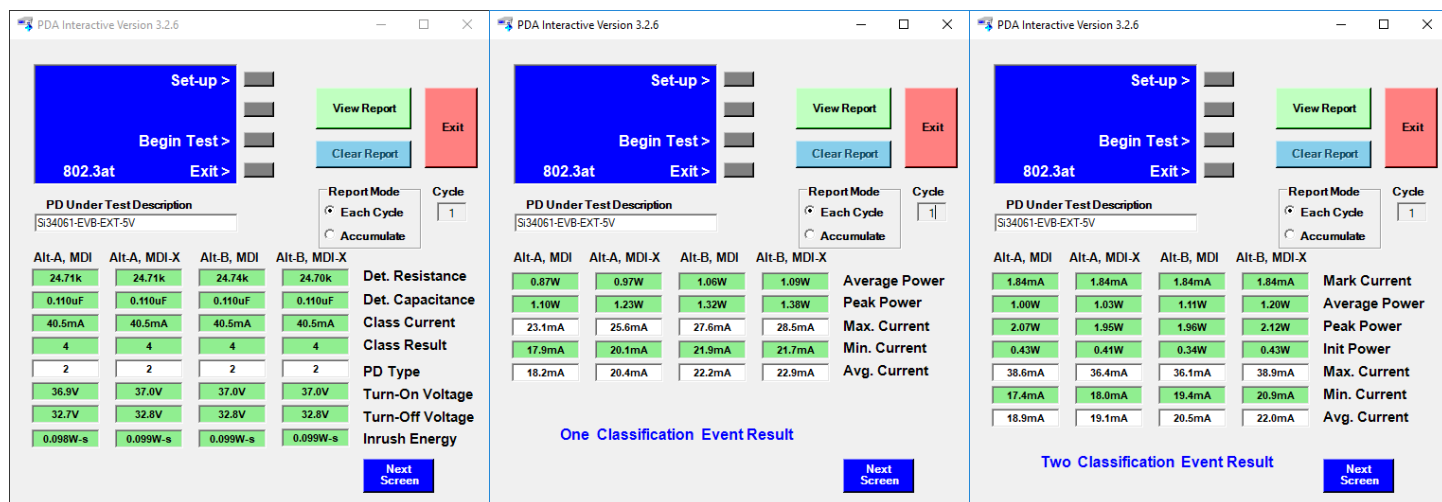


Figure 4.1. Si34061-EVB-EXT-5V PD SIFOS PoE Compatibility Test Results

5. Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si34061 integrates a current-mode-controlled switching-mode power supply controller circuit; therefore, the application is a closed-loop system. To guarantee a stable power supply output voltage and reduce the influence of input supply voltage variations and load changes on the output voltage, the feedback loop must be stable.

To verify the stability of the loop, the loop gain and loop phase shift have been measured.

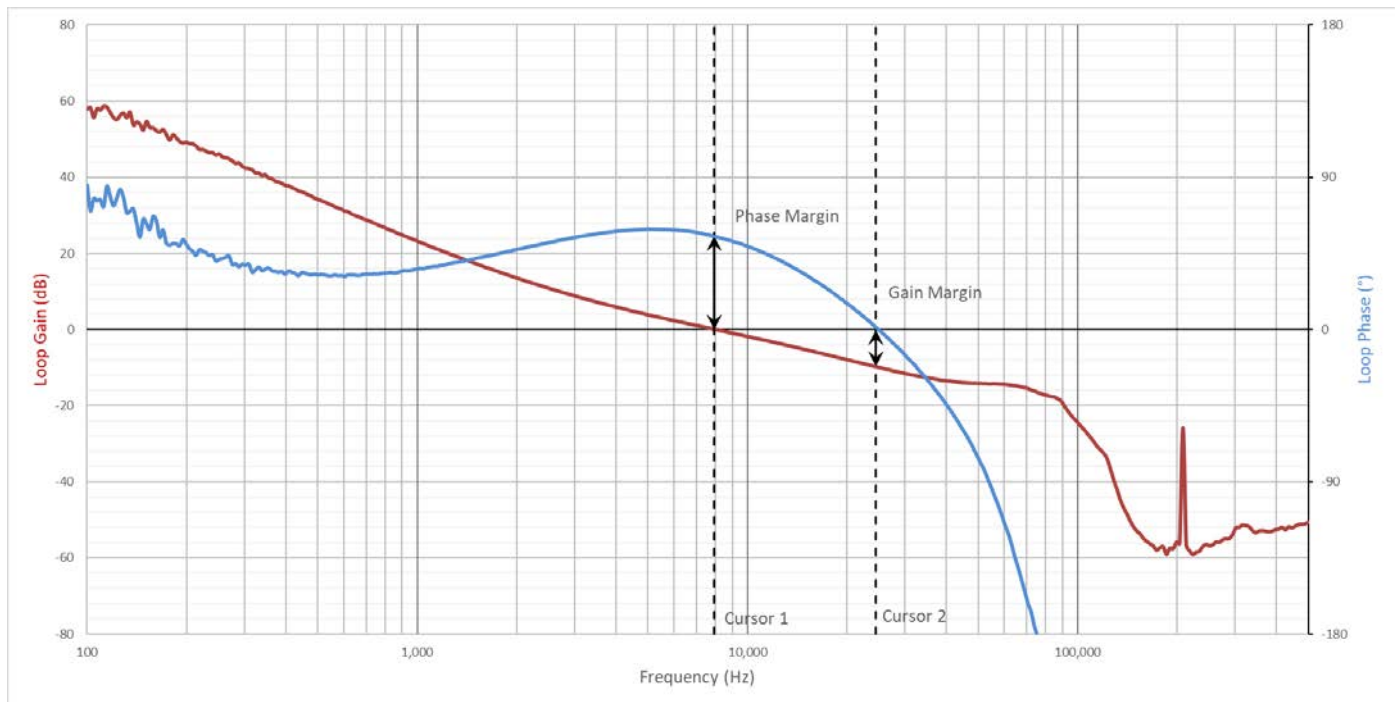


Figure 5.1. Si34061-EVB-EXT-5V Measured Loop-Gain and Phase-Shift Measured at Full Load

Table 5.1. Measured Loop Gain and Phase Shift of the Si34061-EVB-EXT-5V

	Frequency	Gain	Phase
Phase Margin (Cursor 1)	8 kHz	0 dB	55°
Gain Margin (Cursor 2)	25 kHz	-10 dB	0°

6. Load Step Transient Measurement Results

The Si34061-ISO-FB EVB board's output has been tested with a step load function to verify the converter's output dynamic response.

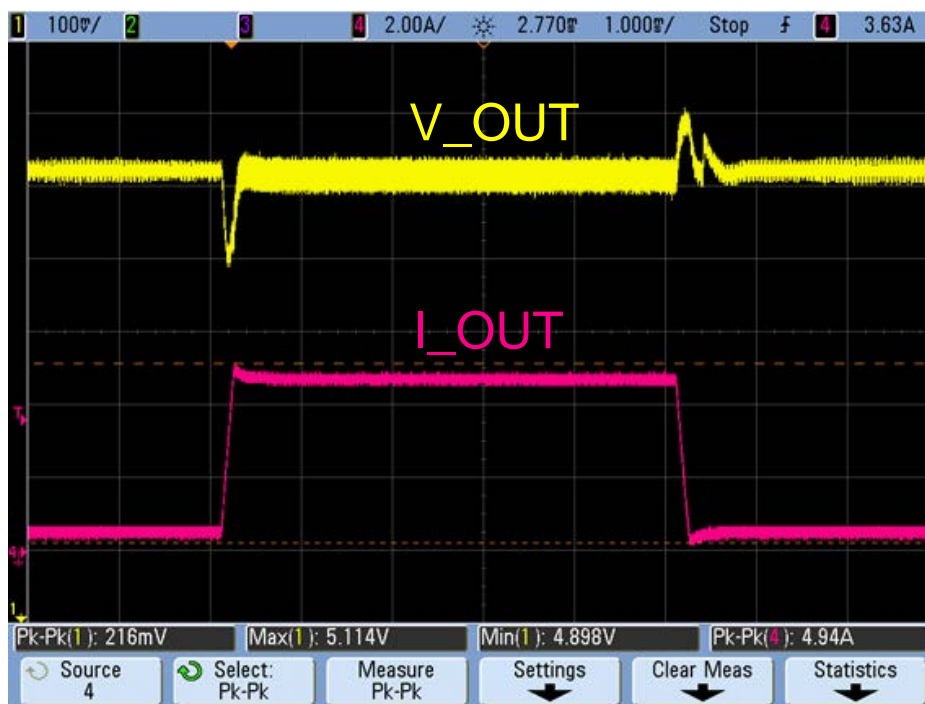


Figure 6.1. Si34061-EVB-EXT-5V Output Load Step Transient Test

Table 6.1. Output Load Step Transient

	From (Output Current)	To (Output Current)	V _{OUT} Change
Load step	0.5 A	5 A	5 V – 102 mV
Load step	5 A	0.5 A	5 V + 114 mV

7. Output Voltage Ripple

The Si34061-EVB-EXT-5V board's output voltage ripple has been measured at no-load and full-load conditions. The following figures show the respective results.

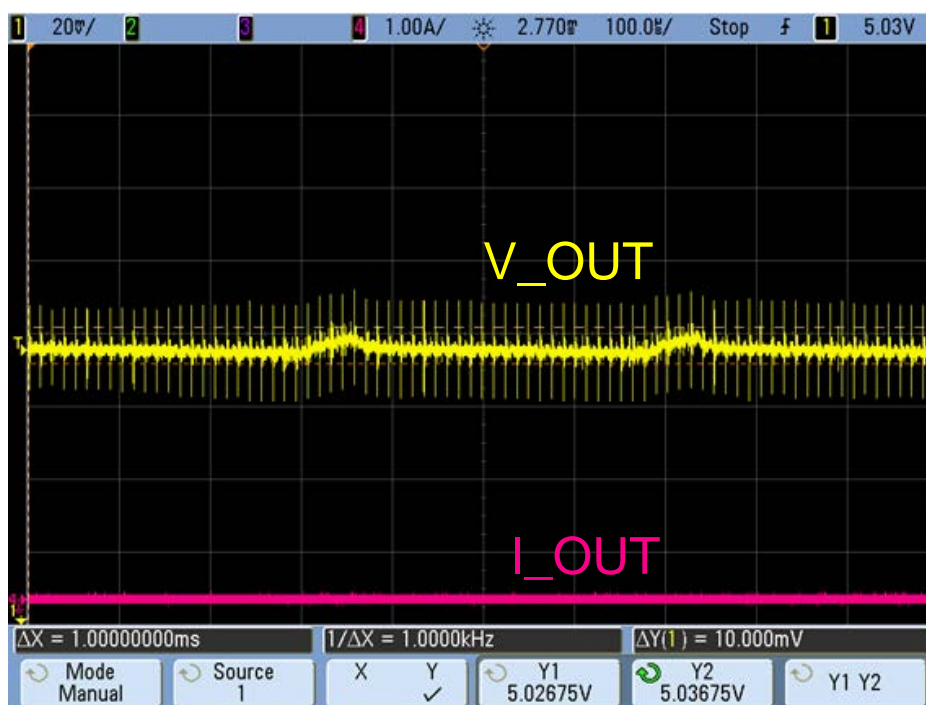


Figure 7.1. Si34061-EVB-EXT-5V Output Voltage Ripple at No-Load Condition: 10 mV

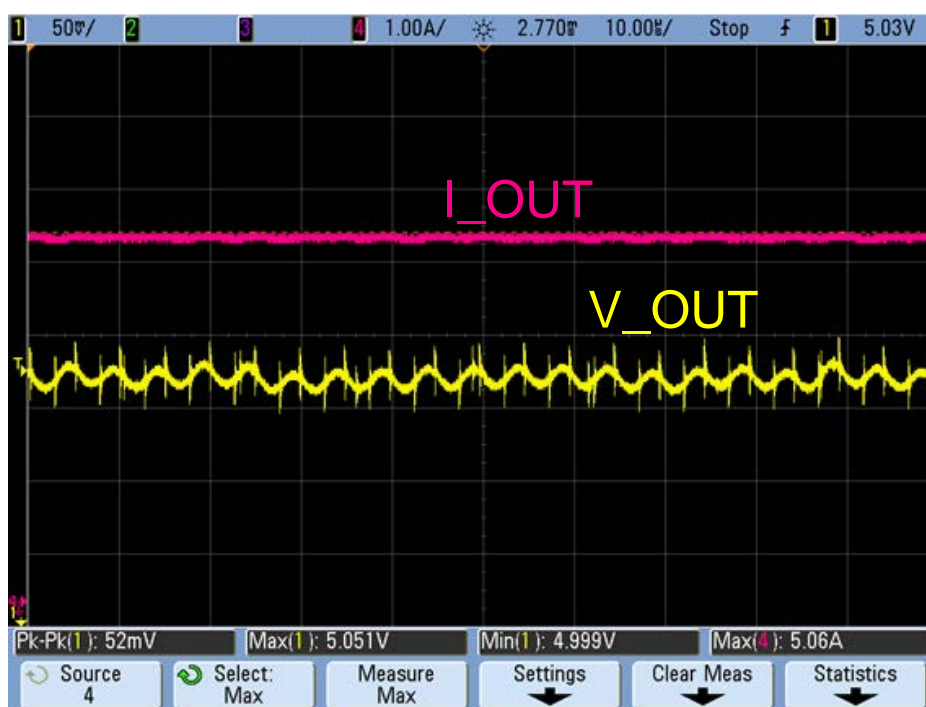


Figure 7.2. Si34061-EVB-EXT-5V Output Voltage Ripple at 5 A Output: 50 mV

8. Soft Start Protection

The Si34061 has an integrated dynamic soft-start protection mechanism to avoid stressing the components with the sudden current or voltage changes associated with initial charging of the output capacitors.

The Si34061 intelligent adaptive soft-start mechanism does not require any external components to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, adjusting the output voltage ramp-up time as a function of the attached load.

The controller allows the output voltage to rise faster in a no-load (or light load) condition. With a heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

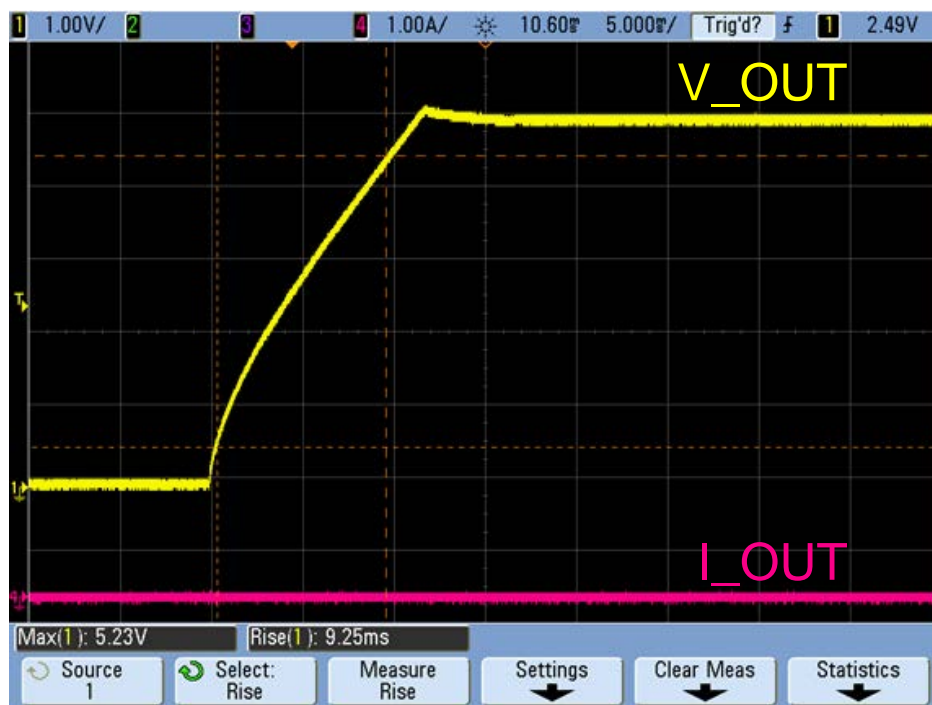


Figure 8.1. Si34061-EVB-EXT-5V Soft-Start with No Load

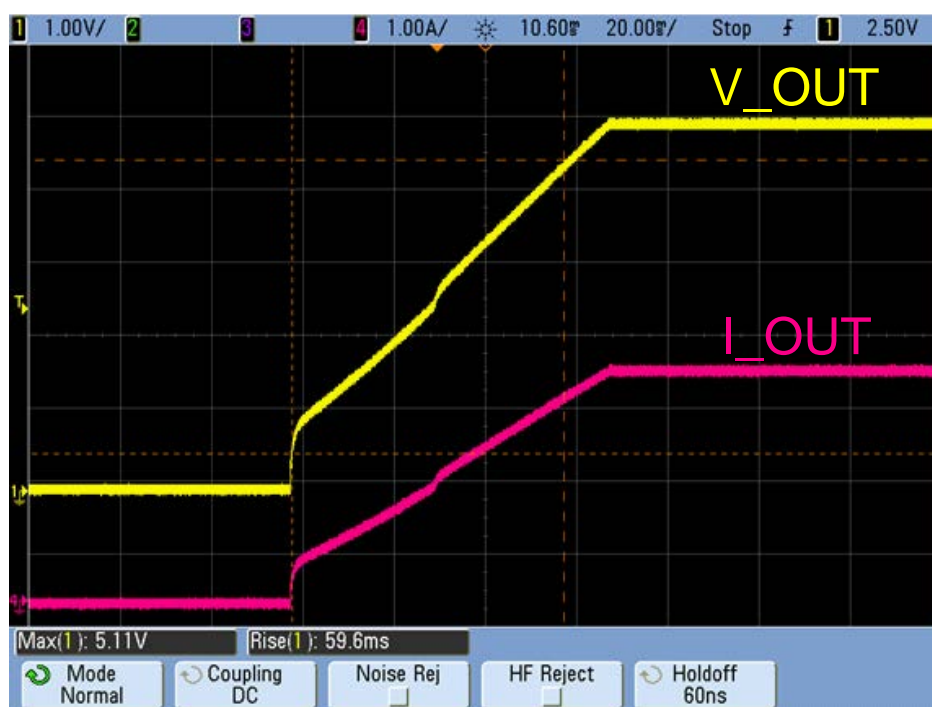


Figure 8.2. Si34061-EVB-EXT-5V Soft-Start with Heavy Load

9. Output Short Protection

The Si34061 PD device has an integrated output short-protection mechanism that protects the IC itself and the surrounding external components from overheating in case of an electrical short on the output. This case is depicted in the figure below by showing the PD's input current and the PD's output voltage when the short is present.

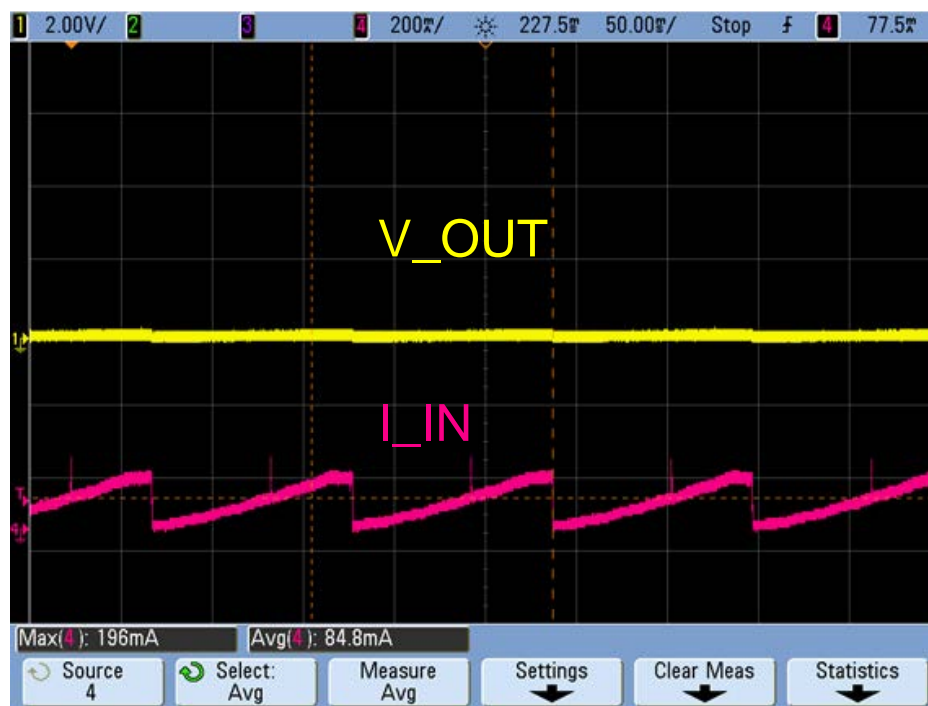


Figure 9.1. Si34061-EVB-EXT-5V Output Short Protection Mechanism

10. Pulse Skipping at No-Load Condition

As the output load decreases, the controller starts to reduce the pulse width of the PWM signal (switcher ON time). At some point, even the minimum width pulse will provide higher energy than the application requires, which could result in loss of voltage regulation.

When the controller detects a light load condition (which requires less ON time than the minimum pulse width), the controller enters into burst or light-load skipping mode. This mode is shown in the figure below, which depicts the switching node of the primary FET (U3) at a no-load condition.

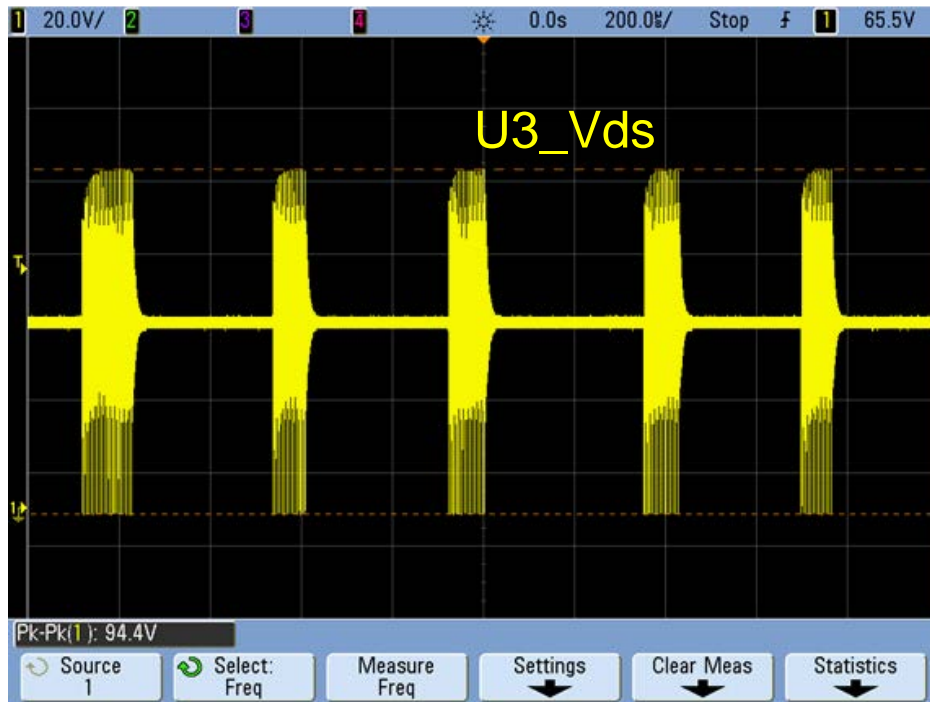


Figure 10.1. Pulse Skipping at No-load Condition

11. Adjustable EVB Current Limit

For additional safety, the Si34061 has an adjustable EVB current limit feature.

The Si34061 controller measures the voltage on the R_{SENSE} (R33) through the ISNS pin. Attention must be paid when this voltage goes below VSS. When V_{RSENSE} reaches -270 mV (referenced to VSS), the current limiter restarts the circuit to protect the application.

The R_{SENSE} value also defines the power level at which the external-HSSW (Q1) and synchronous-FET (U1) are enabled.

When the V_{RSENSE} value is < -30 mV (referenced to VSS), the controller is in low-power mode:

- Q1 - EXT-HSSW is disabled
- U1 – Synchronous FET is disabled

When the V_{RSENSE} value is > -30 mV (referenced to VSS), the controller enters high-power mode:

- Q1 - EXT-HSSW is enabled
- U1 – Synchronous FET is enabled

When V_{RSENSE} reaches -30 mV (referenced to VSS), the current EXTHSSW pin goes up, and the SYNCL pin starts to drive the synchronous FET.

The EVB current limit for Class 4 applications can be calculated with the following formula:

$$R_{SENSE} = 0.3\Omega$$
$$I_{LIMIT} = \frac{270mV}{R_{SENSE}} = \frac{270mV}{0.3\Omega} = 0.9A$$

Equation 1.

With the selected R_{SENSE} value, the external HSSW (Q1) and synchronous-FET (U1) are enabled at the input current calculated below:

$$I_{power-mode} = \frac{30mV}{R_{SENSE}} = \frac{30mV}{0.3\Omega} = 0.1A$$

Equation 2.

Below the calculated value from Equation 2, the internal HSSW conducts, and rectification is accomplished through the D13 diode.

Above the value of Equation 2, the external HSSW conducts and synchronous rectification is accomplished by the U1 FET.

12. Tunable Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor, R14, connected between the RFREQ and VPOS pins. The following figure will aid in selecting the RFREQ value to achieve the desired switching frequency.

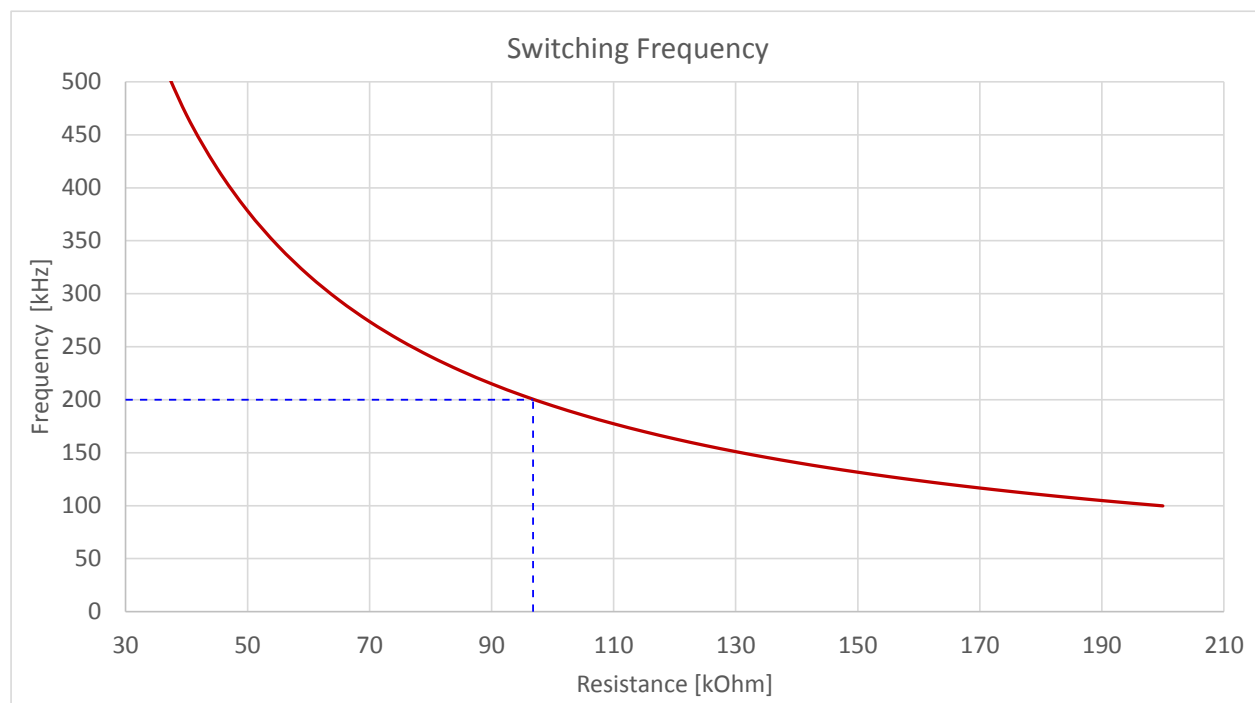


Figure 12.1. Switching Frequency vs. R_{RFREQ} Value

The selected switching frequency for Si34061-EVB-EXT-5V is 200 kHz, which is achieved by setting the R33 resistor to 95.3 kΩ.

13. Synchronous Rectification

The Si34061 device has a synchronous gate driver (SYNCL) to drive the synchronous-MOSFET.

At low-load (below Equation 1 value), the SYNCL driver is disabled, and the converter can work in discontinuous current mode (DCM). In this mode, the drain-source voltage waveform of U3 has a ringing waveform, which is typical for a DCM operation. The drain-source voltage waveform is depicted in the following figure:

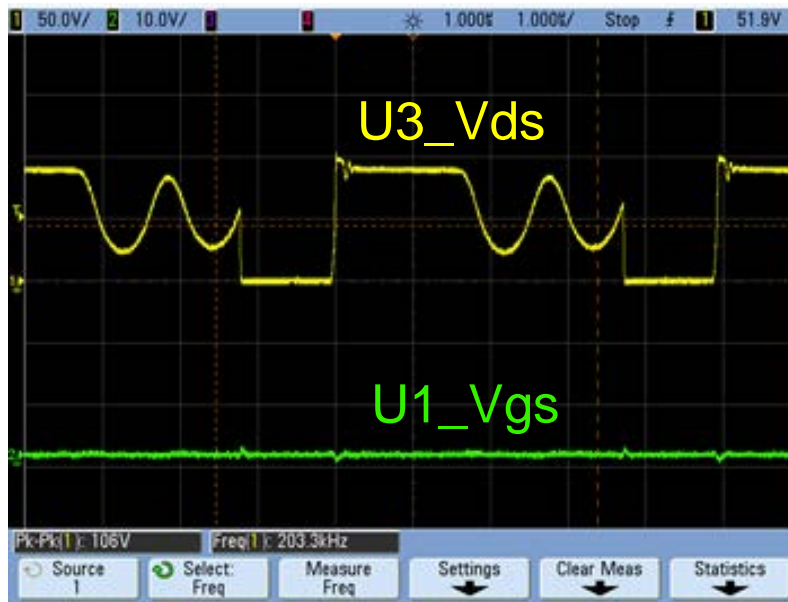


Figure 13.1. Discontinuous Current Mode at Low-Load Condition

At heavy load, the synchronous rectification driver is enabled, and the converter runs in continuous current mode (CCM) as shown in the following figure:

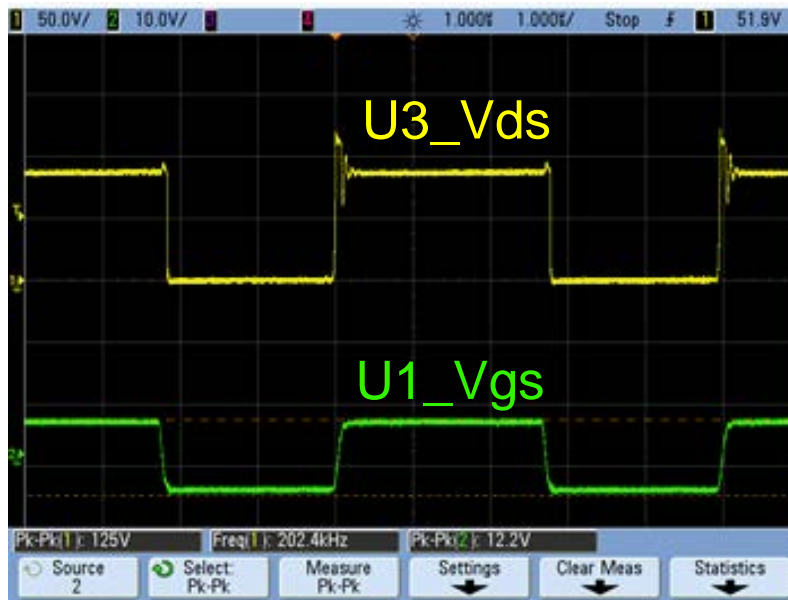


Figure 13.2. Continuous Current Mode at High-Load Condition

14. Maintain Power Signature

The Si34061 device integrates an MPS circuit that ensures connection with the PSE if the PD application current drops below the PSE maintain-power-signature threshold level. When nSLEEP is low at startup, MPS generation depends on the total average current consumption. The controller detects the low consumption and, in order to keep the connection with the PSE, starts to generate the MPS pulses. This case is depicted in the following figure:

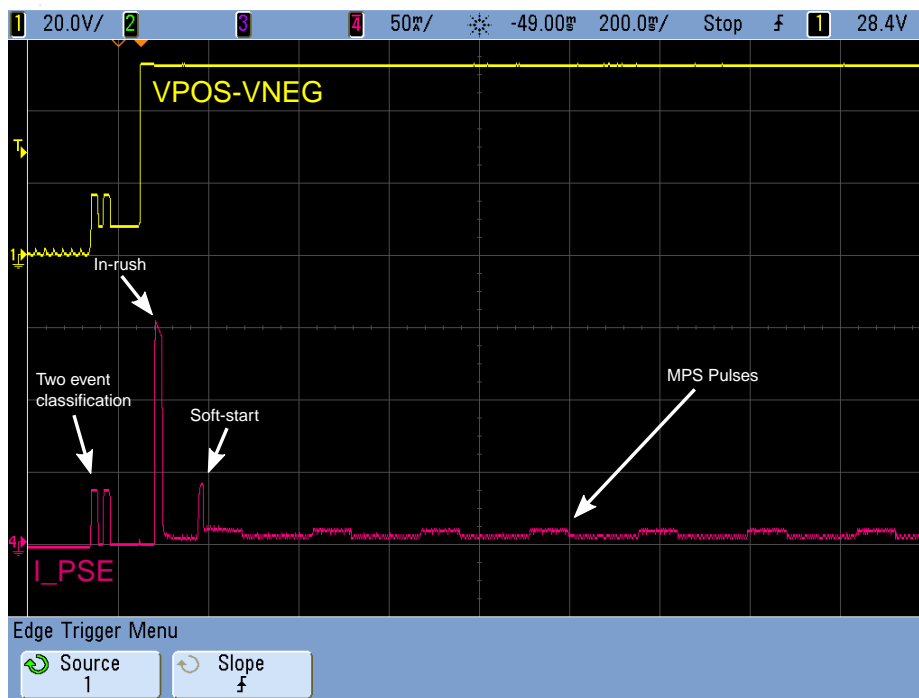


Figure 14.1. MPS Enabled: Connection is Kept with PSE

When nSLEEP is high at startup, MPS generation is disabled. Due to the low port current, the PSE will disconnect the port. In this mode (when nSLEEP is low at startup), MPS generation can be controlled (enabled/disabled) by the user by toggling nSLEEP between low and high.

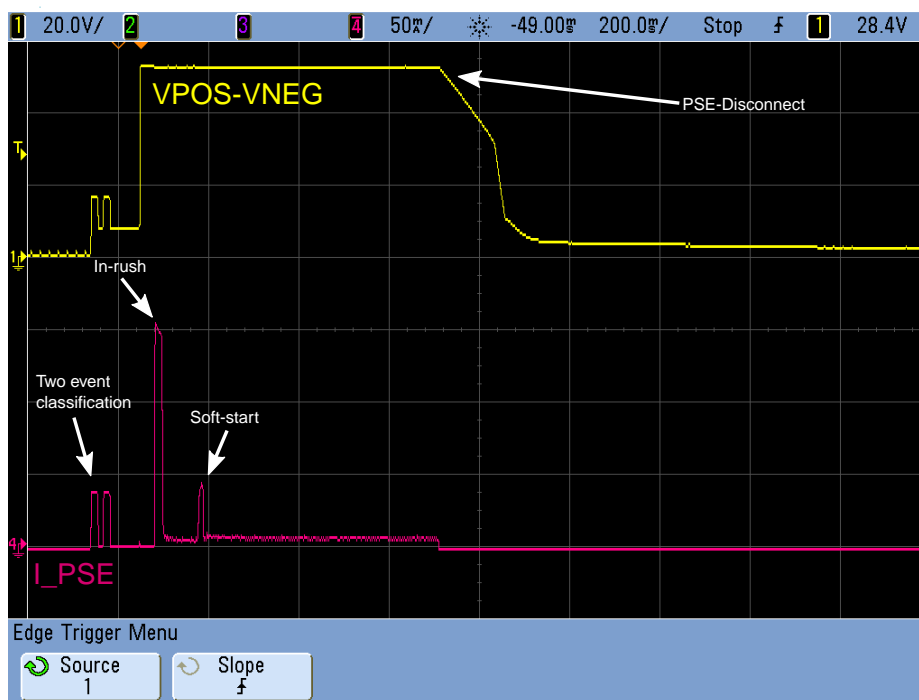


Figure 14.2. MPS Disabled: PSE Disconnects the Port

15. Wall Adapter Support with Priority over PSE

The Si34061-EVB-EXT-5V board can be driven from a wall adapter instead of a PSE. The wall adapter has higher priority than the PSE.

The figure below shows a regular Type-2 startup sequence with the PSE; then, a wall adapter is plugged in. Through the ASUP digital input pin, the Si34061 automatically detects the presence of the wall adapter and starts drawing power from it.

During the transition from the PSE to the wall adapter, there is no interrupt on the output voltage (application).

In wall adapter mode, the Si34061 shows a non-valid detection signature toward the PSE. Therefore, until the wall adapter voltage is present, the PSE is unable to detect and turn ON the PD.

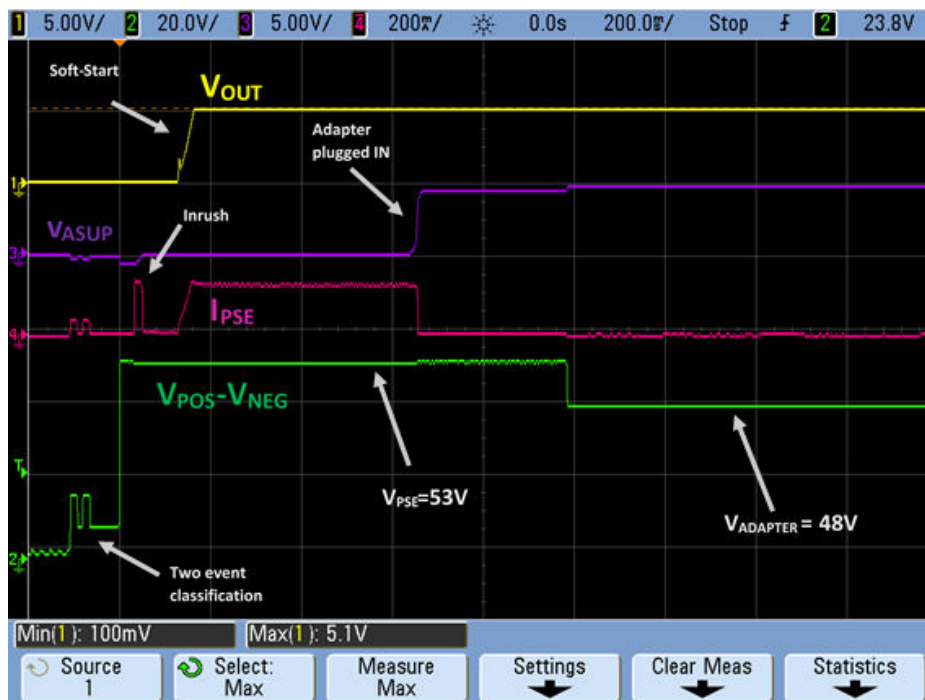


Figure 15.1. Wall Adapter Sequence Using ASUP Pin

16. Radiated Emissions Measurement Results—EN55032 Class B

Radiated emissions of the Si34061-EVB-EXT-5V board have been measured with 50 V input voltage and a full load connected to the output (30 W).

As shown in the following figure, the Si34061-EVB-EXT-5V board is fully compliant with international EN 55032 Class B emissions standards:

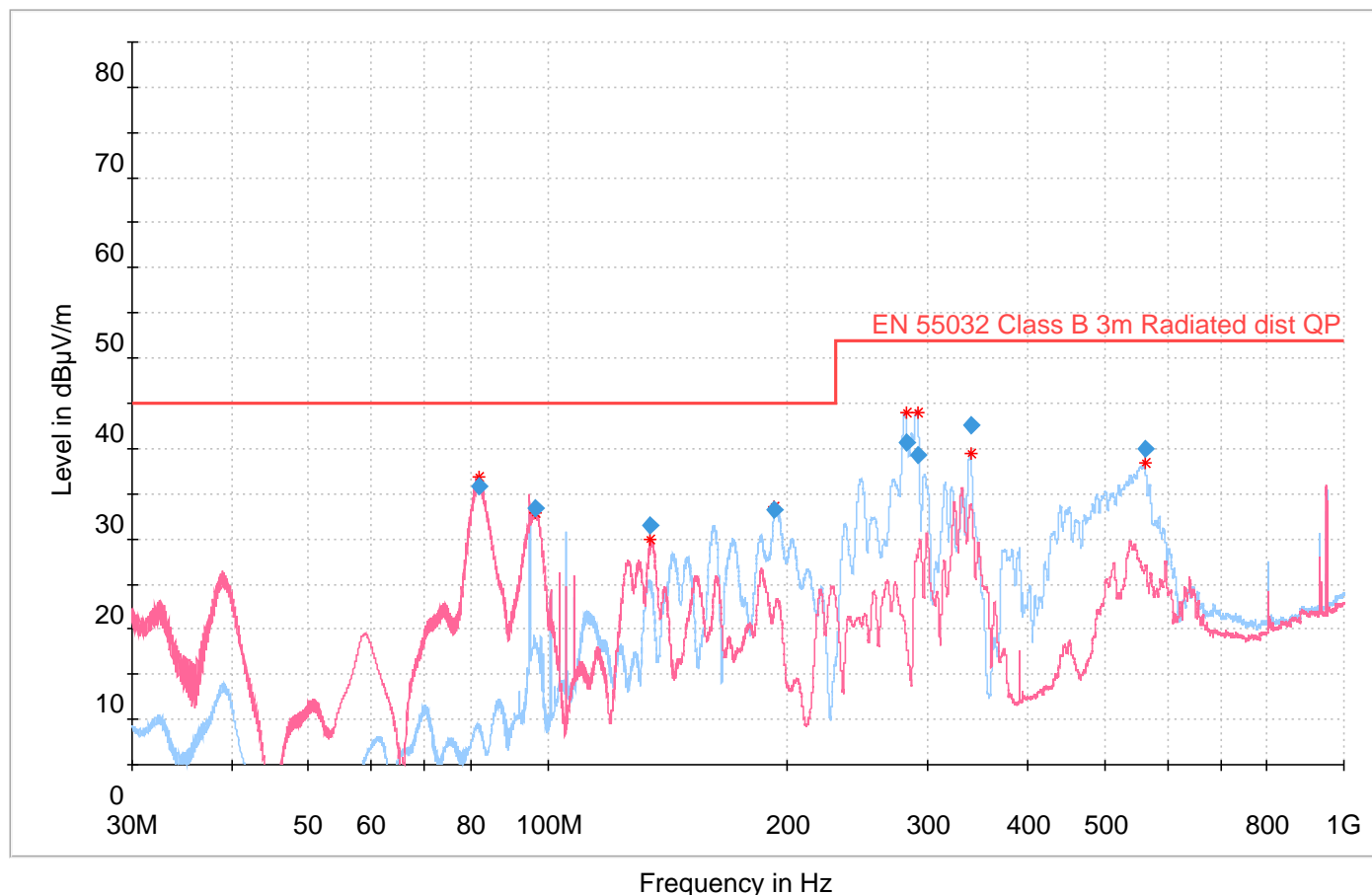


Figure 16.1. Si34061-EVB-EXT-5V Radiated Emissions Measurement Results with 50 V Input and 30 W Output Load

16.1 Radiated EMI Measurement Process

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization).

Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

17. Conducted Emissions Measurement Results—EN55032

The Si34061-EVB-EXT-5V board's conducted emissions have been measured with both peak and average detectors. The following figure shows the conducted EMI measurement setup.

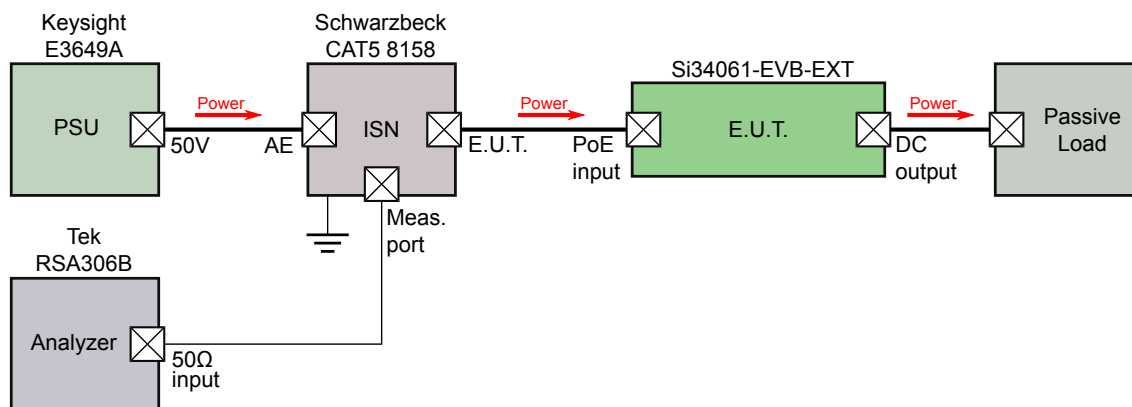


Figure 17.1. Conducted EMI Measurement Setup

The following figures show the measured results.

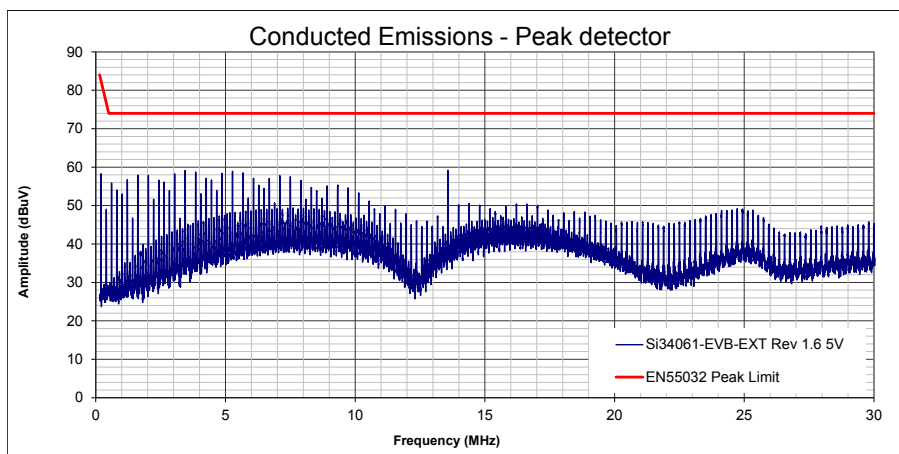


Figure 17.2. Si34061-EVB-EXT-5V Peak Detector Conducted Emissions Measurement Results with 50 V Input and 30 W Output Load

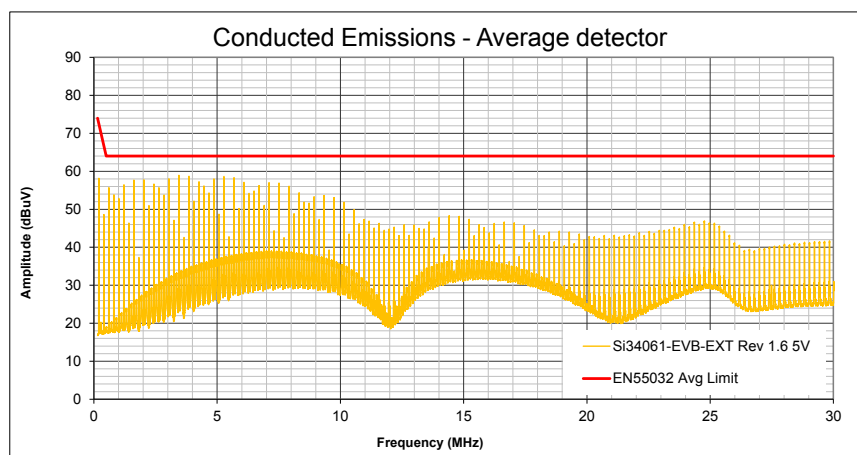


Figure 17.3. Si34061-EVB-EXT-5V Average Detector Conducted Emissions Measurement Results with 50 V Input and 30 W Output Load

18. Thermal Measurements

The Si34061-EVB-EXT-5V board's top and bottom side thermal images at full load are shown in the following figures.

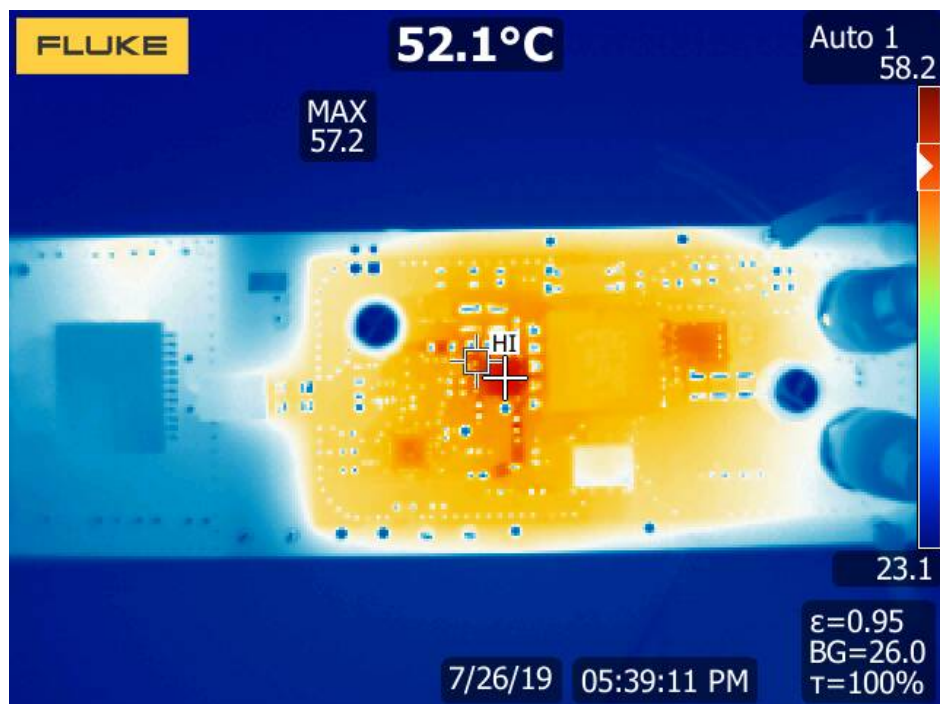


Figure 18.1. Si34061-EVB-EXT-5V Thermal Image at Full Load—Top Side

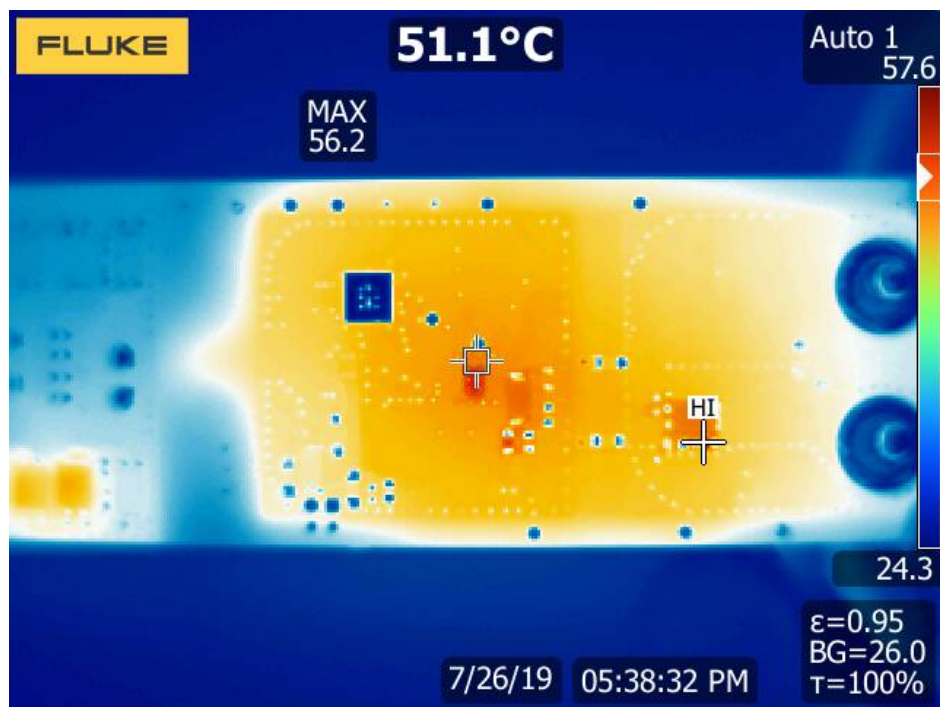


Figure 18.2. Si34061-EVB-EXT-5V Thermal Image at Full Load—Bottom Side

Note: Ambient temperature was 26 °C.

19. Layout

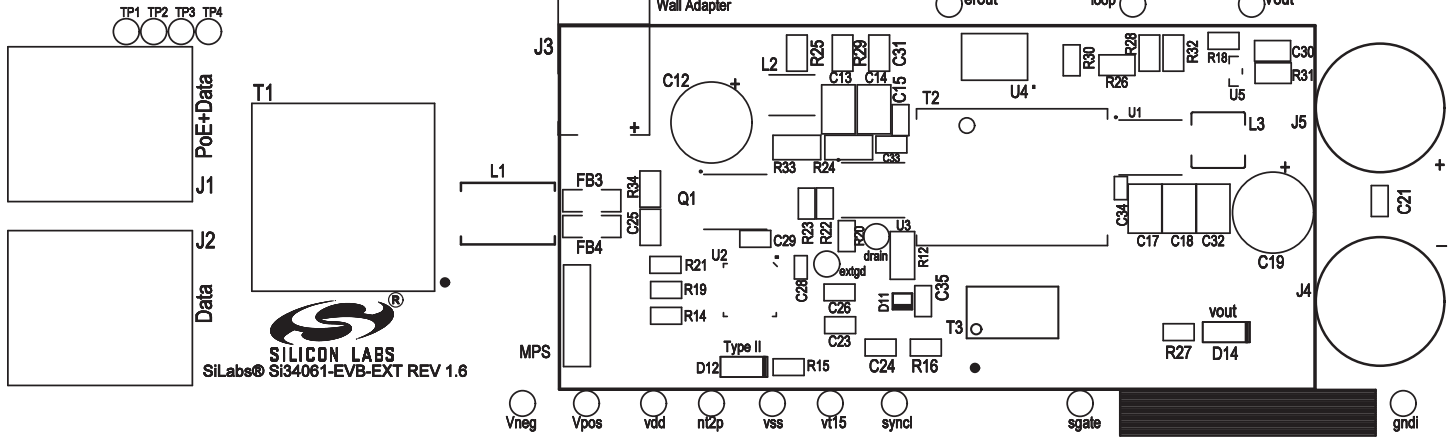


Figure 19.1. Primary Silkscreen

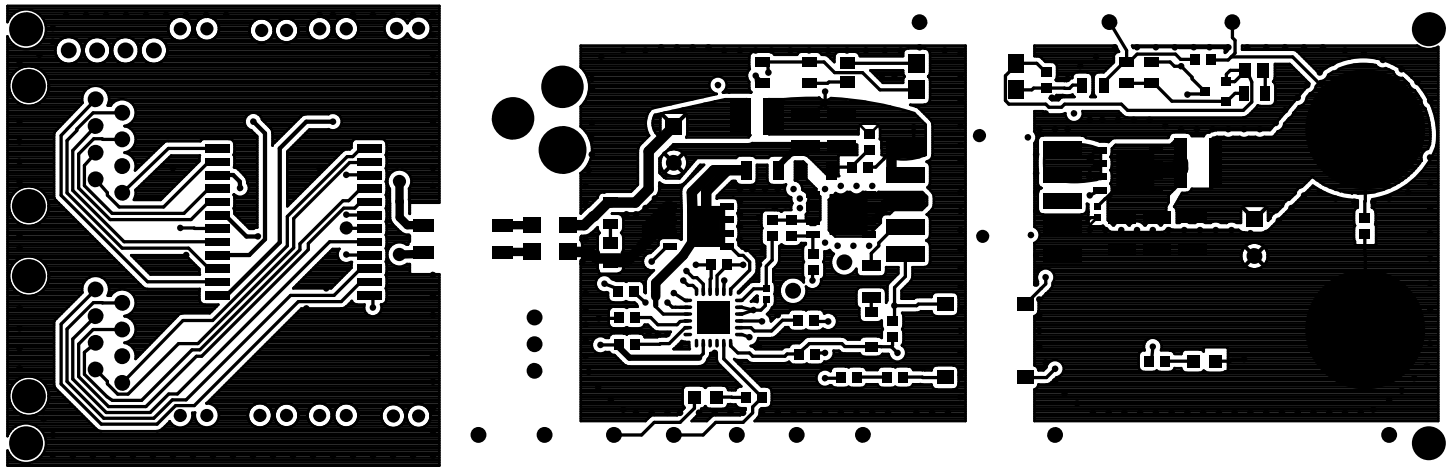


Figure 19.2. Top Layer

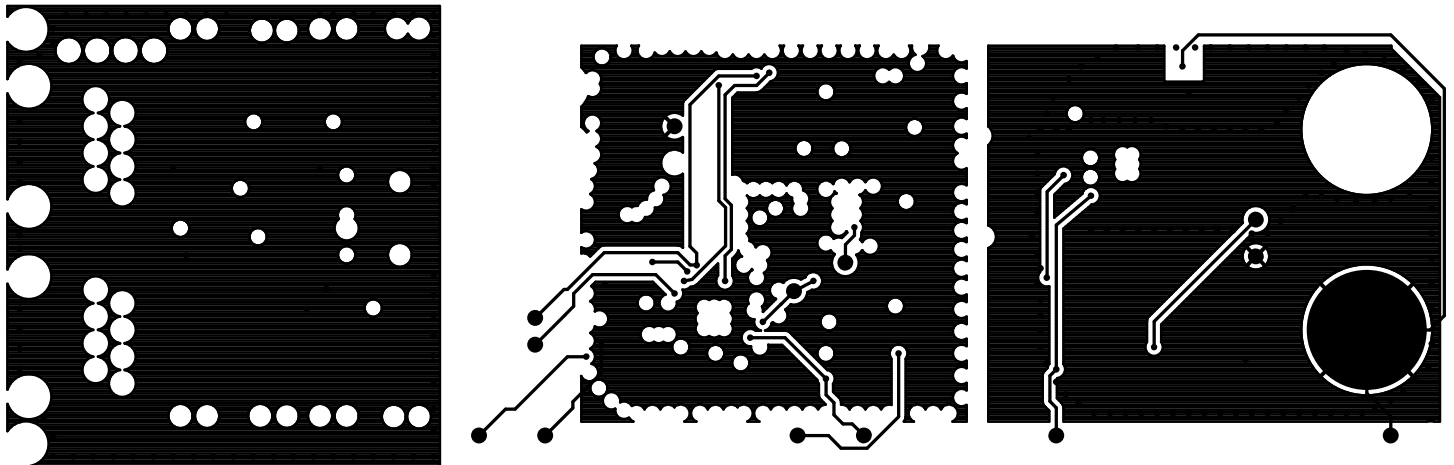


Figure 19.3. Internal 1 Layer

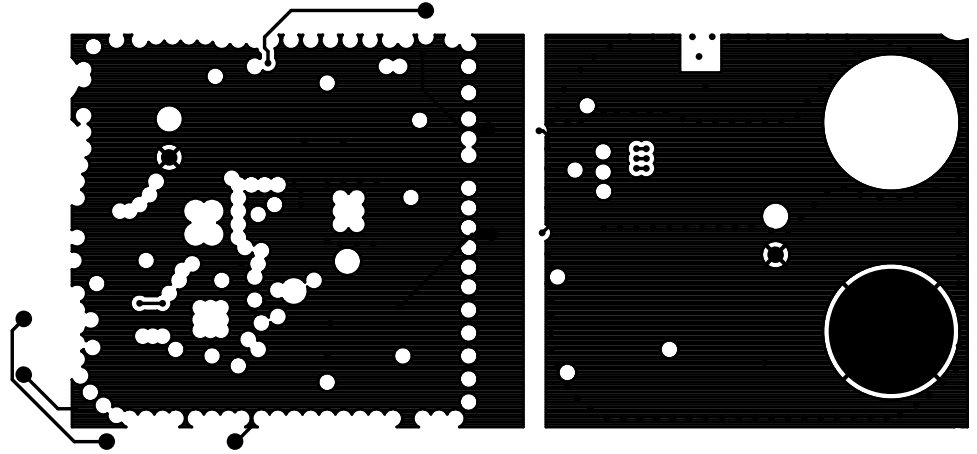
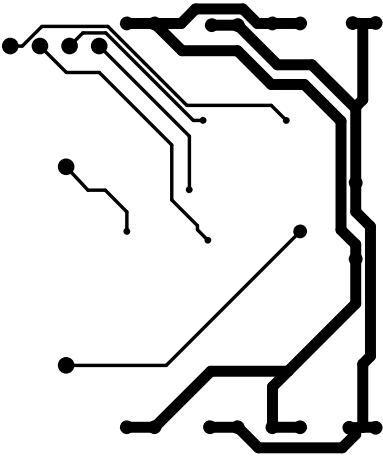


Figure 19.4. Internal 2 Layer

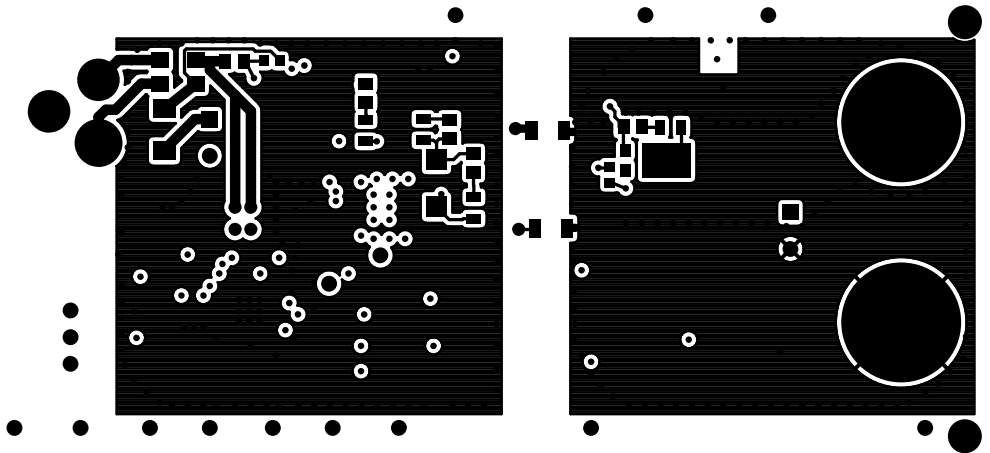
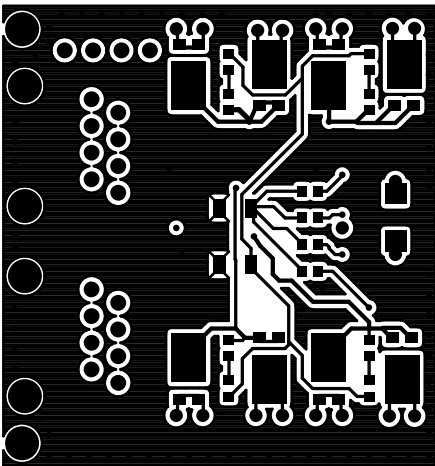


Figure 19.5. Bottom Layer

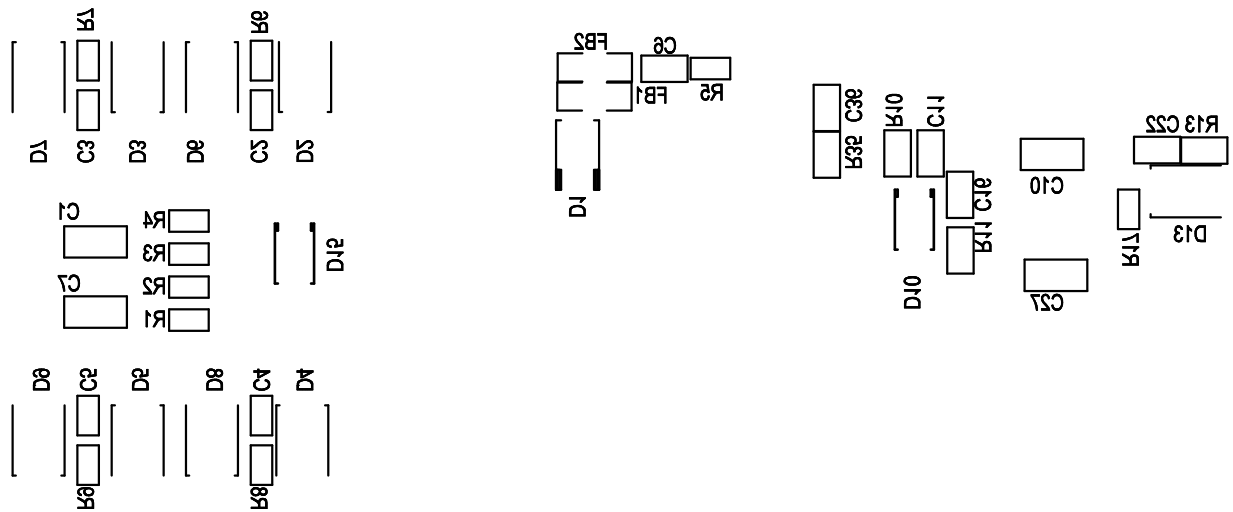


Figure 19.6. Bottom Silkscreen

20. Bill of Materials

Table 20.1. Bill of Materials Rev 1.7¹

Designator	Qty	Description	Mfr	Mfr Part Number
C1, C7, C10, C27	4	CAP, 1 nF, 2000 V, $\pm 5\%$, X7R, 1206	Kemet	C1206C102JGRACU
C12	1	CAP, 47 μ F, 100 V, $\pm 20\%$, AL, RAD	Panasonic	ECA2AM470
C13, C14	2	CAP, 1 μ F, 100 V, $\pm 10\%$, X7R, 1210	Venkel	C1210X7R101-105K
C15	1	CAP, 0.1 μ F, 100 V, $\pm 10\%$, X7R, 0603	Venkel	C0603X7R101-104K
C16	1	CAP, 100 pF, 200 V, $\pm 5\%$, NP0 HIGH Q, 0805	Venkel	C0805HQN201-101J
C17, C18, C32	3	CAP, 100 μ F, 6.3 V, $\pm 10\%$, X5R, 1210	Venkel	C1210X5R6R3-107K
C19	1	CAP, 1000 μ F, 6.3 V, $\pm 20\%$, AL, RAD	Panasonic	ECA0JM102
C2, C3, C4, C5, C33	5	CAP, 0.01 μ F, 100 V, $\pm 10\%$, X7R, 0603	Venkel	C0603X7R101-103K
C21	1	CAP, 0.022 μ F, 50 V, $\pm 20\%$, X7R, 0603	TDK Corporation	C1608X7R1H223M
C22	1	CAP, 3.3 nF, 50 V, $\pm 5\%$, X7R, 0805	Venkel	C0805X7R500-332JNE
C23	1	CAP, 1 μ F, 25 V, $\pm 10\%$, X5R, 0603	Venkel	C0603X5R250-105K
C24, C26	2	CAP, 220 nF, 16 V, $\pm 5\%$, X7R, 0603	Kemet	C0603C224J4RACTU
C25	1	CAP, 0.1 μ F, 100 V, $\pm 10\%$, X7R, 0805	Venkel	C0805X7R101-104K
C29	1	CAP, 0.1 μ F, 10 V, $\pm 10\%$, X7R, 0603	Venkel	C0603X7R100-104K
C30	1	CAP, 680 pF, 25 V, $\pm 1\%$, C0G, 0805	Venkel	C0805C0G250-681FNP
C31	1	CAP, 100 pF, 50 V, $\pm 1\%$, C0G, 0805	Venkel	C0805C0G500-101F
C34	1	CAP, 1.0 μ F, 6.3 V, $\pm 10\%$, X7R, 0402	Murata	GRM155R70J105KA12J
C35	1	CAP, 0.01 μ F, 25 V, $\pm 10\%$, X8R, 0603	KEMET	C0603C103K3HACAUTO
C6, C11	2	CAP, 0.01 μ F, 100 V, $\pm 10\%$, X7R, 0805	Venkel	C0805X7R101-103K
D1	1	DIO, Single, 100 V, 1.0 A, SMA	Fairchild	S1B
D10	1	DIO, Single, 100 V, 1.0 A, SMA	Fairchild	RS1B
D11	1	DIO, Fast, 100 V, 2 A, SOD123	Diodes Inc.	1N4148W
D12, D14	2	LED, Green, 0805	LITE_ON Inc.	LTST-C170GKT
D13	1	DIO, Schottky, 40 V, 10 A, PowerDI-5	Diodes Inc.	PDS1040-13
D2, D3, D4, D5, D6, D7, D8, D9	8	DIO, Schottky, 100 V, 5 A, PowerDI-5	Diodes Inc.	PDS5100H-13
FB1, FB2, FB3, FB4	4	Ferrite Bead, 600 Ω @ 100 MHz, 1206	Murata	BLM31PG601SN1
J1 J2	2	CONN, RJ-45, 1 Port, Tab Down, 0.050" Pitch, PTH	MOLEX	095501-2881
J3	1	CONN, Power JACK, RA, 2.1 mm, PTH	Adam Tech	ADC-002-1
J4, J5	2	CONN, Banana Jack, Threaded un-insulated	Abbatron HH Smith	101

Designator	Qty	Description	Mfr	Mfr Part Number
L1	1	CM Choke, 500 μ H, 1 A, 1 k Ω , SMT	Bourns	SRF0905-501Y
L2	1	Inductor, Power, 3.3 μ H, \pm 20%, 1.5 A, Unshielded	Murata	84332C
L3	1	Inductor, Power, Shielded, 0.16 μ H, 31 A, SMD	Coilcraft	XAL5030-161ME
LB1	1	Label, PDB, Polyimide, White, 1.00 in. X 0.187 in., FONT 2	Silicon Labs	Label-Si34061-EVB-EXT-BOM R1.7
MH1, MH2, MH3, MH4	4	HDW, Screw, 4-40 x 1/4 in. Pan Head, Slotted, Nylon	Richco Plastic Co.	NSS-4-4-01
PCB1	1	PCB, Bare Board, Si34061-EVB-EXT REV 1.6	Silicon Labs	Si34061-EVB-EXT REV 1.6
Q1	1	Transistor, MOSFET, N-CHNL, 100 V, 23 A, PowerPAK-SO-8	Vishay	SQJ476EP-T1_GE3
R1, R2, R3, R4, R6, R7, R8, R9	8	RES, 75 Ω , 1/16 W, \pm 0.5%, ThinFilm, 0603	Susumu	RR0816Q-750-D
R10	1	RES, 78.7 k Ω , 1/8 W, \pm 1%, ThickFilm, 0805	Yageo	RC0805FR-0778K7L
R11	1	RES, 100 Ω , 1/10 W, \pm 1%, ThickFilm, 0805	Venkel	CR0805-10W-1000F
R12	1	RES, 10 Ω , 1/4 W, \pm 1%, ThickFilm, 1206	Venkel	CR1206-4W-10R0F
R13, R34	2	RES, 3 Ω , 1/8 W, \pm 1%, ThickFilm, 0805	Venkel	CR0805-8W-3R00FT
R14	1	RES, 95.3 k Ω , 1/16 W, \pm 1%, Thick-Film, 0603	Venkel	CR0603-16W-9532F
R15, R27	2	RES, 1 k Ω , 1/10 W, \pm 1%, ThickFilm, 0603	Venkel	CR0603-10W-1001F
R16, R18	2	RES, 10 Ω , 1/16 W, \pm 1%, ThickFilm, 0603	Venkel	CR0603-16W-10R0F
R17, R22	2	RES, 24 k Ω , 1/10 W, \pm 1%, ThickFilm, 0603	Panasonic	ERJ-3EKF2402V
R19	1	RES, 33.2 Ω , 1/16 W, \pm 1%, ThickFilm, 0603	Venkel	CR0603-16W-33R2F
R20	1	RES, 23.7 Ω , 1/16 W, \pm 1%, ThickFilm, 0603	Venkel	CR0603-16W-23R7F
R21	1	RES, 24.9 k Ω , 1/10 W, \pm 1%, Thick-Film, 0603	Venkel	CR0603-10W-2492F
R23	1	RES, 0 Ω , 1 A, ThickFilm, 0603	Panasonic	ERJ-3GEY0R00V
R24	1	RES, 0.1 Ω , 1 W, \pm 1%, ThickFilm, 1206	Panasonic	ERJ-8BWFR100V
R25	1	RES, 3.24 k Ω , 1/8 W, \pm 1%, ThickFilm, 0805	Vishay	CRCW08053K24FKEA
R26	1	RES, 2.2 k Ω , 1/10 W, \pm 5%, ThickFilm, 0805	Venkel	CR0805-10W-222J
R28	1	RES, 36.5 k Ω , 1/10 W, \pm 1%, Thick-Film, 0805	Venkel	CR0805-10W-3652F

Designator	Qty	Description	Mfr	Mfr Part Number
R29, R31	2	RES, 0 Ω , 2 A, ThickFilm, 0805	Venkel	CR0805-10W-000
R32	1	RES, 12.1 k Ω , 1/10 W, $\pm 1\%$, Thick-Film, 0805	Venkel	CR0805-10W-1212F
R33	1	RES, 0.3 Ω , 1/2 W, $\pm 1\%$, ThickFilm, 1206	Venkel	LCR1206-R300F
R5	1	RES, 845 k Ω , 1/10 W, $\pm 1\%$, ThickFilm, 0603	Panasonic	ERJ-3EKF8453V
SO1, SO2, SO3, SO4	4	HDW, Standoff, 4-40 x 1/2", Nylon	SPC Technology	2397
SW1	1	Switch, SPDT, Slide, ON-ON, 0.1 Pitch, 12 V, PTH	Apem Inc.	NK236H
T1	1	Module, PoE+/PoE++ Magnetics, PULSE XFMR 1CT:1CT TX 1CT:1CT RX, SMD	Würth	7490220121
T2	1	Transformer, Flyback, 30 W, 5 V, SMD	LinkCom	LDT1020-51R
T3	1	Gate XFMR, 1:1, 1500 Vrms, 1200 μ H, 27.2 V μ sec	Pulse Engineering	PA0184NL
TP5, TP6	2	Testpoint, Red, 0.050 in. LOOP, PT	Keystone	5000
TP8, TP9, TP10, TP12, TP15, TP18, TP19	7	Testpoint, Black, 0.050" LOOP, PT	Keystone	5001
U1	1	Transistor, MOSFET, N-CHNL, 40 V, 40 A, PowerPAK-SO-8	Vishay	SiR422DP-T1-GE3
U2	1	IC, IEEE 802.3-Compliant POE+ PD Interface, QFN24	Silicon Labs	Si34061
U3	1	Transistor, MOSFET, N-CHNL, 150 V, 29 A, PowerPAK-SO-8	Vishay	SIR632DP-T1-RE3
U4	1	Photocoupler, 5300 Vrms Isolation, 4-PIN SMD	Vishay	VO618A-3X017T
U5	1	IC, ADJ PREC SHUNT REG LV SOT-23 Voltage-Output 1.24 ~ 6 V	TI	TLV431BCDBZR
Not Installed Components				
C28	1	CAP, 470 pF, 25 V, $\pm 20\%$, X7R, 0402	Venkel	C0402X7R250-471M
C36	1	CAP, 0.01 μ F, 100 V, $\pm 10\%$, X7R, 0805	Venkel	C0805X7R101-103K
D15	1	DIO, TVS, UNIDIR, 58 V, 400 W	Littelfuse	SMAJ58A
R30	1	RES, 1 k Ω , $\pm 1\%$, ThickFilm, 0603	Venkel	CR0603-10W-1001F
R35	1	RES, 100 Ω , $\pm 1\%$, ThickFilm, 0805	Venkel	CR0805-10W-1000F
TP1, TP2, TP3, TP4	4	Testpoint, Black, PTH	Kobiconn	151-203-RC
TP7, TP11, TP14, TP16, TP17	5	Testpoint, Black, 0.050" LOOP, PTH	Keystone	5001
Note:				
1. The PCB is Rev 1.6, and the Bill of Materials is Rev 1.7.				

21. Design and Layout Checklist

The complete EVB design databases are located at www.silabs.com/PoE link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

The following is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the Si34061 data sheet and [AN1130: Si3404/06x PoE-PD Controller Design Guide](#) when using the following checklist.

1. Design Planning checklist:

- a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
- b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si34061-EVB-EXT into your system design process.
- c. Determine your load's power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions).
- d. Based on your required PD power level, select the appropriate class resistor RCLASS value by referring to AN1130.

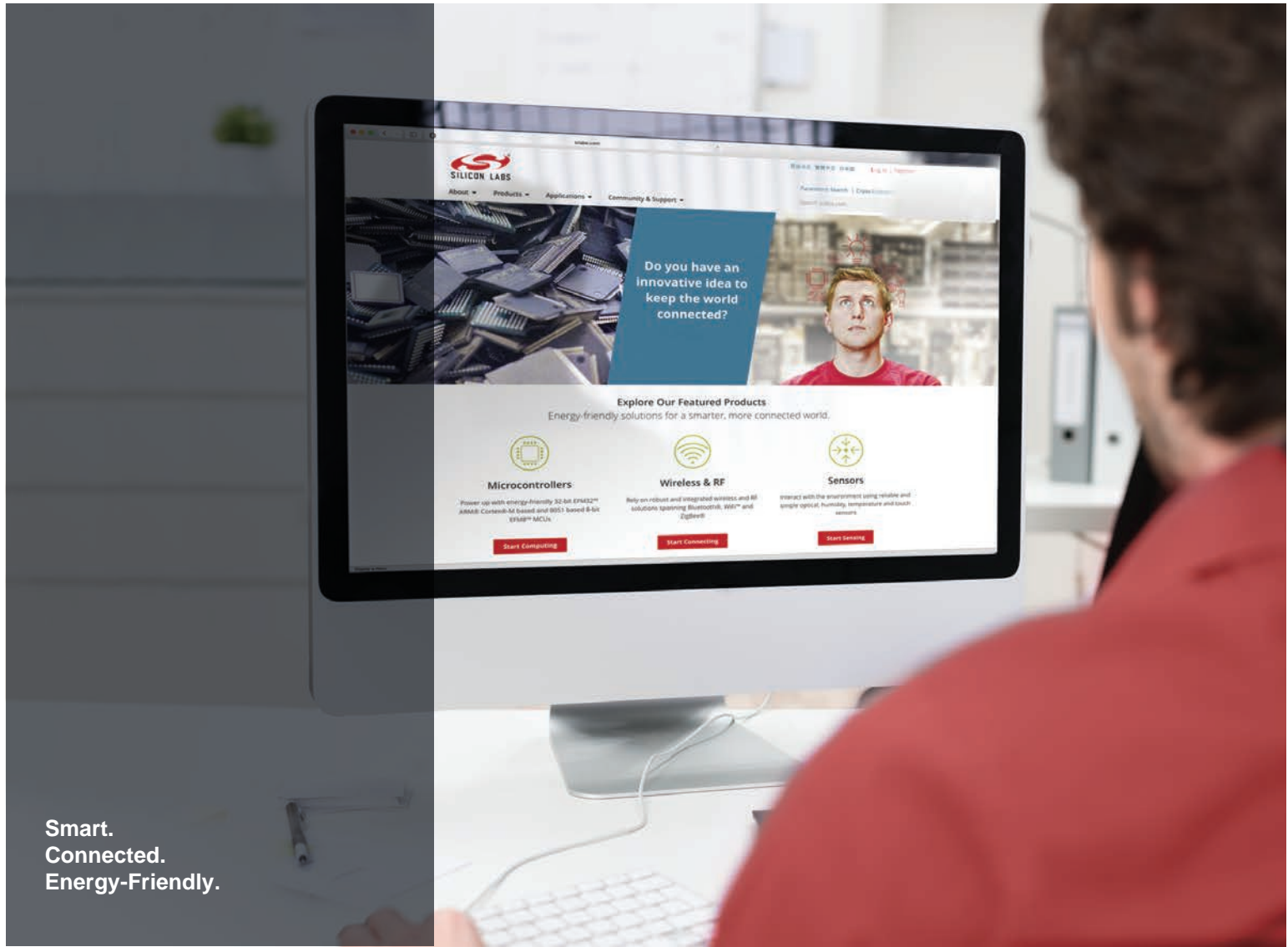
2. General Design Checklist:

- a. Non-standard PoE injectors turns on the PD without detection and classification phases. In most cases, dV/dt is not controlled and could violate IEEE requirements. To ensure robustness with those injectors, please include a 3Ω resistors in place of R34.

3. Layout Guidelines:

- a. Make sure VNEG pin of the Si34061 is connected to the backside of the QFN package with an **adequate thermal plane**, as noted in the data sheet and AN1130.
- b. Keep the trace length from the switching FET to VSS as short as possible. Make all the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
- c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
- d. Keep the circular area of the loop from the switching FET to the transformer and returning from the input filter capacitors (C13, C14, C15) to VSS as small a diameter as possible. Also, minimize the circular area of the loop from the output of the transformer to the syncFET (U1) and returning through the output filter capacitor back to the transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.
- e. Keep the high-power traces as short as possible.
- f. Keep the feedback and loop stability components as far from the transformer and noisy power traces as possible.
- g. If the output has a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

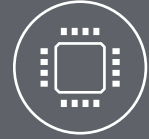
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