Si34071 Data Sheet

The Si34071 integrates the signaling, control, and power conversion functions required in a Power over Ethernet 802.3bt-powered device (PD) application.

The optimized architecture minimizes the solution footprint and external BOM while using standard, low cost components. The integrated PoE PD interface fully complies with the IEEE 802.3bt standard and uses external resistors to program the requested classification and detection signatures. Connection to the PSE switch is maintained during no-load condition by an optional maintain-power-signature (MPS) signal. An internal, current-mode controlled switching regulator converts the high voltage supplied over the 10/100/1000BASE-T Ethernet connection to a regulated, low-voltage output supply. The switching regulator supports isolated flyback and forward converter topologies. An external resistor tunes the switching frequency. High efficiency features include a main transformer bias winding input and a synchronous gate driver for secondary side FET control, or active clamp, depending on the topology.

The Si34071 is available in a low-profile, 32-pin, 5 x 5 mm QFN package.

KEY FEATURES

- Full IEEE 802.3bt compliance
- Synchronous FET or Active clamp driver
- Peak current mode dc-dc converter
- Tunable switching frequency
- Auxiliary transformer winding support
- Maintain-power-signature (MPS) support
- UART interface to system controller
- Autoclass support
- –40 to +85 °C temperature
- Compact ROHS-compliant 5 mm x 5 mm QFN Package

APPLICATIONS

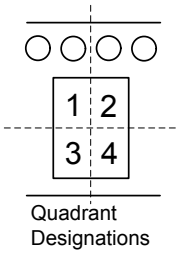
- Voice over IP telephones
- Wireless access points
- Security and surveillance IP cameras
- Lighting luminaires
- Point-of-sale terminals
- Internet appliances
- Network devices

1. Ordering Guide

Table 1.1. Si34071 Ordering Guide

Ordering Part Number[1]	Package[2]	Temperature Range (Ambient)	Applications
Si34071-A01-GM	5 x 5 mm 32-QFN Pb-free, RoHS-compliant	–40 to 85 °C	All Purposes

1. Add an “R” to the end of the part number for tape and reel option (e.g., Si34071-A01-GM or Si34071-A01-GMR).
2. Pin 1 is oriented in Quadrant 1 in the tape:



Quadrant Designations

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2. System Overview

The following block diagrams will give the designer a sense for the internal arrangement of functional blocks, plus their relationships to external pins. The block diagrams are followed by a description of the features of these integrated circuits.

2.1 Block Diagram

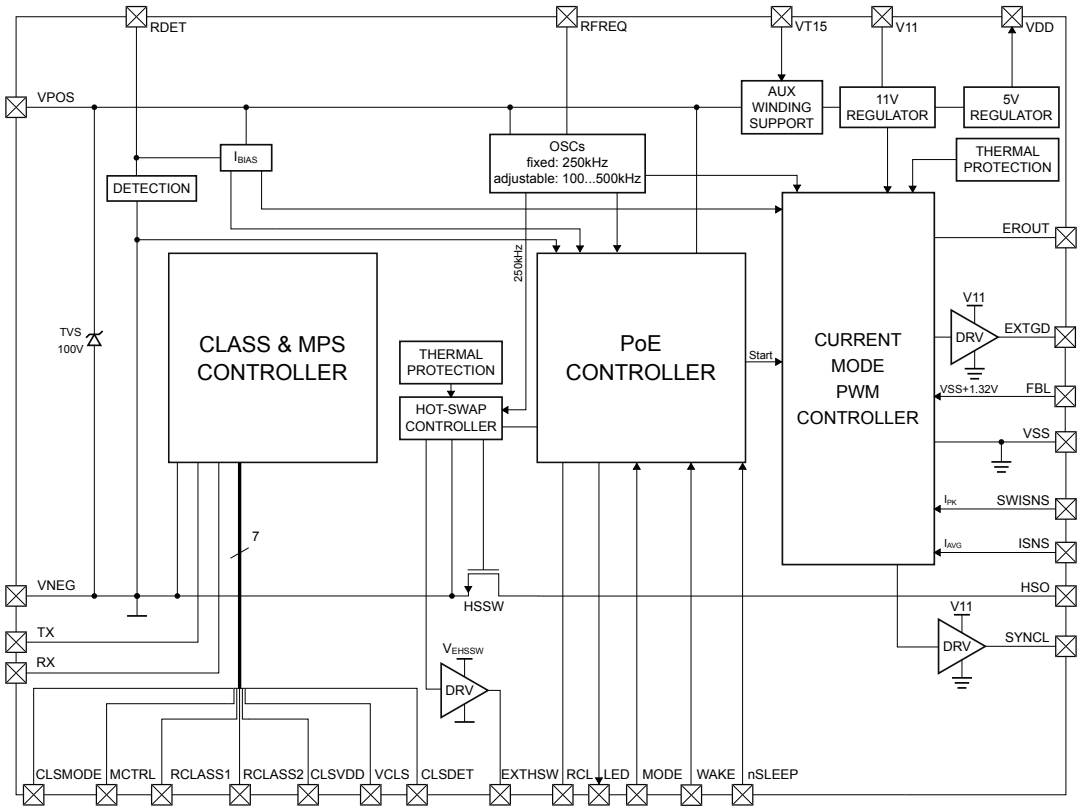


Figure 2.1. Si34071 Block Diagram

2.2 Power over Ethernet (PoE) Line-Side Interface

The PoE line interface consists of internal surge protection and the protocol interface support for detection, mark, and classification. The chip features active protection against surge transients and accidentally applied telephony voltages.

The Si34071 supports external diode bridges using standard diodes. For higher efficiency, Schottky diodes are recommended. Instead of a diode bridge, a MOSFET-based bridge can be used as well to further improve the overall efficiency.

The Si34071 uses an external classification BOM controlled by the Si34071 PoE interface controller to provide the PSE with detect and classification signatures compliant to IEEE 802.3bt specifications. See 2.3 External Classification BOM for more information.

2.2.1 Surge Protection

The surge protection circuit is activated if the VPOS-VNEG voltage exceeds V_{PROT} *and* the hotswap switch is off (dc-dc is not powered). If the hotswap switch is on, the surge power is sunk in the dc-dc input capacitance.

The internal surge protection can be augmented with an external TVS if higher than specified surge conditions need to be tolerated. The external surge device must be connected between VPOS and VNEG in parallel to the internal one; therefore, the designer must ensure that the external surge protection will activate prior to the internal surge protection.

2.2.2 Telephony Protection

The Si34071 provides protection against telephony ringing voltage. The telephony ringing is much longer than the surge pulse but it has less energy, therefore, the Si34071 has a switch in parallel with the supply (between VPOS and VNEG). When the protection circuit is activated, it turns ON the protection switch; the ringing energy then dissipates on this switch and ringing generator resistance (> 400 Ω).

2.2.3 Maximum Power Available at PD Input

Once power has been applied, the system controller is responsible for querying the Si34071 to determine the class granted by the PSE and the maximum available input power. The Si34071 UART interface provides information about the class granted by the PSE. See 2.10 UART Interface for more details.

2.3 External Classification BOM

The Si34071 is fully 802.3bt-compliant and supports powering from 802.3af, 802.3at, and 802.3bt PSEs. IEEE 802.3bt-compliant PDs are backwards compatible with 802.3af and 802.3at PSEs. However, the maximum class will be limited to Class 4 (25.5 W) when connected to an 802.3at PSE and Class 3 (13 W) when connected to an 802.3af PSE.

An 802.3bt-compliant PSE will produce up to 5 classification pulses of approximately 18 V with each pulse separated by a mark period of approximately 8.5 V. The Si34071 uses external resistors to produce a classification signature of approximately 40 mA for the first and second classification pulses indicating a request for Class 4 power. Subsequent classification pulses will be at lower currents according to the classification level configured by the external resistors (Class 5 to Class 8). After power on, the system controller must query the Si34071 to determine the classification result and adjust the system power level accordingly. This is to account for potential power demotion situations in which the PD is not granted the full power requested.

IEEE 802.3bt-compliant PDs must support power demotion and may optionally support Autoclass. The Si34071 supports both features.

Classification demotion requires the PD system to recognize the power level being granted by the PSE and adjust the system power to be consistent with the power granted. For example, in a wireless access point the radio output power may need to be reduced to match the power granted by the PSE.

Autoclass enables the PSE to measure the maximum power consumption by a PD and allocate power accordingly. This feature is optional and both the PSE and PD must support autoclass for the feature to be enabled. An autoclass enabled PSE puts out a long first classification pulse and the PD reduces the classification signature to Class 0 at approximately 81 ms after the start of classification. An autoclass enabled PD has 1.35 seconds after inrush to enter its maximum power state. Maximum power consumption must be maintained for at least 3.65 seconds after the inrush period so the PSE can measure the actual consumption of the PD and adjust the power allocation accordingly. After this time the PD can either enter a lower power state or continue drawing maximum power. The PSE will then adjust its policing threshold such that the PD will not be allowed to draw more power than the power levels consumed during this period, with some margin.

The Si34071 uses internal signaling combined with an external classification BOM to generate the necessary IEEE 802.3bt detection and classification signatures. The Si34071 can be configured to request Class 4–8 and autoclass from the PSE by setting the voltage on the CLSMODE pin using external resistors and adjusting the values of R_{CLASS1} and R_{CLASS2} in the classification BOM. The values of R_{CLASS1} and R_{CLASS2} must be adjusted to match the classification set by the CLSMODE pin. The figure below shows the schematic for the external classification BOM and Table 2.2 External Classification BOM on page 8 lists the recommended values and component types. See "AN1179: Si34071 802.3bt PD PoE Interface" for further details on the classification BOM and selecting alternate components.

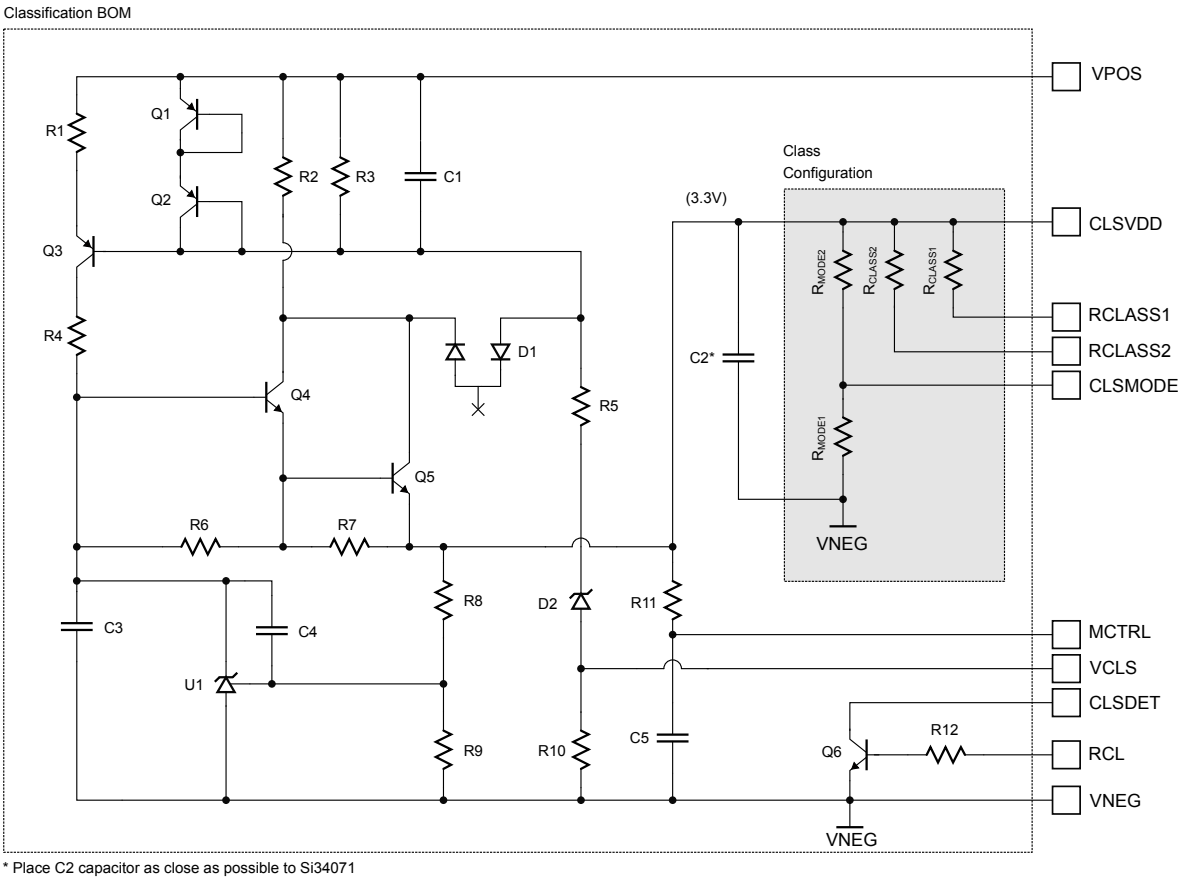


Figure 2.2. External Classification BOM Schematic

Table 2.1. Voltages to Configure Requested Class and Autoclass

Class	Autoclass	CLSMODE Pin Voltage	R_{MODE1}[1]	R_{MODE2}[1]	R_{CLASS1}[2]	R_{CLASS2}[2]
4	No	0.1618 V	6.8 kΩ	130 kΩ	169 Ω	169 Ω
5		0.4918 V	16 kΩ	91 kΩ	169 Ω	169 Ω
6		0.8218 V	30 kΩ	91 kΩ	98 Ω	492 Ω
7		1.1518 V	33 kΩ	62 kΩ	138 Ω	215 Ω
8		1.4818 V	39 kΩ	47 kΩ	258 Ω	125 Ω
4	Yes	1.8182 V	47 kΩ	39 kΩ	169 Ω	169 Ω
5		2.1482 V	82 kΩ	43 kΩ	169 Ω	169 Ω
6		2.4782 V	91 kΩ	30 kΩ	98 Ω	492 Ω
7		2.8082 V	130 kΩ	22 kΩ	138 Ω	215 Ω
8		3.1382 V	200 kΩ	10 kΩ	258 Ω	125 Ω

Note:

1. The CLSMODE pin voltage configures the Si34071 and the values listed for R_{MODE1} and R_{MODE2} are example values. Any resistor values that achieve the listed CLSMODE pin voltage may be used.
2. R_{CLASS1} and R_{CLASS2} are used to generate the correct classification current signatures and the listed values for R_{CLASS1} and R_{CLASS2} must be used.

Table 2.2. External Classification BOM

Reference	Value	Rating	Voltage	Tolerance	Type	PCB Footprint	Manufacturer Part Number	Manufacturer
C1, C3	0.01 µF		100 V	±10%	X7R	C0603	C0603X7R101-103K	Venkel
C2	0.1 µF		25 V	±10%	X7R	C0603	C0603X7R250-104K	Venkel
C4	1 nF		100 V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
C5	47 pF		100 V	±10%	X7R	C0603	C0603X7R101-470K	Venkel
D1	BAV99	300 mA	100 V		Dual, Switch	SOT23-AKC	BAV99-7-F	Diodes Inc.
D2	10 V	500 mW	10 V	5%	Zener	SOD-123	MMSZ4697T1G	On Semi
Q1, Q2, Q3	MMBTA56L	500 mA	-80 V		PNP	SOT23-BEC	MMBTA56L	On Semi
Q4, Q5, Q6	MMBTA06LT1	500 mA	80 V		NPN	SOT23-BEC	MMBTA06LT1	On Semi
R1	3.65 kΩ	1/16 W		±1%	ThickFilm	R0603	CR0603-16W-3651FT	Venkel
R10	1.20 kΩ	1/10 W		±1%	ThickFilm	R0603	CR0603-10W-1201F	Venkel
R11	100 kΩ	1/16 W		±5%	ThickFilm	R0603	CR0603-16W-104J	Venkel
R12	10 kΩ	1/16 W		±1%	ThickFilm	R0603	CR0603-16W-1002F	Venkel
R2, R4	20.0 kΩ	1/16 W		±1%	ThickFilm	R0603	CR0603-16W-2002F	Venkel
R3, R5	100 kΩ	1/10 W		±1%	ThickFilm	R0603	CR0603-10W-1003F	Venkel
R6, R7	49.9 kΩ	1/10 W		±1%	ThickFilm	R0603	CR0603-10W-4992F	Venkel
R8	41.2 kΩ	1/10 W		±1%	ThickFilm	R0603	CR0603-10W-4122F	Venkel
R9	24.9 kΩ	1/10 W		±1%	ThickFilm	R0603	CR0603-10W-2492F	Venkel
U1	TLV431				SHUNT	TLV431-DBZ	TLV431BCDBZR	TI

2.4 Hotswap Switch

The hotswap switch (HSSW) is a high-voltage device that separates the PoE interface from the dc-dc converter domain. The Si34071 has an internal hotswap FET and a driver for an external hotswap FET. Based on the average input current, the HSSW controller decides whether the internal or external HSSW will conduct. An external FET must be used with the Si34071 to reduce thermal dissipation on the integrated HSSW and improve overall conversion efficiency at high power. The external HSSW must be an NMOS type FET connected directly to the EXTHSW pin, between VNEG and HSO. As shown in the figure below, the added FET will be in parallel with the internal HSSW. Both FETs will be operational, but their loading will be tightly controlled by the HSSW controller. The EXTHSW driver controls the external FET with 10 V logic level relative to VNEG.

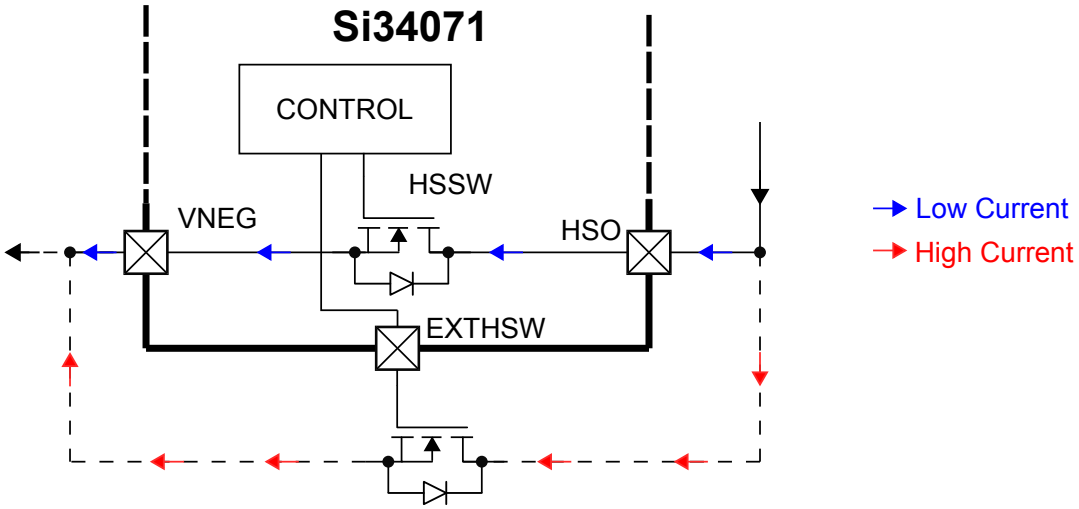


Figure 2.3. Si34071 Hotswap Switch Architecture

The HSSW controller turns on the HSSW when the PoE interface voltage goes above V_{UVLO_R}. The HSSW controller also limits inrush current until the dc-dc side capacitor is charged. If voltage on the HSSW (HSO-VNEG) is greater than V_{HSSW_OFF}, the HSSW controller opens the HSSW.

In overload, the HSSW controller goes into current-limiting mode with a current limit of I_{OVL}. It will turn the HSSW back ON after $T_{WAITHSSW}$ elapses and the dc-dc input capacitor is recharged, with the HSO-VNEG voltage less than V_{HSSW_ON}

2.5 HSSW State Machine

The HSSW operates as a simple, 4-state, state machine. In the following figure, the red labels, S1–S4, indicate the states of the HSSW state machine.

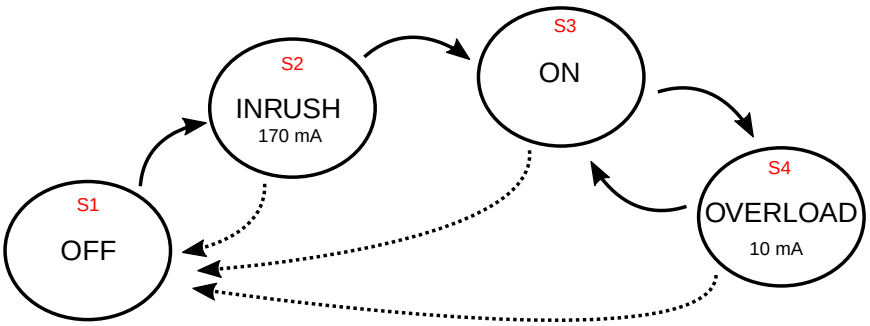


Figure 2.4. Hotswap Switch 4-State Machine

OFF State

HSSW turn-on is controlled by UVLO, the undervoltage lockout feature. When UVLO is engaged, the HSSW is OFF. In this state, the HSSW is in idle mode, VNEG and HSO pins are disconnected. In normal operation, a complete detect/classification procedure precedes the HSSW turn-on, and the control of this sequence is implemented in the state machine logic of the chip.

INRUSH State

After the controller enables the HSSW, the block starts operation in the INRUSH state. In this state the switch itself is not directly turned on, but operating in a closed-loop current limit mode to avoid high current peaks during the charging of the input capacitor of the dc-dc converter.

If the V_{HSSW} voltage drops below 380 mV (meaning the bypass cap is 99% charged), the HSSW will change state to ON either in Type 1 classification immediately, or in Type 2, 3, or 4 classification if the HSSW has been in the INRUSH state for at least 80 ms.

ON State

In ON state, the HSSW switch is completely turned on. The HSSW circuit continuously monitors V_{HSSW}. HSSW will change to OVERLOAD state if V_{HSSW} voltage increases over 3.5 V for at least 140 µs.

OVERLOAD State

In OVERLOAD state the HSSW operates in closed-loop low current limit mode. If the V_{HSSW} voltage drops below 380 mV again, and the HSSW has been in the OVERLOAD state for at least 80 ms, the HSSW will change back to the ON state.

2.6 DC-DC Converter

The dc-dc converter is current-controlled for easier compensation and more robust protection of circuit magnetics. The controller has the following features:

- Supports flyback and forward topologies
- Complementary FET driver
- Overcurrent detection
- Low current detection
- Cycle skipping at low current and short circuit conditions
- Automatic non-overlap control

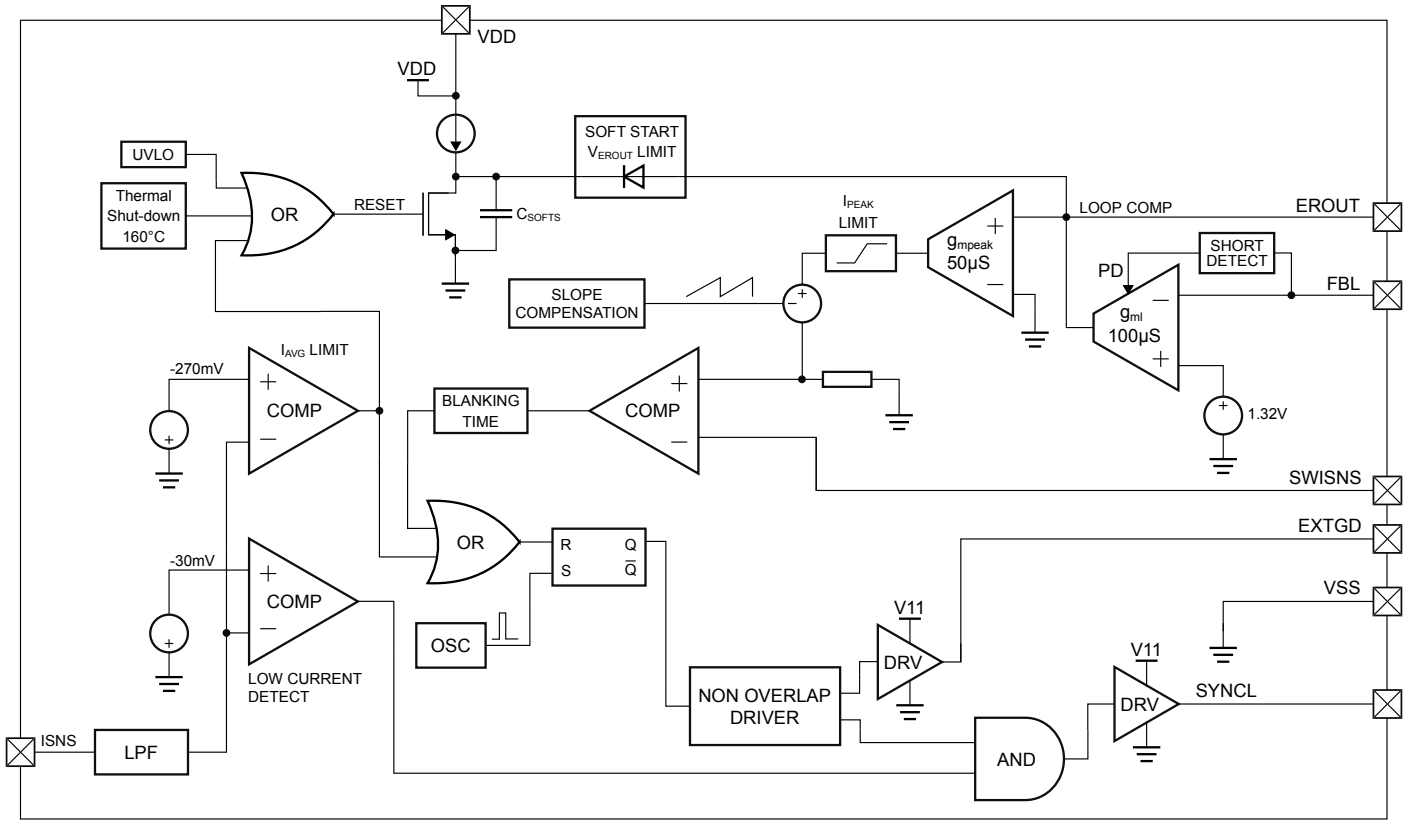


Figure 2.5. Si34071 DC-DC Converter Block Diagram

The Si34071 uses an external current sense resistor to measure the peak current connected to the SWISNS pin. Changing this resistor allows the application to set the converter maximum primary peak current to protect the magnetic components (like the transformer) from saturation.

Feedback to the dc-dc converter can be provided to the EROUT pin by a voltage to current converter (isolated flyback, forward).

The loop compensation impedance is connected to EROUT. The active voltage range is V_{EROUT}, which is proportional to the converter peak current.

The converter start time is not configurable; soft start is accomplished by internal circuitry. Soft start time is $T_{SOFTSTART}$. The intelligent soft start circuit dynamically adjusts the soft start time depending on the connected load.

2.6.1 Average Current Sensing, Overcurrent, Low-Current Detection, and Output Short Protection

The application average current is sensed by an external resistor (R_{SENSE}) connected between VSS and ISNS. Overcurrent is detected and triggered when the voltage on the sense resistor exceeds V_{ISNS_OVC}. Sizing the resistor allows the designer to set the overcurrent limit according to application needs. When overcurrent is triggered, the dc-dc controller goes into reset until the overcurrent resolves. When the overcurrent is no longer present, the controller starts up again with soft start.

This external sense resistor is also used to detect a low current situation. When the voltage on the sense resistor goes below V_{ISNS_LC}, the dc-dc controller disables the driver on the SYCNL pin allowing low current consumption—the internal hotswap switch then measures the chip current internally.

The Si34071 integrates output short protection. When the output is shorted, the average input current remains in the normal operating range; therefore, the PSE will not disconnect the PD. When the output is shorted for more than 1 ms, the controller detects a high EROUT signal, resets the dc-dc controller, and a new startup cycle with soft-start turn ON follows.

2.6.2 SYNCL Complementary FET Driver

Depending on the topology (flyback or forward), the SYNCL pin can be used as a synchronous rectification driver in flyback or as an active clamp driver in forward.

If SYNCL is not used in the design, do not connect to any power ground, it should be left open. The SYNCL driver is disabled when the dc-dc converter measures low average current (meaning lower than V_{ISNS_LC} on ISNS). This ensures low current consumption in flyback topologies.

In flyback topology, when the controller is in low-power mode (SYNCL is not switching), the rectification is done by a body-diode of the synchronous-FET.

In active-clamp forward topology, when the controller is in low-power mode (SYNCL is not switching), the transformer's reset winding, in series with a reset diode, ensure proper operation.

2.7 Tunable Oscillator

The dc-dc frequency can be fixed to 250 kHz or tunable by an external resistor.

The tuning resistor must be connected between the RFREQ pin and VPOS. If RFREQ is shorted to VPOS, the fixed frequency oscillator will provide the clock, F_{OSCINT}, to the dc-dc converter; otherwise, the resistor will determine the frequency as shown in the curve below.

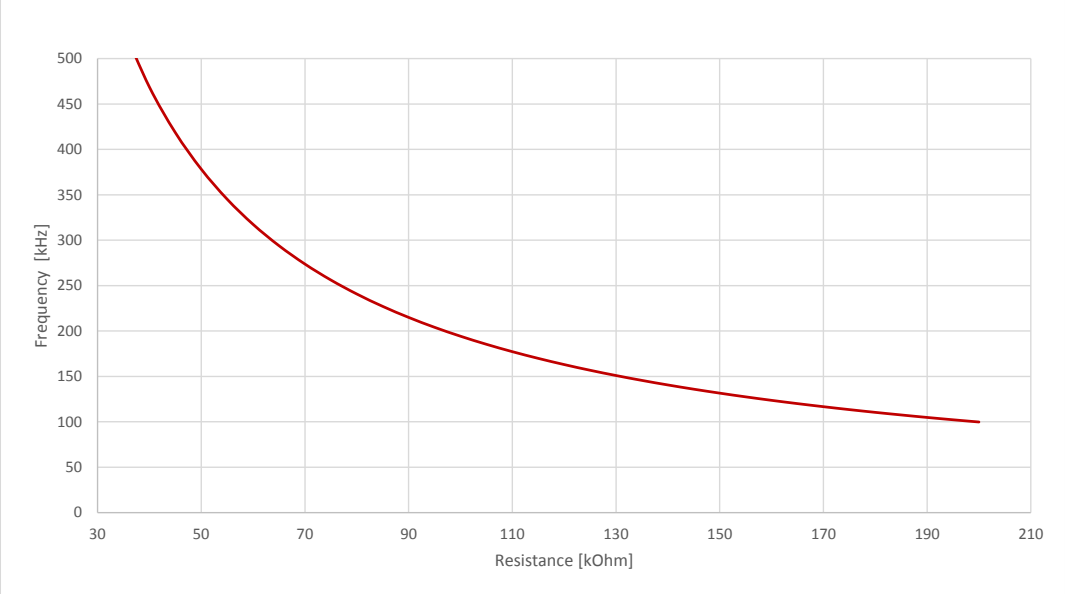


Figure 2.6. RFREQ Frequency Selector Diagram

2.8 Regulators

The chip provides a 5 V output to power LEDs or optocouplers. This is a closed-loop regulator, which ensures accurate output voltage. The 5 V regulator is supplied by an internal 11 V open loop regulator, which also provides power for the external FET gate drivers. The 11 V regulator is supplied by a coarse regulator, which is also open-loop. With the Si34071, the VT15 pin can be used to supply this regulator from an optional auxiliary transformer winding. The advantage of doing so is additional power saving since the external FET drivers' current is not generated from the PoE 50 V but, rather, from a transformer-provided 12–16.5 V. The application must be designed to ensure that the absolute maximum rating voltage for the VT15 pin is not exceeded.

2.9 Maintain Power Signature

The Si34071 is capable of generating IEEE 802.3af/at (long) or IEEE 802.3bt (short) maintain power signature (MPS) pulses to maintain the connection with the PSE when the system is in a low-power state. The PSE will remove power from the PD if the total application current consumption is between 4-9 mA for Class 1–4 two-pair power, 4–10 mA for Class 1–4 four-pair power, and 4–14 mA for Class 5–8 four-pair power. The MPS pulse generation is not automatic. A UART command from the system controller enables Si34071 MPS pulse generation. Once MPS generation is enabled, the Si34071 automatically selects short or long MPS pulses based on which type the PSE supports. The Si34071 generates MPS pulses by pulling the TX pin high and low. The value of R_{MPS} determines the current draw from the MPS pulses. See 2.10 UART Interface for more information on the UART interface and list of commands.

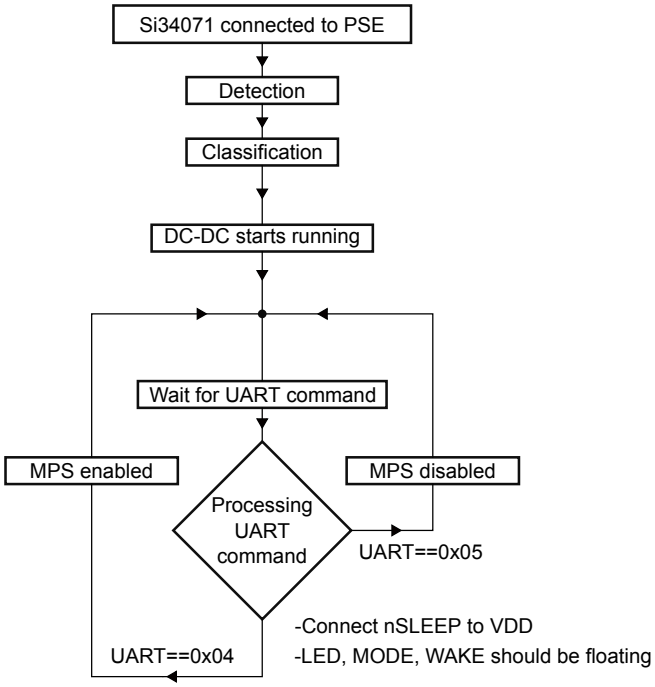


Figure 2.7. Si34071 MPS State Diagram

2.10 UART Interface

The Si34071 includes an asynchronous, full duplex UART port for interfacing with the system controller. The UART port baud rate is fixed at 9600 bps and cannot be changed. A total of 10 bits are used per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX pin and received at the RX pin.

The Si34071 uses a simple command interface. A command is written to the Si34071 using the UART port and the Si34071 will execute the command and, if required, respond with the corresponding data. The system controller must wait until the Si34071 has finished sending the response to a command before writing another command. For example, to determine the class received from the PSE simply write the command 0x01 to the Si34071. The Si34071 will respond with a byte of data containing the class received from the PSE during classification. The system controller must wait until the Si34071 has completely written the response byte before sending another command. See Table 2.3 for a complete list of Si34071 commands and their responses.

The Si34071 uses the UART TX pin to generate MPS pulses by pulling the pin high and low. R_{MPS} enables the Si34071 to consume enough current to maintain the connection to the PSE. After sending the enable MPS command (0x04) the system controller should disregard all data received from the Si34071 until the disable MPS command has been sent (0x05). After receiving the disable MPS command (0x05), the Si34071 resumes normal UART operation on the TX and RX pins.

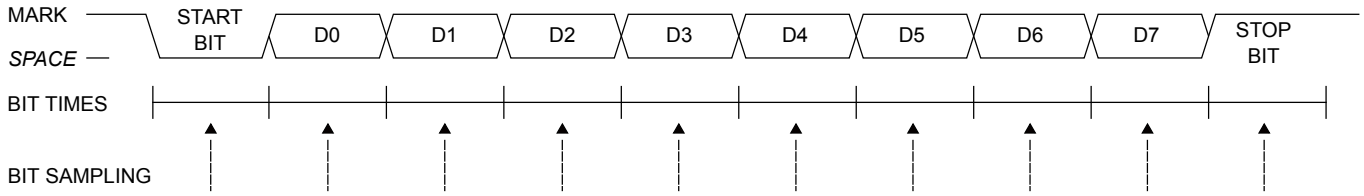


Figure 2.8. UART Interconnect Diagram

Table 2.3. Si34071 UART Interface Baud Rate

Parameter	Min	Typ	Max	Unit
Baud	9433	9630	9827	bps

Table 2.4. Si34071 Command Interface

Command	Name	Type	Description
0x01	CLASS	R	Class requested and class assigned
0x02	STATUS	R	Class pulses detected and PSE MPS support
0x03	VPWR	R	Input voltage to Si34071
0x04	MPS_ON	W	Enable MPS pulse generation
0x05	MPS_OFF	W	Disable MPS pulse generation

Table 2.5. CLASS Command

Command	Bit Position							
0x01	7	6	5	4	3	2	1	0
Access	R				R			
	CLASS_REQUESTED				CLASS_RECEIVED			

Bit	Name	Access	Description
7:4	CLASS_REQUESTED	R	Binary value for class requested by Si34071
3:0	CLASS_RECEIVED	R	Binary value for class granted by PSE to Si34071
Note: The CLASS command typically takes 4ms to complete, including time for the Si34071 to receive the command (one byte of data), process the command, and complete sending the one byte response.			

Table 2.6. STATUS Command

Command	Bit Position							
0x02	7	6	5	4	3	2	1	0
Access			R	R		R		
			MPS_TYPE	AUTOCLASS		CLS_PULSES		

Bit	Name	Access	Description
7:6	Reserved		Si34071 sets these bits to 0
5	MPS_TYPE	R	MPS type supported by PSE: 0 = long MPS, 1 = short MPS
4	AUTOCLASS	R	Si34071 sets this bit to 1 if it is configured to request autoclass from the PSE.
3	Reserved		Si34071 sets this bit to 0
2:0	CLS_PULSES	R	CLS pulses: number of CLS pul- ses seen during classification
Note: The STATUS command typically takes 4ms to complete, including time for the Si34071 to receive the command (one byte of data), process the command, and complete sending the one byte response.			

Table 2.7. VPWR Command

Command	Bit Position - Byte 1								Bit Position - Byte 2							
0x03	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	R								R							
	MSB_VPWR								LSB_VPWR							

Bit	Name	Access	Description
7:0 (byte 1)	MSB_VPWR	R	Eight most significant bits of the VPWR value
7:0 (byte 2)	LSB_VPWR	R	Eight least significant bits of the VPWR value

Note: V_{PWR} (mV) = (256*V_{PWRMSB} + V_{PWRLSB}) * 148.2 + 11830

The VPWR command typically takes 15ms to complete, including time for the Si34071 to receive the command (one byte of data), process the command, and complete sending the two byte response.

Table 2.8. MPS_ON Command

Command	Bit Position
0x04	N/A
Access	W
	MPS_ON

Bit	Name	Access	Description
N/A	MPS_ON	W	Writing the command 0x04 to the Si34071 enables MPS pulse generation. The Si34071 automatically selects short or long pulses based on what the PSE supports. While MPS pules are being generated UART data sent by the Si34071 is invalid, as the UART TX pin is used to generate the MPS pulses. The Si34071 does not send a response after receiving the MPS_ON command.

Note: The MPS_ON command typically takes 3ms to complete, including time for the Si34071 to receive the command (one byte of data) and begin MPS pulse generation.

Table 2.9. MPS_OFF Command

Command	Bit Position
0x05	N/A
Access	W
	MPS_OFF

Bit	Name	Access	Description
N/A	MPS_OFF	W	Writing the command 0x05 to the Si34071 disables MPS pulse generation and causes the Si34071 to resume standard UART operation. The Si34071 does not send a response after receiving the MPS_OFF command.

Note: The MPS_OFF command typically takes 3ms to complete, including time for the Si34071 to receive the command (one byte of data) and disable MPS pulse generation.

3. Application Examples

The following diagram demonstrates the ease of use and straightforward BOM of the Si34071 Powered Device IC. Detailed reference designs are available in Evaluation KIT User Guides. Also, refer to AN1179.

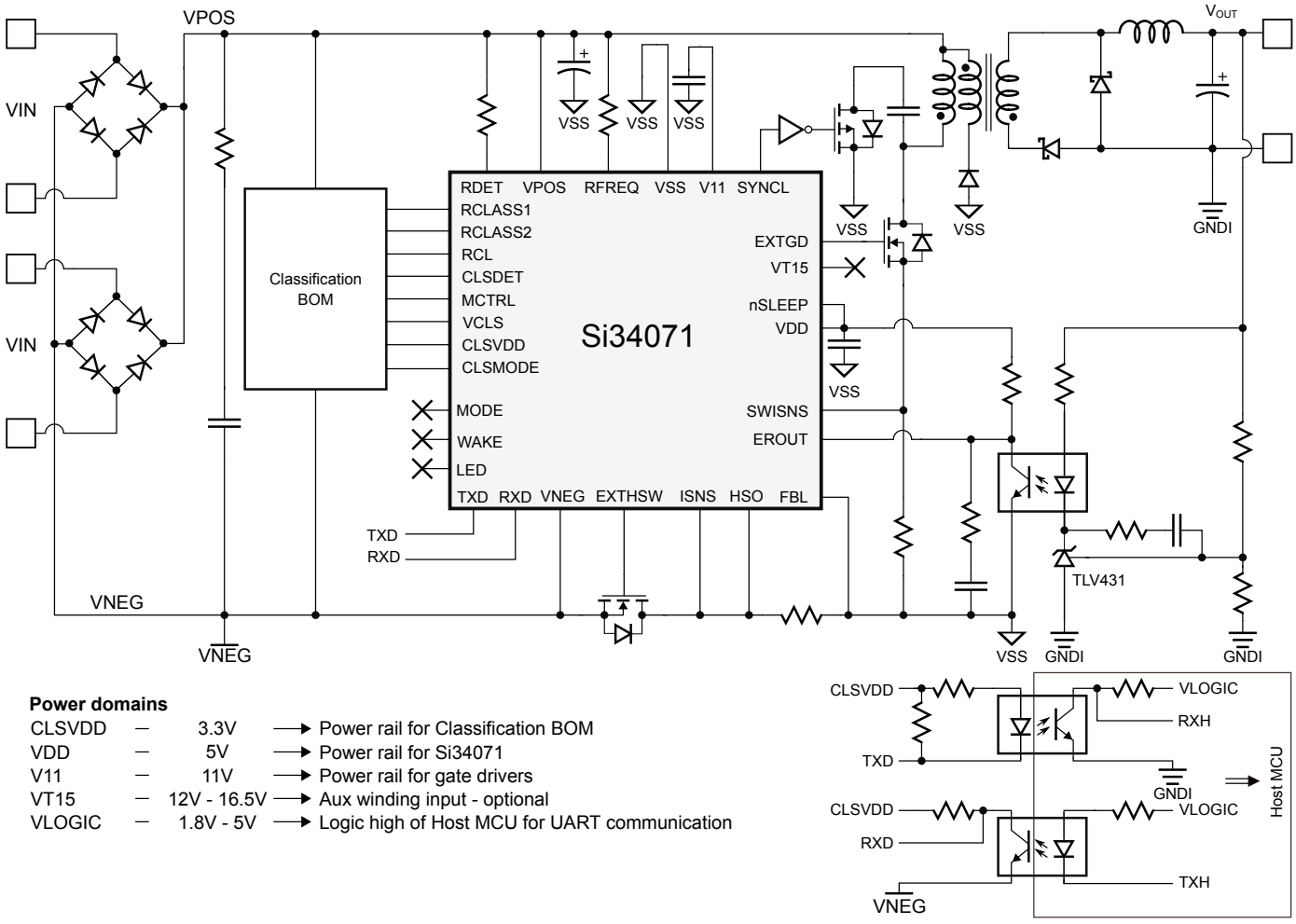


Figure 3.1. Si34071 Simplified Isolated Forward Application Diagram

4. Electrical Specifications

Table 4.1. Absolute Maximum Ratings

Type	Description	Min	Max	Units
Voltage	VSS-VNEG, VPOS-VNEG, HSO[2], RDET[3]	–0.7	100	V
	ISNS, SWISNS	–1	1	V
	EROUT, nSLEEP, RCL[2], RFREQ[3] MODE, LED	–0.7	6	V
	SYNCL,VT15, EXTGD, EXTHSW[2]	–0.7	18	V
	V11	–0.7	12	V
	CLSVDD[2]	-0.3	4.2	V
	RX[2], TX[2], VCLS[2], CLSMODE[2], R_{CLASS1}[2], R_{CLASS2}[2], MCTRL[2], CLSDET[2]	-0.3	5.8	V
Peak Current	VPOS[4]	–5	5	A
Temperature	Storage Temperature	–65	150	°C
	Ambient Operating Temperature	–40	85	
	Junction Temperature	—	125	

Note:

1. Unless otherwise noted, all voltages referenced to VSS. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. Voltage referenced to VNEG.
3. Voltage referenced to VPOS.
4. The Si34071 provides internal protection from certain transient surge voltages on this pin.

Table 4.2. Recommended Operating Conditions

Parameter (Condition)	Symbol	Min	Typ	Max	Unit
VPOS – VNEG	V_{PORT}	1.6	—	57	V
VNEG – VSS, VNEG – HSO, VPOS – VSS		1.6	—	57	V
VPOS referred low voltage pins: RFREQ, RDET		–5.5	—	0	V
VSS referred low voltage pins: VDD, EROUT, nSLEEP, LED, MODE		0	—	5.5	V
VNEG referred low voltage pin: RCL		0	—	5.5	V
VSS referred current sensing pins: ISNS, SWISNS		–0.5	—	0.5	V
VSS referred medium voltage pins: SYNCL, EXTGD		0	—	13	V
VNEG referred medium voltage pin: EXTHSW		0	—	13	V
VSS referred medium voltage pin: VT15[1]	V_{VT15}	12	14.5	16.5	V
Allowable continuous current on VSS and VNEG when internal HSSW is used[2]	I_{AVG}	—	—	600	mA
Maximum current on VNEG, VPOS Max 75 ms 5% Duty Cycle when internal HSSW is used[2]	I_{MAX}	—	—	683	mA

Note:

1. V_{VT15} is relevant for Si34071 only when an external auxiliary winding from the primary side of the transformer is being used to improve power conversion efficiency. This can be left undriven, in which case an internal regulator will be used.
2. The Si34071 requires an externally connected HSSW FET and automatically manages the use of either the internal HSSW or the external HSSW FET. See 2.4 Hotswap Switch for more details on the HSSW.

Table 4.3. Electrical Characteristics

Excluding detection and classification and unless otherwise noted, 37 V < VPOS – VNEG ≤ 57 V; junction temperature = –40 to +125 °C; typical specs are measured at 25 °C. All voltages are with respect to VSS unless otherwise noted.

Parameter (Condition)	Symbol	Min	Typ	Max	Unit
PoE PROTOCOL					
Detection					
Signature Range (at V_{PORT})	V_{DET}[1, 2]	2.7	—	10.1	V
Signature Resistance (at V_{PORT})		23.75	—	26.25	kΩ
Classification					
Classification Reset (at V_{PORT})	V_{RESET}[1]	0	—	2.81	V
Classification ON threshold (at V_{PORT})	V_{CLASS}[1]	—	—	14.5	V
Classification OFF threshold (at V_{PORT})		20.5	—	—	V
0	Class signature[3]	1		4	mA
1		9		12	mA
2		17		20	mA
3		26		30	mA
4		36		44	mA
Type 2 Classification					
Mark event voltage (at V_{PORT})	V_{MARK}[1]	6.9	—	10.1	V
Mark event current	I_{MARK}	0.25	—	4	mA
Power On and UVLO					
Hotswap closed and converter on	V_{UVLO_R}[1]	34	37	40	V
Hotswap open and converter off	V_{UVLO_F}[1]	30	32	34	V
	V_{UVLO_HYST}[1]	3.5	4.5	6	V
Thermal Characteristics					
Thermal shutdown	T_{SHD}	—	160	—	°C
Thermal shutdown hysteresis	T_{HYST}	—	20	—	°C
On-Chip Transient Voltage Suppression/Protection					
TVS protection activation voltage (VPOS-VNEG)	V_{PROT}	100	—	—	V
Hotswap Switch					
Switch ON voltage	V_{HSSW_ON}	—	380	—	mV
Switch OFF voltage, HSSW goes to overload cycle	V_{HSSW_OFF}	—	3.5	—	V
Switch current limit in OVERLOAD State	I_{OVL}	—	10.5	—	mA
External hotswap driver peak current on EXTHSW pin	I_{EXT_DRV}	—	—	10	mA

Parameter (Condition)	Symbol	Min	Typ	Max	Unit
External hotswap driver voltage on EXTHSW pin	V_{EXT_DRV}[1]	9	11	13	V
Wait time in OVERLOAD and type 2, 3, and 4 inrush	$T_{WAITHSSW}$	80	96	116	ms
DC-DC					
External FET driver voltage (EXTGD pin)	V_{EXTGD}	9	11	13	V
External FET driver peak current (EXTGD pin)	I_{EXTGD}	—	—	500	mA
Using internal Oscillator	F_{OSCINT}	215	250	290	kHz
Using external Oscillator, RFREQ = 215 kΩ	F_{OSCEXT}	75	95	115	kHz
Using external Oscillator, RFREQ = 39 kΩ		420	470	520	kHz
Output duty cycle of PWM	DUC	—	—	75	%
Operating voltage range of error input	V_{EROUT}	1	—	4	V
Output short protection if EROUT is max	T_{HICCUP}	—	1	—	ms
Overcurrent limit voltage on ISNS (ref. to VSS)	V_{ISNS_OVC}	–305	–270	–255	mV
Low current limit voltage on ISNS (ref. to VSS)	V_{ISNS_LC}	–45	–30	–15	mV
External FET peak current sense	$V_{SWISNSMAX}$	—	240	—	mV
Startup time[4]	$T_{SOFTSTART}$	—	15	—	ms
Regulators					
Override internal regulator with transformer winding	VT15	12.5	—	16.5	V
5 V regulated output	VDD	4.9	5.2	5.5	V
DC current limit of VDD	VDD_{ILIM}	9.7	11.2	—	mA
Filter capacitor on VDD and V11	C_{REG}	82	100	220	nF
LED pin max current, reduces VDD_{ILIM}	I_{MAXLED}	—	5	—	mA
Digital output max current, reduces VDD_{ILIM}	I_{MAXDO}	2	2.5	—	mA
Power Dissipation[5]					
Total chip power	P_{MAX}	—	500	—	mW
Operating current (V_{PORT} 57 V; 250 kHz)	I_{PortOP}	—	4.5	6.5	mA
Package Thermal Characteristics[5]					
QFN32	θ_{JA}	—	34	—	°C/W

Parameter (Condition)	Symbol	Min	Typ	Max	Unit

Note:

1. Referenced to VNEG.
2. Minimum VDET valid assuming a maximum bridge loss of 1.12 V. If a FET bridge is used, Schottky diodes must be placed in parallel to ensure the bridge loss is < 1.12 V for ambient temperatures below 0 °C.
3. For a long first classification pulse of the class, signature will change from Class 4 to Class 0 at between 75 and 88 ms if Auto-class operation is enabled by the setting of the classification mode pin. Classification pulse 2 will always give the classification Signature 4. The classification mode pin voltage also sets the class signature for subsequent classification pulses (requested Class 5 gives Class Signature 0 up to requested Class 8 giving Class Signature 3). The actual classification current is determined by the resistors R_{CLASS1} and R_{CLASS2} in the classification BOM. The recommended value of these resistors depends on the setting of the classification mode.
4. Depends on output load, automatically adjusted.
5. Assumes 4-Layer PCB with adequate layout.

5. Pin Descriptions

Si34071 Pinout
(Top View)

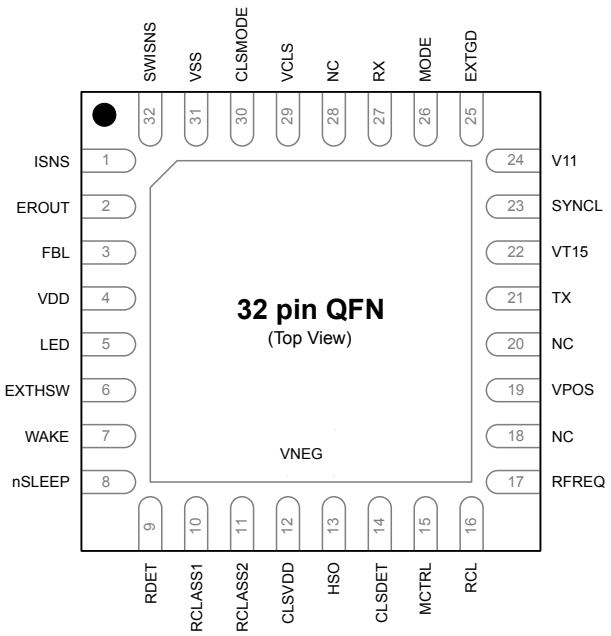


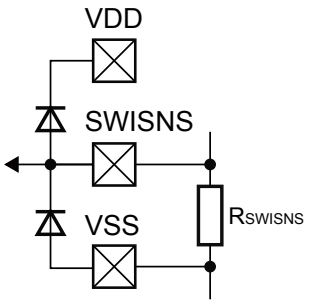
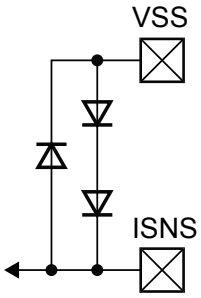
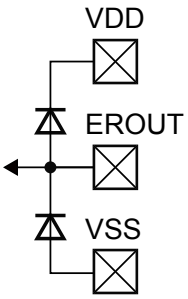
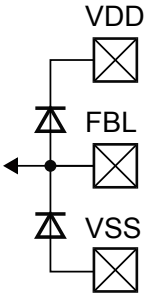
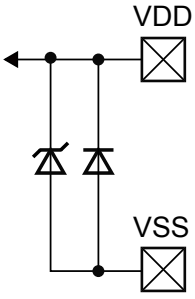
Table 5.1. Pin Descriptions

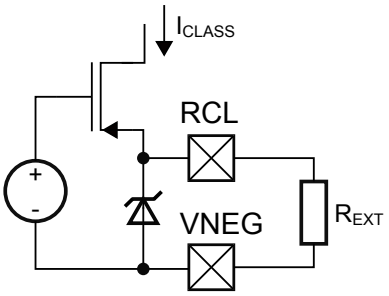
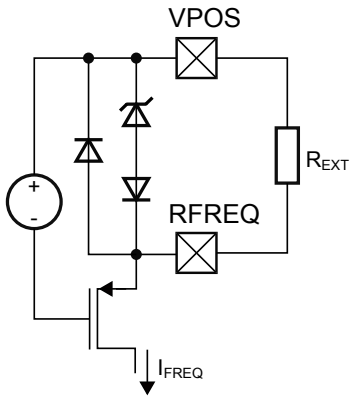
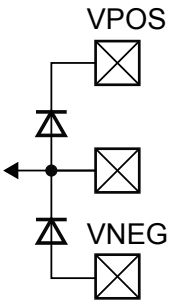
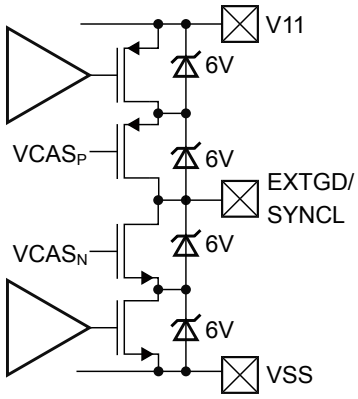
Pin Descriptions	Name	Ref.	Dir.	Description
1	ISNS	VSS	I	Chip average current sense resistor input.
2	EROUT	VSS	IO	Compensation impedance input.
3	FBL	VSS	I	Low-side (VSS referenced) dc-dc feedback (flyback converter).
4	VDD	VSS	O	5 V regulator output.
5	LED	VSS	O	Leave floating.
6	EXTHSW	VNEG	O	External hotswap switch drive.
7	WAKE	VSS	I	Leave floating.
8	nSLEEP	VSS	I	Tie to VDD.
9	RDET	VPOS	IO	Detection resistor.
10	R_{CLASS1}	CLSVDD	IO	Connect to one of two resistors that sets the current in classification.
11	R_{CLASS2}	CLSVDD	IO	Connect to one of two resistors that sets the current in classification.
12	CLSVDD	VNEG	IO	V_{DD} of the classification circuit.
13	HSO	VNEG	IO	Hotswap switch output.
14	CLSDET	VNEG	I	The voltage on this pin will go low when the input voltage is in the classification range.
15	MCTRL	VNEG	I	Controls power in mark state.

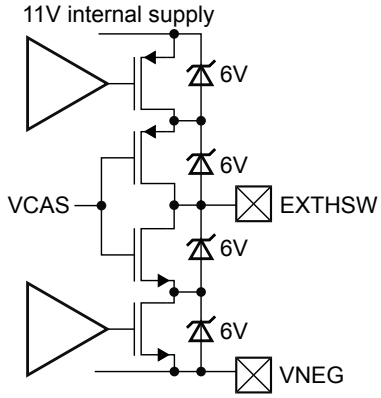
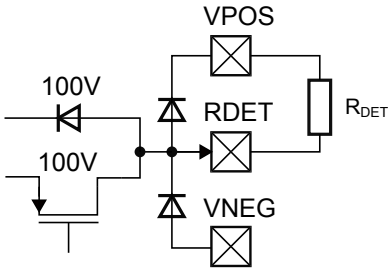
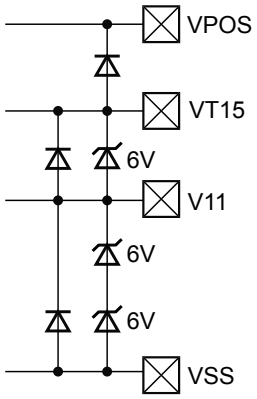
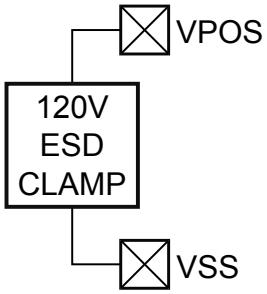
Pin Descriptions	Name	Ref.	Dir.	Description
16	RCL	VNEG	IO	This pin will go to approximately 1.2 V when the input is in the classification range.
17	RFREQ	VPOS	IO	Oscillator frequency tuning resistor, tie to VPOS to select default frequency.
18	NC			No connect, can be left floating or tied to VNEG.
19	VPOS	—	IO	Rectified high-voltage supply positive rail.
20	NC			No connect, can be left floating or tied to VNEG.
21	TX	VNEG	O	UART interface TX, also used to generate MPS pulses when MPS mode is enabled.
22	VT15	VSS	I	DC-DC transformer bias winding input.
23	SYNCL	VSS	O	Gate driver for rectification FET.
24	V11	VSS	IO	11 V regulator output for filter cap.
25	EXTGD	VSS	O	External FET gate drive.
26	MODE	VSS	I	Leave floating.
27	RX	VNEG	I	UART interface RX.
28	NC			No connect, leave floating.
29	VCLS	VNEG	I	This node is used for sensing when the input voltage is out of the classification range.
30	CLSMODE	VNEG	I	A resistor divider connected to this node sets the PD classification signature and autoclass flag.
31	VSS	—	IO	DC-DC converter primary ground.
32	SWISNS	VSS	I	External FET peak current sense resistor voltage input.
ePad	VNEG	—	IO	Negative output of the diode bridge.

5.1 Detailed Pin Descriptions

Table 5.2. Circuit Equivalent and Description of Select Die Pads

Pin Name	Detailed Description	Circuit Detail
SWISNS	External dc-dc switching FET peak current sense resistor input. The maximum current of the switching FET should correspond to voltage $V_{SWISNSMAX}$.	
ISNS	Average current sense resistor input. The resistor value will set the maximum allowed average current for the application. The overcurrent threshold voltage V_{ISNS_OVC}. Note that this pin voltage goes below VSS.	
EROUT	dc-dc converter error output; voltage sense. Loop compensating impedance should be connected here.	
FBL	Low side dc-dc feedback input. Need to be tied to VSS when not used. See V_{FBREF}.	
VDD	Regulated 5 V relative to VSS. There is no foldback characteristic, reaching VDD_{ILIM} the output voltage decreases. The regulator needs C_{REG} external capacitance.	

Pin Name	Detailed Description	Circuit Detail
RCL	Classification resistor input. Pin is active only during classification.	
RFREQ	Used for adjusting the oscillator frequency. The frequency is inversely proportional to the value of the connected resistor. See 2.7 Tunable Oscillator.	
VPOS, VNEG	VPOS: Positive power rail derived from the rectified PoE source VNEG: Negative power rail derived from the rectified PoE source. Note that VNEG (the ePad on the bottom of the chip) also provides thermal relief.	
EXTGD, SYNCL	EXTGD: External switch driver of the dc-dc converter. SYNCL: Optional synchronous rectifier switch driver of the flyback dc-dc converter or active clamp driver in forward. When not used the pin must be left floating.	

Pin Name	Detailed Description	Circuit Detail
EXTHSW	External hotswap switch driver output. This driver controls the external switch with 10 V logic level, relative to VNEG.	
RDET	The user has to tie the RDET resistor between this pin and VPOS. During detection, a high voltage switch pulls down RDET to VNEG. After detection, the reference block uses RDET as absolute chip current reference, forcing –750 mV relative to VPOS, creating 30 µA for the internal blocks.	
VT15, V11	VT15 is input for an optional 15 V supply generated by an auxiliary transformer bias winding. If the bias winding voltage is lower than VT15_MIN, the internal 15 V coarse regulator will provide the current for the 11 V regulator. The V11 pin is for filtering capacitor for the 11 V regulator. A capacitor of value C_{REG} is required referenced to V_{SS}.	
VSS	dc-dc converter ground.	

6. Packaging

6.1 Package Outline: Si34071

The figure below illustrates the package details for the Si34071. The table lists the values for the dimensions shown in the illustration.

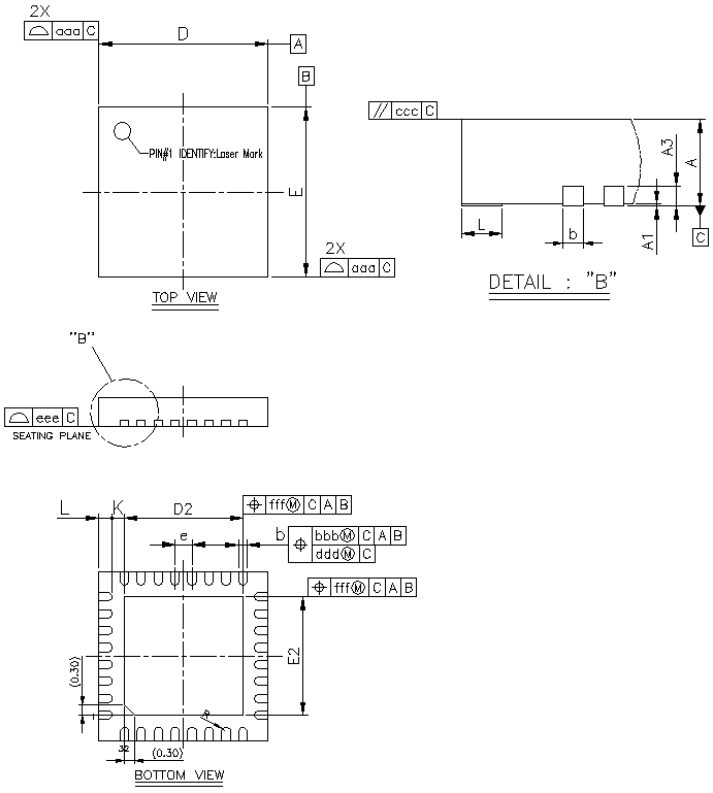


Figure 6.1. 32-Pin, QFN Package

Table 6.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	

Dimension	Min	Nom	Max
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHHD.

6.2 Land Pattern: Si34071

The figure below illustrates the land pattern details for the Si34071. The table lists the values for the dimensions shown in the illustration.

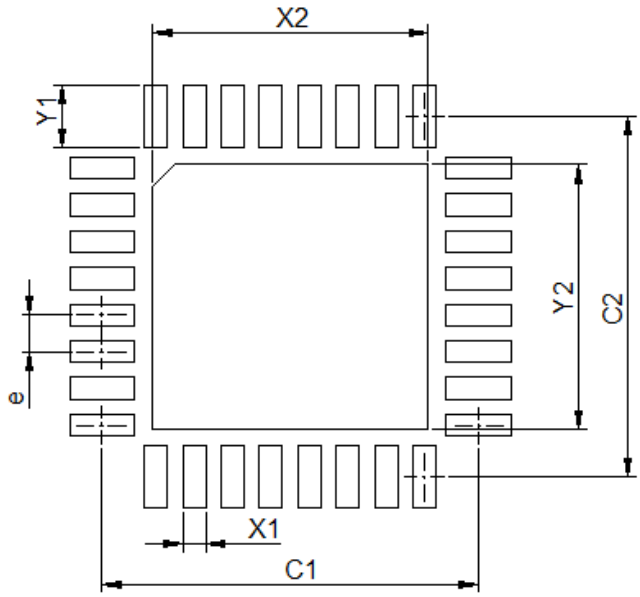


Figure 6.2. 32-Pin, QFN Land Pattern

Table 6.2. Land Pattern Dimensions

Dimension	Max
C1	4.90
C2	4.90
e	0.50
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	Max

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3x3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Markings

7.1 Si34071 Top Marking

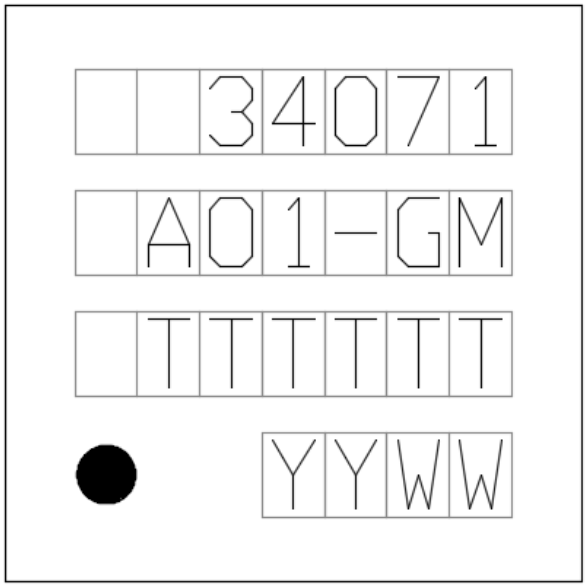


Figure 7.1. Si34071 Top Marking

Table 7.1. Si34071 Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Circle = 0.50 mm Diameter (Lower-Left Corner)	
Font Size:	2.0 Point (28 mils)	
Line 1 Mark Format:	Device Part Number	Si34071
Line 2 Mark Format:	Device Type	A = Device Revision A 01 = Firmware revision G = Temperature range M = QFN package
Line 3 Mark Format:	TTTTTT	Manufacturing Trace Code (assigned at assembly)
Line 4 Mark Format:	YY = Year WW = Work Week	Assembly Year Assembly Week

8. Revision History

Revision 1.0

April, 2021

- Updated Figure 2.4 Hotswap Switch 4-State Machine on page 9.
- Updated 2.10 UART Interface.
  - Improved formatting of tables.
- Updated 4. Electrical Specifications.
  - Updated Table 4.2 Recommended Operating Conditions on page 19.
  - Updated cold temperature operation specs in Table 4.3 Electrical Characteristics on page 20.

Revision 0.5

March, 2020

- Initial release.

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