Si50122-A3/A4

CRYSTAL-LESS PCI-EXPRESS GEN 1 & GEN 2 DUAL OUTPUT CLOCK GENERATOR

Features

- Crystal-less clock generator with integrated CMEMS
- PCI-Express Gen 1/2 compliant
- Two PCIe 100 MHz differential HCSL outputs
- One 25 MHz single-ended LVCMOS output
- Supports Serial (ATA) at 100 MHz
- Low power differential output buffers
- No termination resistors required for differential output clocks
- Triangular spread spectrum profile for maximum EMI reduction (Si50122-A4)
- Industrial Temperature –40 to 85 °C
- 2.5 V, 3.3 V Power supply
- Small package 10-pin TDFN (2.0x2.5 mm)
- Si50122-A3 does not support spread spectrum outputs
- Si50122-A4 supports 0.5% down spread outputs

Ordering Information:
See page 10

Applications

- Digital TV
- Set top box
- Solid State Drives (SSD)
- Wireless Access Point
- Home Gateway
- Network Attached Storage
- Multi-function Printer
- Wireless Access Point
- Digital Video Cameras

Pin Assignments

|		
VSS	1	10 VDD
REFOUT	2	9 VDD
NC	3	8 $\overline{DIFF2}$
DIFF1	4	7 DIFF2
$\overline{DIFF1}$	5	6 VSS

Patents pending

Description

Si50122-A3/A4 is a high performance, crystal-less PCIe clock generator that can generate two 100 MHz PCIe clock and one 25 MHz LVCMOS clock outputs. The differential clock outputs are compliant to PCIe Gen1 and Gen 2 specifications. The ultra-small footprint (2.0x2.5 mm) and industry leading low power consumption make Si50122-A3/A4 the ideal clock solution for consumer and embedded applications where board space is limited and low power is needed.

Functional Block Diagram
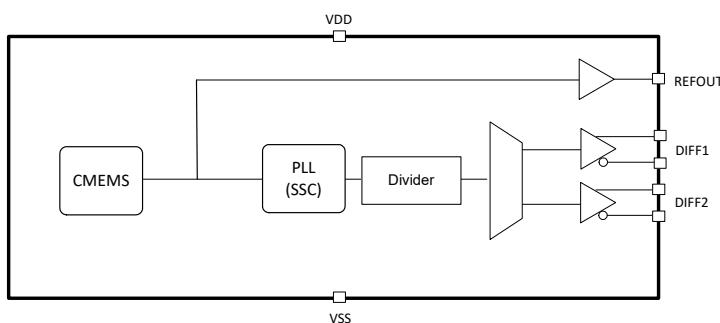
SILICON LABS

TABLE OF CONTENTS

SILICON LABS

Si50122-A3/A4

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (3.3 V Supply)	V_{DD}	3.3 V ± 10%	2.97	3.3	3.63	V
Supply Voltage (2.5 V Supply)	V_{DD}	2.5 V ± 10%	2.25	2.5	2.75	V

Table 2. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage$_{VDD=3.3\ V}$	V_{DD}	3.3 V ± 10%	2.97	3.30	3.63	V
Operating Voltage$_{VDD=2.5\ V}$	V_{DD}	2.5 V ± 10%	2.25	2.5	2.75	V
Operating Supply Current	I_{DD}	Full active; 3.3 V ± 10%	—	20	23	mA
		Full active; 2.5 V ± 10%	—	18	21	mA
Input Pin Capacitance	C_{IN}	Input Pin Capacitance	—	3	5	pF
Output Pin Capacitance	C_{OUT}	Output Pin Capacitance	—	—	5	pF

Rev 0.7

SILICON LABS

Table 3. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DIFF Clocks						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Skew	T_{SKEW}	Measured at 0 V differential	—	—	100	ps
Output Frequency	F_{OUT}	VDD = 3.3 V	—	100	—	MHz
Frequency Accuracy	F_{ACC}	All output clocks	—	—	100	ppm
Slew Rate	$t_{r/f2}$	Measured differentially from ±150 mV	0.6	—	5.0	V/ns
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		–0.3	—	—	V
Spread Range	S_{RNG}	Down Spread, –A4 only	—	—	–0.5	%
Modulation Frequency	F_{MOD}	–A4 only	30	31.5	33	kHz
DIFF Clocks Jitter Parameters, VDD = 3.3 V ± 10%						
PCIe Gen1 Pk-Pk	Pk-Pk$_{GEN1}$	PCIe Gen 1	—	20.7	35	ps
PCIe Gen2 Phase Jitter	RMS$_{GEN2}$	10 kHZ < F < 1.5 MHz	—	0.8	2.1	ps
		1.5 MHZ < F < Nyquist	—	1.4	2.2	ps
DIFF Clocks Jitter Parameters, VDD = 2.5V ± 10%						
PCIe Gen1 Pk-Pk	Pk-Pk$_{GEN1}$	PCIe Gen 1	—	25	40	ps
PCIe Gen2 Phase Jitter	RMS$_{GEN2}$	10 kHZ < F < 1.5 MHz	—	0.9	2.9	ps
		1.5 MHZ < F < Nyquist	—	1.7	3.0	ps
25 MHz at 3.3 V						
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	—	55	%
Output Rise Time	t_r	C_L = 10 pF, 20% to 80%		1.2	3.0	ns
Output Fall Time	t_f	C_L = 10 pF, 20% to 80%		1.2	3.0	ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	—	250	ps
Long Term Accuracy	L_{ACC}	Measured at 1.5 V	—	—	100	ppm
Powerup Time						
Clock Stabilization from Powerup	T_{STABLE}	First powerup to first output	—	—	10	ms
Note: Visit www.pcisig.com for complete PCIe specifications.						

Table 4. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature, Storage	T_S	Non-functional	–65		150	°C
Temperature, Operating Ambient	T_A	Functional	–40		85	°C
Temperature, Junction	T_J	Functional	—		150	°C
Dissipation, Junction to Case	$\varnothing_{JC}$	JEDEC (JESD 51)	—		38.3	°C/W
Dissipation, Junction to Ambient	$\varnothing_{JA}$	JEDEC (JESD 51)	—		90.4	°C/W

Table 5. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$		—		4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5		4.6	V_{DC}
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000		—	V
Flammability Rating	UL-94	UL (Class)		V–0		
Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is NOT required.						

SILICON LABS

2. Test and Measurement Setup

Figures 1–3 show the test load configuration for the differential clock signals.
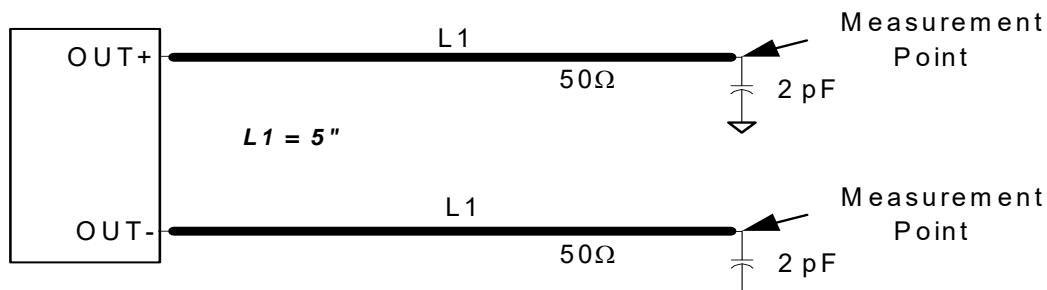
Figure 1. 0.7 V Differential Load Configuration
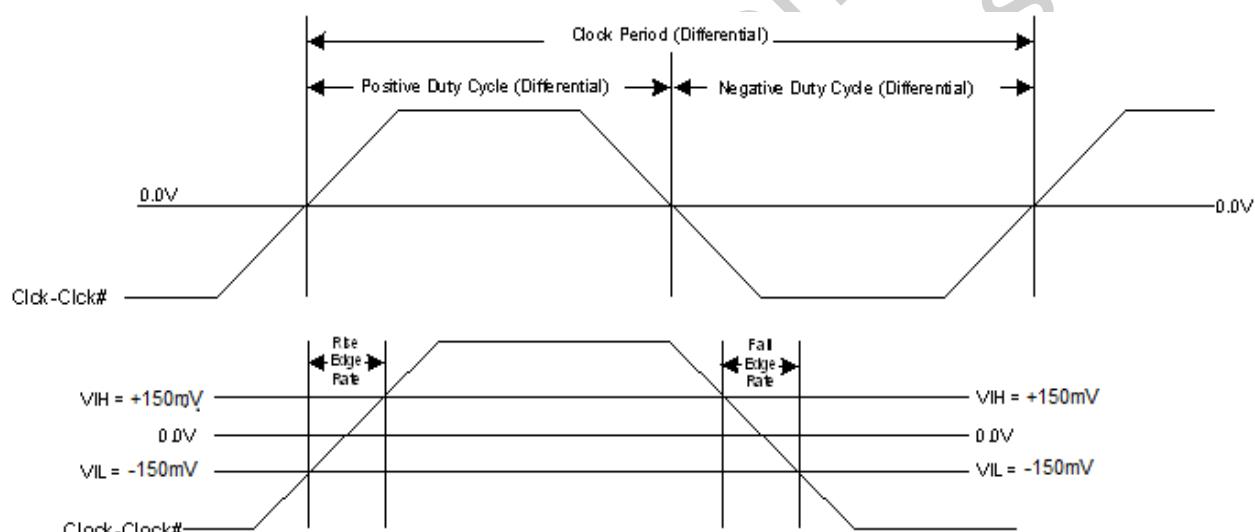
**Figure 2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)**
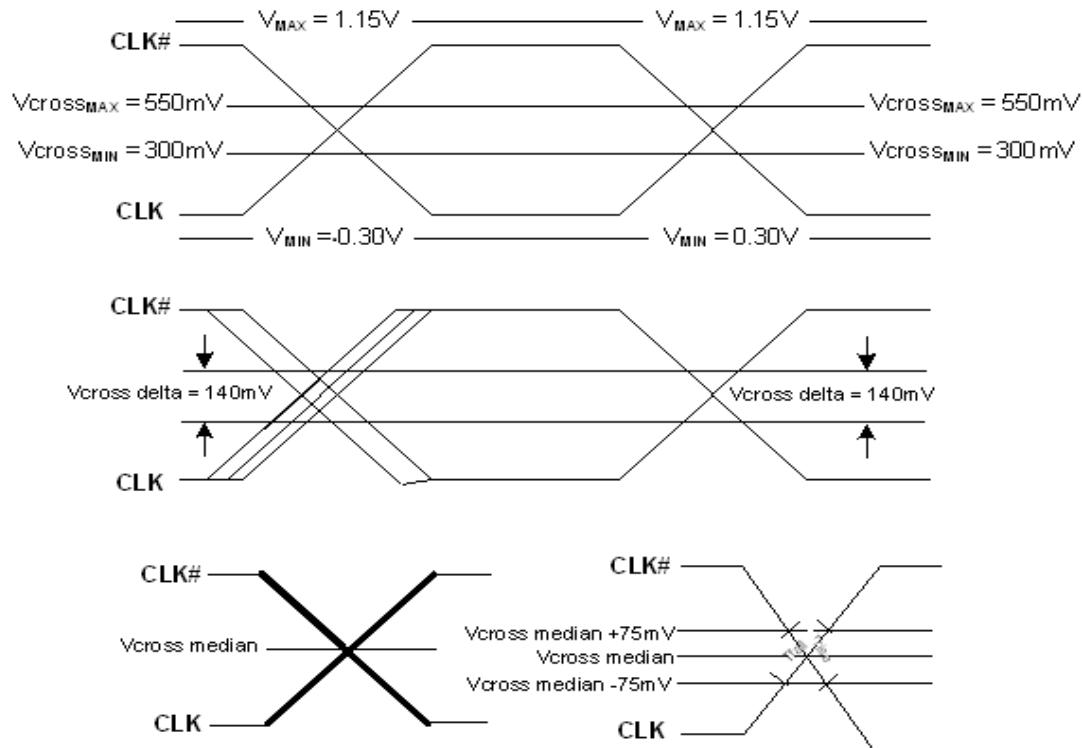
**Figure 3. Single-ended Measurement for Differential Output Signals
(for AC Parameters Measurement)**
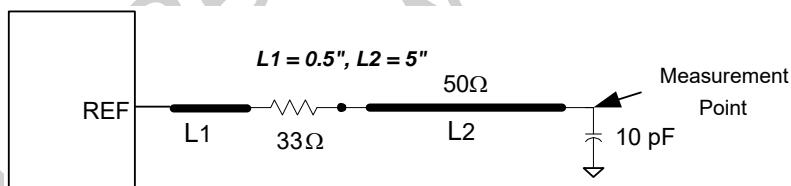

Figure 4. Single-ended Clocks with Single Load Configuration
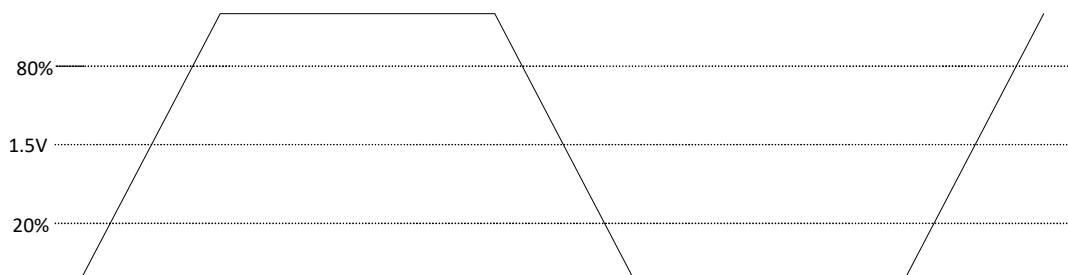
Figure 5. Single-ended Output Signal (for AC Parameter Measurement)

3. Pin Descriptions
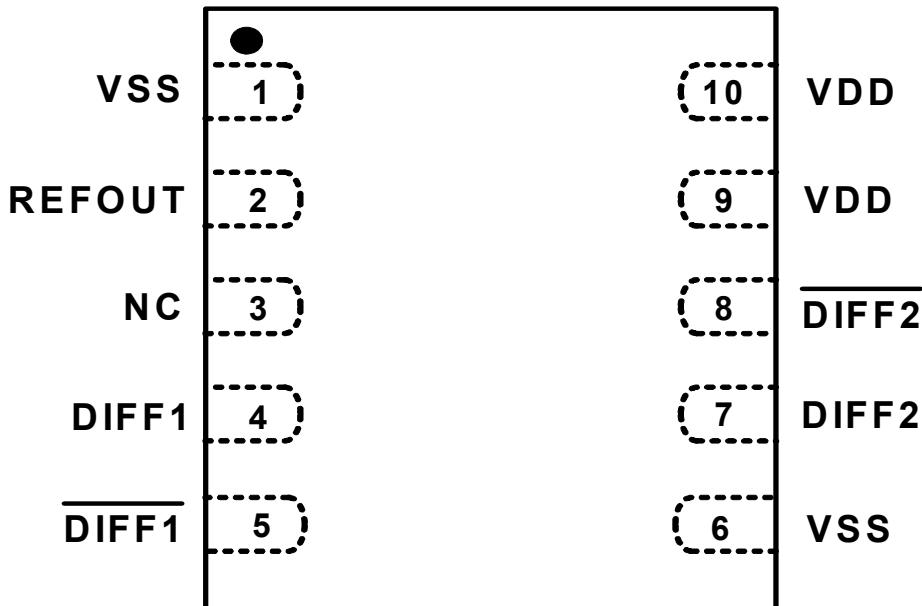
Figure 6. 10-Pin TDFN

Table 6. Si50122-Ax-GM 10-Pin TDFN Descriptions

Pin #	Name	Type	Description
1	VSS	GND	Connect to Ground
2	REFOUT	O, SE	25 MHz LVCMOS clock output
3	NC	NC	No Connect. Do not connect this pin to anything.
4	DIFF1	O, DIF	0.7 V, 100 MHz differential clock output
5	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock output
6	VSS	GND	Connect to Ground
7	DIFF2	O, DIF	0.7 V, 100 MHz differential clock output
8	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock output
9	VDD	PWR	Power supply
10	VDD	PWR	Power supply

4. Ordering Guide

| Part Number	Spread Option	Package Type	Temperature
Si50122-A3-GM	No Spread	10-pin TDFN	Industrial, –40 to 85 °C
Si50122-A3-GMR	No Spread	10-pin TDFN—Tape and Reel	Industrial, –40 to 85 °C
Si50122-A4-GM	–0.5% Spread	10-pin TDFN	Industrial, –40 to 85 °C
Si50122-A4-GMR	–0.5% Spread	10-pin TDFN—Tape and Reel	Industrial, –40 to 85 °C

```
┌──────────┐      ┌──────┐      ┌──────┐
│ Si50122  │──────│  Ax  │──────│ GMR  │
└──────────┘      └──────┘      └──────┘
     │               │             │
┌──────────────┐     │     ┌──────────────────────────────┐
│ Base part    │     │     │ Operating Temp Range:        │
│ number       │     │     │ G: -40 to +85 °C             │
└──────────────┘     │     │ M:10-TDFN Package, ROHS6, Pb-free │
                     │     │ R: Tape & Reel               │
         ┌───────────────────────┐ │ (blank) = Tubes     │
         │ A: Product Revision A  │ └──────────────────────────────┘
         │ x=3: non-spread outputs│
         │ x=4: -0.5% spread outputs│
         └───────────────────────┘
```
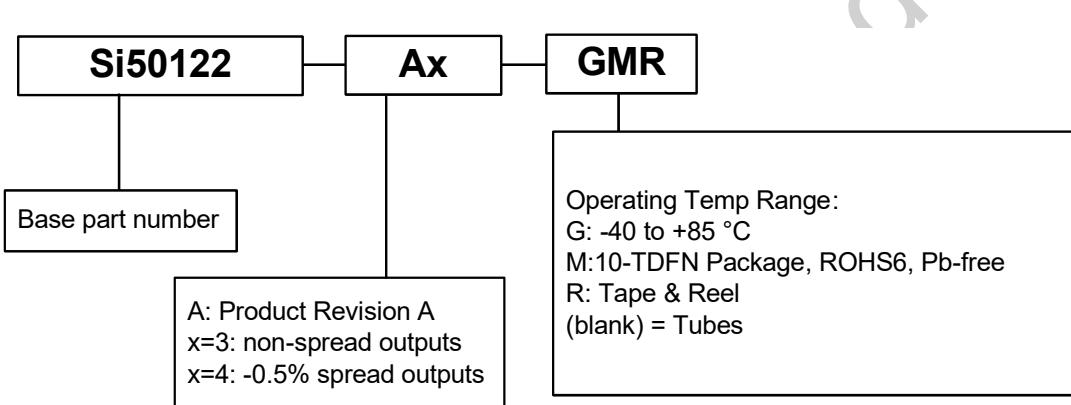
Figure 7. Ordering Information

SILICON LABS

5. Package Outlines
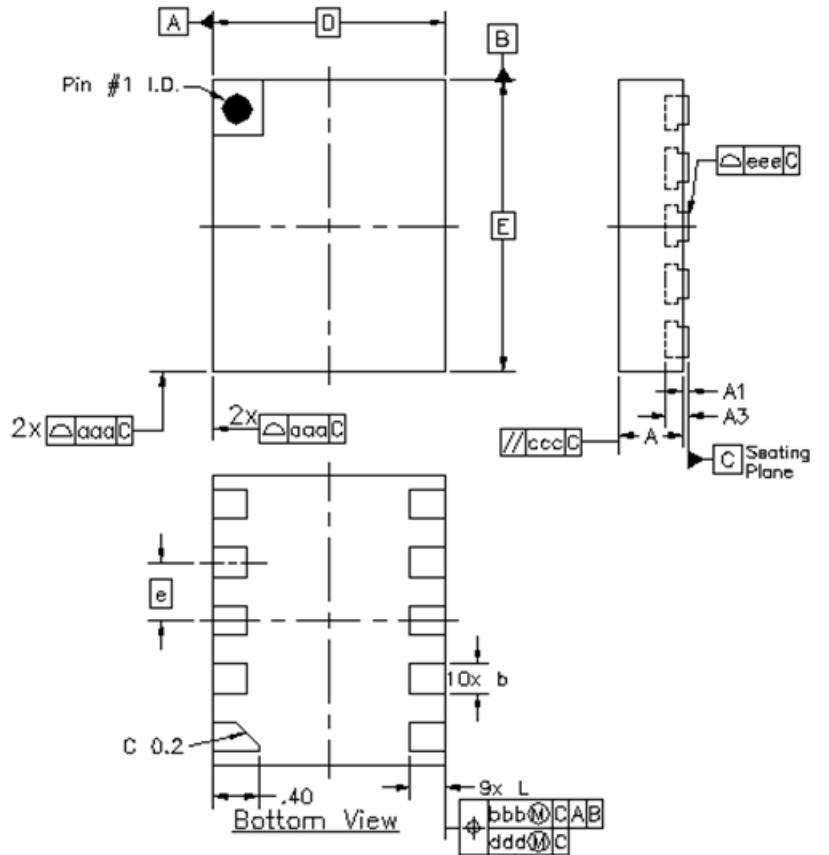
Figure 8. 10-Pin TDFN Package Drawing

Table 7. Package Diagram Dimensions

Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	2.00 BSC		
e	0.50 BSC		
E	2.50 BSC		
L	0.35	0.4	0.45
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

SILICON LABS

6. Recommended Design Guideline
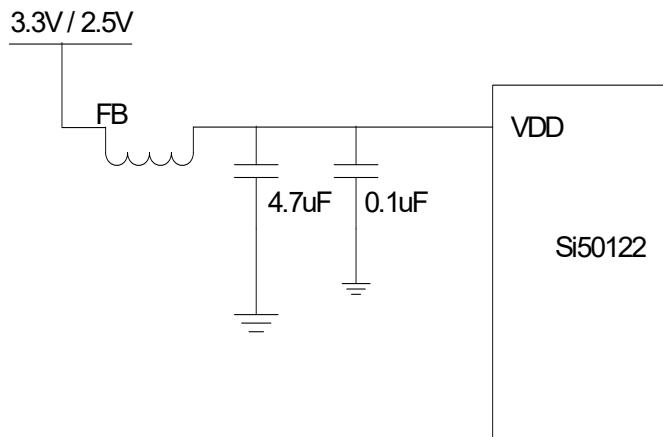
Note: FB Specifications:
DC resistance 0.1–0.3 Ω
Impedance at 100 MHz ≥ 1000 Ω

Figure 9. Recommended Application Schematic

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Clock Generators & Support Products *category:*

Click to view products by Silicon Labs *manufacturer:*

Other Similar products are found below :

5P49V5901A748NLGI 5P49V5901B680NLGI 5P49V5901B744NLGI 5P49V5929B502NLGI 5P49V5935B520LTGI 5V49EE903-116NLGI CV183-2TPAG 82P33814ANLG/W 8T49N004A-002NLGI 8T49N004A-039NLGI 9FGV0631CKLF 9FGV0641AKLFT 9LRS3197AKLF 9UMS9633BFILF 9VRS4450AKLF NB3N51132DTR2G 8N3Q001EG-0035CDI 932SQ426AKLF 950810CGLF 9DBV0531AKILF 9DBV0741AKILF 9FGV0641AKLF 9UMS9633BKLF 9VRS4420DKILF 9VRS4420DKLF 9VRS4420DKLFT CY25404ZXI226 CY25422SXI-004 5P49V5901B712NLGI NB3H5150-01MNTXG 6INT61041NDG PL602-20-K52TC PL613-51QC 8N3Q001FG-1114CDI 9FGV0641AKILF ZL30314GKG2 ZL30253LDG1 ZL30251LDG1 ZL30250LDG1 ZL30169LDG1 ZL30142GGG2 9UMS9633BKILFT 9FGV0631CKLFT 9FGV0631CKILF 5P49V5935B536LTGI PI6LC48P0101LIE DS1099U-ST+ MAX24305EXG+ PI6LC48H02-01LIE 82P33814ANLG