

# Si51211 Data Sheet

## Three Output Factory Programmable Clock Generator

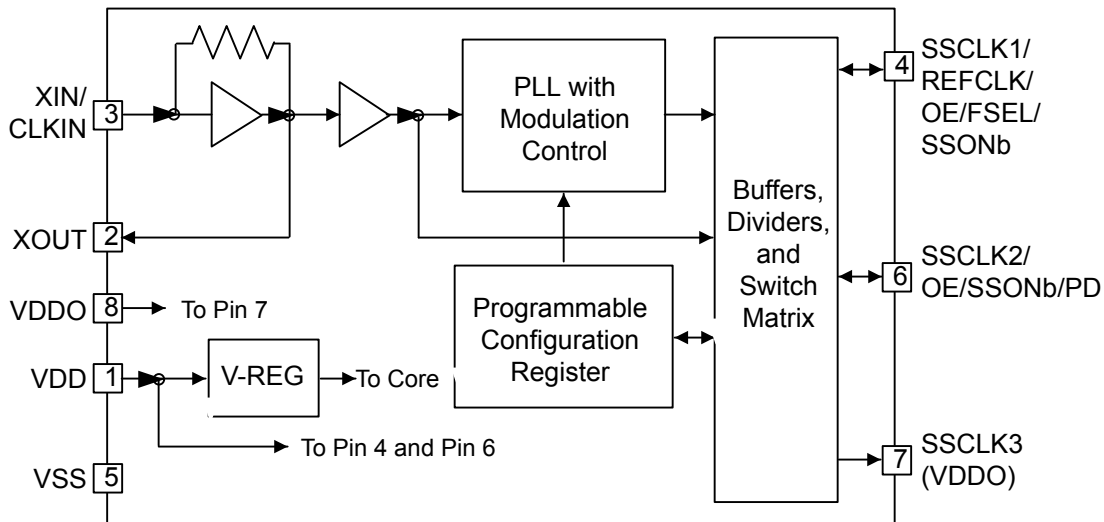
The factory programmable Si51211 is a low power, small footprint and frequency flexible programmable clock generator targeting low power, low cost and high volume consumer and embedded applications. The device operates from a single crystal or an external clock source and generates 1 to 3 outputs up to 170 MHz. The device is factory programmed to provide customized output frequencies and control input such as frequency select, spread spectrum on, power down and output enable. Center spread spectrum can also be programmed to reduce EMI to meet board level system requirements.

### Applications

- Crystal/XO replacement
- EMI reduction
- Portable devices
- Digital still camera
- IP phone
- Smart meter

### KEY FEATURES

- Generates up to 3 CMOS clock outputs from 3 to 170 MHz
- Accepts crystal or reference clock input
  - 3 to 165 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable FSEL, SSONb, PD, and OE input functions



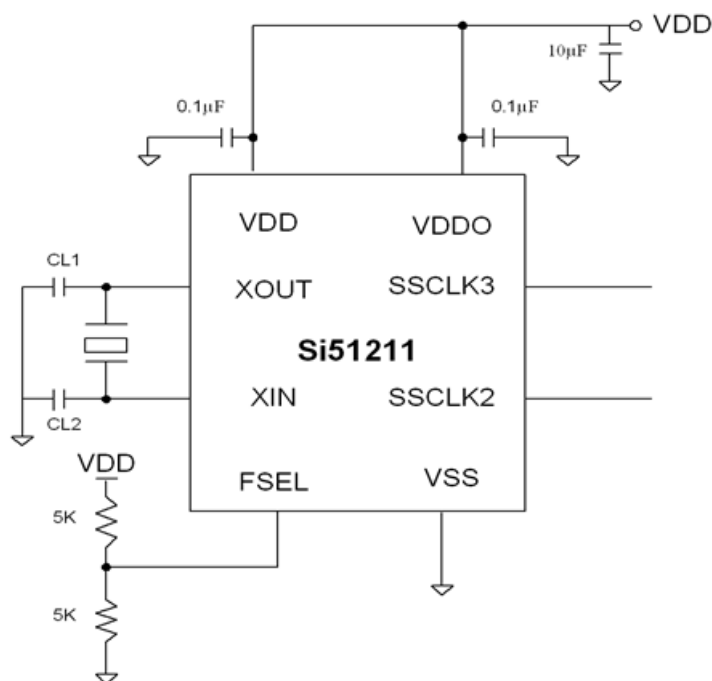
## 1. Feature List

The Si51211 highlighted features are listed below.

- Generates up to 3 CMOS clock outputs from 3 to 170 MHz
- Accepts crystal or reference clock input
  - 3 to 165 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable FSEL, SSONb, PD, and OE input functions
- Low power dissipation
- Separate voltage supply pins
  - $V_{DD} = 2.5$  to  $3.3$  V
  - $V_{DDO} = 1.8$  to  $3.3$  V ( $V_{DDO} \leq V_{DD}$ )
- $\pm 0.25\%$ ,  $\pm 0.5\%$  or  $\pm 1\%$  spread spectrum (center spread)
- Low cycle-cycle jitter
- Ultra small 8-pin TDFN package (1.4 mm x 1.6 mm)

## 2. Design Considerations

### 2.1 Typical Application Schematic



### 2.2 Comments and Recommendations

**Decoupling Capacitor:** A decoupling capacitor of 0.1 µF must be used between VDD and VSS on pins 1 and 8. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin. In addition, a 10 µF capacitor should be placed between VDD and VSS.

**Series Termination Resistor:** A series termination resistor is recommended if the distance between the outputs (SSCLK or REFCLK pins) and the load is over 1 ½ inches. The nominal impedance of the SSCLK output is about 30 Ω. Use a 20 Ω resistor in series with the output to terminate a 50 Ω trace impedance and place a 20 Ω resistor as close to the SSCLK output as possible.

**Crystal and Crystal Load:** Only use a parallel resonant fundamental AT cut crystal. Do not use higher overtone crystals. To meet the crystal initial accuracy specification (in ppm) make sure that the external crystal load capacitor is matched to the crystal load specification. To determine the value of CL1 and CL2, use the following formula:

$$CL1 = CL2 = 2CL - (C_{pin} + C_p);$$

where CL is the load capacitance stated by the crystal manufacturer,

C<sub>pin</sub> is the Si51211 pin capacitance (3 pF), and

C<sub>p</sub> is the parasitic capacitance of the PCB traces.

**Example:** If a crystal with CL = 12 pF specification is used and C<sub>p</sub> = 1 pF (parasitic PCB capacitance on PCB), 19 or 20 pF external capacitors from pins XIN (pin 2) and XOUT (Pin 3) to VSS are required. Users must verify C<sub>p</sub> value.

**Table 2.1. Crystal Specifications**

Equivalent Series Resistance (ESR)	Crystal Output Capacitance (CO)	Load Capacitance (CL)
≤ 50 Ω	≤ 3 pF	≤ 13 pF

### 3. Electrical Specifications

**Table 3.1. DC Electrical Specifications**
 $(V_{DD} = 2.5\text{ V} \pm 10\%, \text{ or } V_{DD} = 3.3\text{ V} \pm 10\%, V_{DDO} = V_{DD}, C_L = 10\text{ pF}, T_A = -40\text{ to } 85\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	$V_{DD} = 3.3\text{ V} \pm 10\%$	2.97	3.3	3.63	V
		$V_{DD} = 2.5\text{ V} \pm 10\%$	2.25	2.5	2.75	V
	$V_{DDO}$	$V_{DDO} \leq V_{DD}$	1.71	—	3.6	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4\text{ mA}$ , $V_{DDX} = V_{DD}$ or $V_{DDO}$	$V_{DDX} - 0.5$	—	—	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 4\text{ mA}$	—	—	0.3	V
Input High Voltage	$V_{IH}$	CMOS Level	$0.7 V_{DD}$	—	—	V
Input Low Voltage	$V_{IL}$	CMOS Level	0	—	$0.3 V_{DD}$	V
Operating Supply Current <sup>1</sup>	$I_{DD}$	$F_{IN} = 12\text{ MHz}$ , $SSCLK1 = 12\text{ MHz}$ , $SSCLK2 = 24\text{ MHz}$ , $C_L = 5\text{ pF}$ , $V_{DD}$ $= V_{DDO} = 3.3\text{ V}$	—	6.3	10	mA
Power Down Current		$I_{DDPD}$	—	0.5	0.65	mA
Nominal Output Impedance	$Z_O$		—	30	—	$\Omega$
Internal Pull-up/Pull-down Resistor	$R_{PUP}/R_{PD}$	Pin 6	—	150k	—	$\Omega$
Input Pin Capacitance	$C_{IN}$	Input pin capacitance	—	3	5	pF
Load Capacitance	$C_L$		—	—	10	pF

**Note:**

1.  $I_{DD}$  depends on input and output frequency configurations.

**Table 3.2. AC Electrical Specifications**
 $(V_{DD} = 2.5\text{ V} \pm 10\%, \text{ or } V_{DD} = 3.3\text{ V} \pm 10\%, V_{DDO} = V_{DD}, C_L = 10\text{ pF}, T_A = -40\text{ to } 85\text{ }^\circ\text{C})$ 

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	$F_{IN1}$	Crystal input	8	—	48	MHz
Input Frequency Range	$F_{IN2}$	Reference clock Input	3	—	165	MHz
Output Frequency Range	$F_{OUT}$	SSCLK1/2/3	3	—	170	MHz
Frequency Accuracy	$F_{ACC}$	Configuration dependent	—	0	—	ppm
Output Duty Cycle	$DC_{OUT}$	Measured at $V_{DDO}/2$ $F_{OUT} \leq 75\text{ MHz}$	45	50	55	%
		Measured at $V_{DDO}/2$ $F_{OUT} > 75\text{ MHz}$	40	50	60	%
Input Duty Cycle	$DC_{IN}$	CLKIN, CLKOUT through PLL	30	50	70	%

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Rise/Fall Time	$t_r/t_f$	$C_L = 10$ pF, 20 to 80%	—	1	2	ns
Period Jitter	PJ <sub>1</sub>	SSCLK1/2/3, at the same frequency	—	12	20	ps rms
	PJ <sub>2</sub>	SSCLK1/2/3, at different output frequencies <sup>1</sup>	—	30	95 <sup>2</sup>	ps rms
Cycle-to-Cycle Jitter	CCJ <sub>1</sub>	SSCLK1/2/3, at the same frequency	—	85	150	ps
	CCJ <sub>2</sub>	SSCLK1/2/3, at different output frequencies <sup>1</sup>	—	145	290 <sup>2</sup>	ps
Power-up Time	$t_{PU}$	Time from 0.9 $V_{DD}$ to valid frequencies at all clock outputs	—	1.2	5	ms
Output Enable Time	$t_{OE}$	Time from OE rising edge to active at outputs SSCLK1/2 (asynchronous), $F_{OUT} = 133$ MHz	—	15	—	ns
Output Disable Time	$t_{OD}$	Time from OE falling edge to active at outputs SSCLK1/2 (asynchronous), $F_{OUT} = 133$ MHz	—	15	—	ns
Spread Spectrum Modulation Rate <sup>3</sup>	SS <sub>DEV</sub>		—	37	—	kHz

**Note:**

1. Example frequency configurations:

- 8 MHz, 100 MHz, 75 MHz
- 48 MHz, 100 MHz, 66 2/3 MHz
- 96 MHz, 133 1/3 MHz, 133 1/3 MHz

2. Jitter performance depends on configuration and programming parameters.

3. The SS modulation rate is a fixed ratio of the reference frequency with values in the range of 30 kHz to 50 kHz based on the frequency plan.

**Table 3.3. Absolute Maximum Conditions**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD}$		-0.5	—	4.2	V
Input Voltage	$V_{IN}$	Relative to $V_{SS}$	-0.5	—	$V_{DD} + 0.5$	V
Temperature, Storage	$T_S$	Non-functional	-65	—	150	°C
Temperature, Operating Ambient	$T_A$	Functional, I-Grade	-40	—	85	°C
ESD Protection (Human Body Model)	ESD <sub>HBM</sub>	JEDEC (JESD 22-A114)	-4000	—	4000	V
ESD Protection (Charge Device Model)	ESD <sub>CDM</sub>	JEDEC (JESD 22-C101)	-1500	—	1500	V
ESD Protection (Machine Model)	ESD <sub>MM</sub>	JEDEC (JESD 22-A115)	-200	—	200	V

**Note:**

1. While using multiple power supplies, the Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

## 4. Functional Description

### 4.1 Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 3.0 to 165.0 MHz.

### 4.2 Output Frequency Range and Outputs

Up to three outputs can be programmed as SSCLK or REFCLK. SSCLK output can be synthesized to any value from 3 to 170 MHz with spread based on valid input frequency. The spread at the SSCLK pins can be enabled or disabled by the SSONb input control pin. If SSONb is used, when this pin is pulled high ( $V_{DD}$ ), the frequency at SSCLK pin is synthesized to the nominal value of the input frequency without spread. If low (GND), the frequency at SSCLK is synthesized to the nominal value of the input frequency with spread..

REFCLK is the buffered output of the oscillator and is the same frequency as the input frequency without spread. By using only low cost, fundamental mode crystals, the Si51211 can synthesize output frequency up to 170 MHz, eliminating the need for higher order crystals (Xtals) and crystal oscillators (XOs). This reduces the cost while improving the system clock accuracy, performance, and reliability.

### 4.3 Programmable Spread Percent (%)

The spread percent (%) value is programmable to  $\pm 0.25\%$ ,  $\pm 0.5\%$  or  $\pm 1\%$  (center spread) for all SSCLK frequencies.

### 4.4 SSONb or Frequency Select (FSEL)

The Si51211 pins 4 and 6 can be programmed as SSONb to enable or disable the programmed spread percent value. If SSONb is used, when this pin is pulled high ( $V_{DD}$ ), the frequency at SSCLK pin is synthesized to the nominal value of the input frequency without spread. If low (GND), the frequency at SSCLK is synthesized to the nominal value of the input frequency with spread. Pin 4 can also be programmed as frequency select (FSEL) function.

If FSEL function is used, the output pin can be programmed for different set of frequencies as selected by FSEL. SSCLK value can be any frequency from 3 to up to 170 MHz, but the spread % is the same percent value. REFCLK is the same frequency as the input reference clock. The set of frequencies in the table below are given as an example, using a 48 MHz crystal.

**Table 4.1. Example Frequencies**

FSEL Pin 4	SSCLK1 Pin 6
0	66 MHz, $\pm 1\%$
1	33 MHz, $\pm 1\%$

### 4.5 Power Down (PD) or Output Enable (OE)

The Si51211 pin 6 can be programmed as PD input. Pin 4 and pin 6 can be programmed as OE input. PD turns off both PLL and output buffers whereas OE only disables the output buffers to Hi-Z. The OE function is asynchronous. Any requirement for synchronous operations (like glitchless output clock switching) needs to be handled externally.

## 5. Pin Description

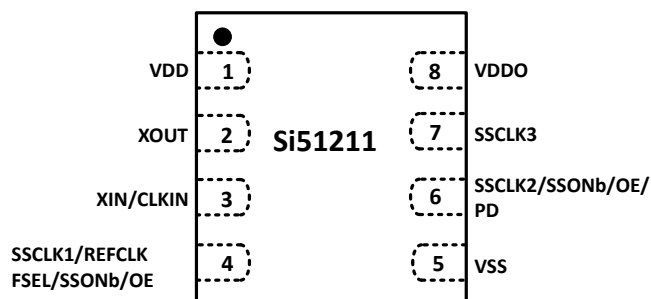


Figure 5.1. 8-Pin TDFN

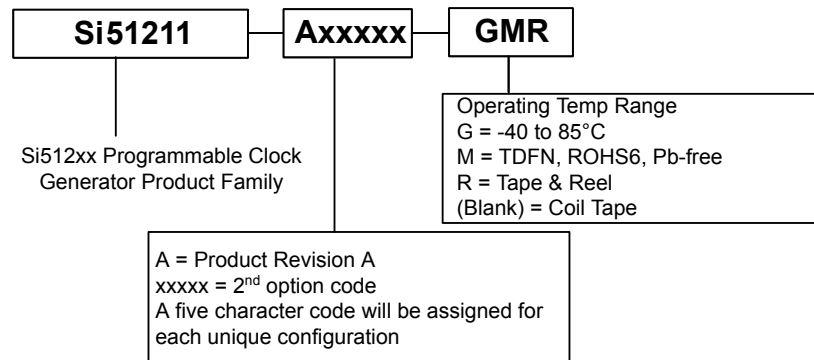
Table 5.1. Si51211 8-Pin Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	2.5 to 3.3 V power supply.
2	XOUT	O	Crystal output. Leave this pin unconnected (floating) if an external clock input is used.
3	XIN/CLKIN	I	External crystal and clock input.
4	SSCLK1/REFCLK/FSEL/SSONb/OE	I/O	Programmable SSCLK1 or REFCLK output or MultiFunction control input. The frequency at this pin is synthesized by the internal PLL if programmed as SSCLK1 with or without spread. If programmed as REFCLK, output clock is a buffered output of crystal or reference clock input. If programmed as a MultiFunction control input, it can be OE, FSEL, and SSONb.
5	VSS	GND	Ground.
6	SSCLK2/SSONb/PD/OE	I/O	Programmable SSCLK2 output or MultiFunction control input. The frequency at this pin is synthesized by the internal PLL if programmed as SSCLK2 with or without spread. SSCLK2 output can also be programmed as a buffered output of crystal or reference clock input divided by N, $2 \leq N \leq 8$ . If programmed as a MultiFunction control input, it can be OE, PD, and SSONb. This pin cannot be programmed as FSEL control input.
7	SSCLK3	O	Programmable SSCLK3 output. The frequency at this pin is synthesized by internal PLL with or without spread. It is powered by $V_{DDO}$ pin (pin 8).
8	VDDO	PWR	1.8 to 3.3 V output power supply to SSCLK3 (pin 7) $V_{DDO} \leq V_{DD}$ .

## 6. Ordering Guide

Table 6.1. Si51211 Ordering Guide

Part Number	Package Type	Temperature
Si51211-Axxxxx-GM	8-pin TDFN	Industrial, -40 to 85 °C
Si51211-Axxxxx-GMR	8-pin TDFN—Tape and Reel	Industrial, -40 to 85 °C





## 7. Package Outline

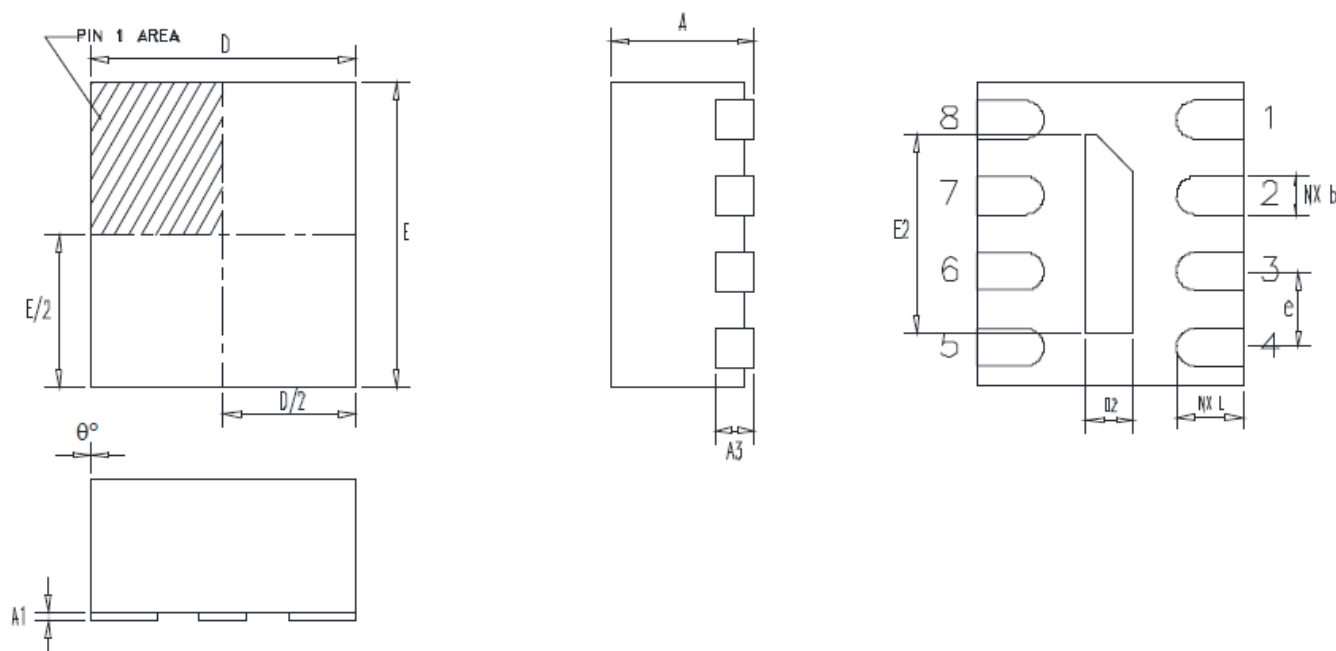


Figure 7.1. 8-pin TDFN

Table 7.1. Si51211 Package Dimensions

Dimension	mm		mils		
	Symbol	Min	Max	Min	Max
A		0.70	0.80	27.56	31.50
A1		0	0.05	0	1.97
A3		0.175	0.225	6.89	8.86
D		1.3	1.5	51.18	59.06
E		1.5	1.7	59.06	66.93
D2		0.20	0.30	7.87	11.81
E2		1.0	1.1	39.37	43.31
e		0.4 BSC		15.75 BSC	
NX b		0.15	0.25	5.91	9.84
NX L		0.25	0.45	9.84	17.72
$\theta^\circ$		$0^\circ$	$4^\circ$	$0^\circ$	$4^\circ$
ND		0			
NE		4			

Dimension	mm		mils	
Symbol	Min	Max	Min	Max
<b>Note:</b> <ol style="list-style-type: none"><li>1. Spade width, lead width and lead thickness exclusive of solder plate.</li><li>2. Package outline exclusive of mold flashes and burr dimensions.</li><li>3. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08 mm.</li><li>4. Warpage shall not exceed 0.10 mm.</li><li>5. The Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.</li><li>6. ND and NE refer to the number of terminals on each D and E side respectively.</li></ol>				

## 8. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the device. The table below lists the values for the dimensions shown in the illustration.

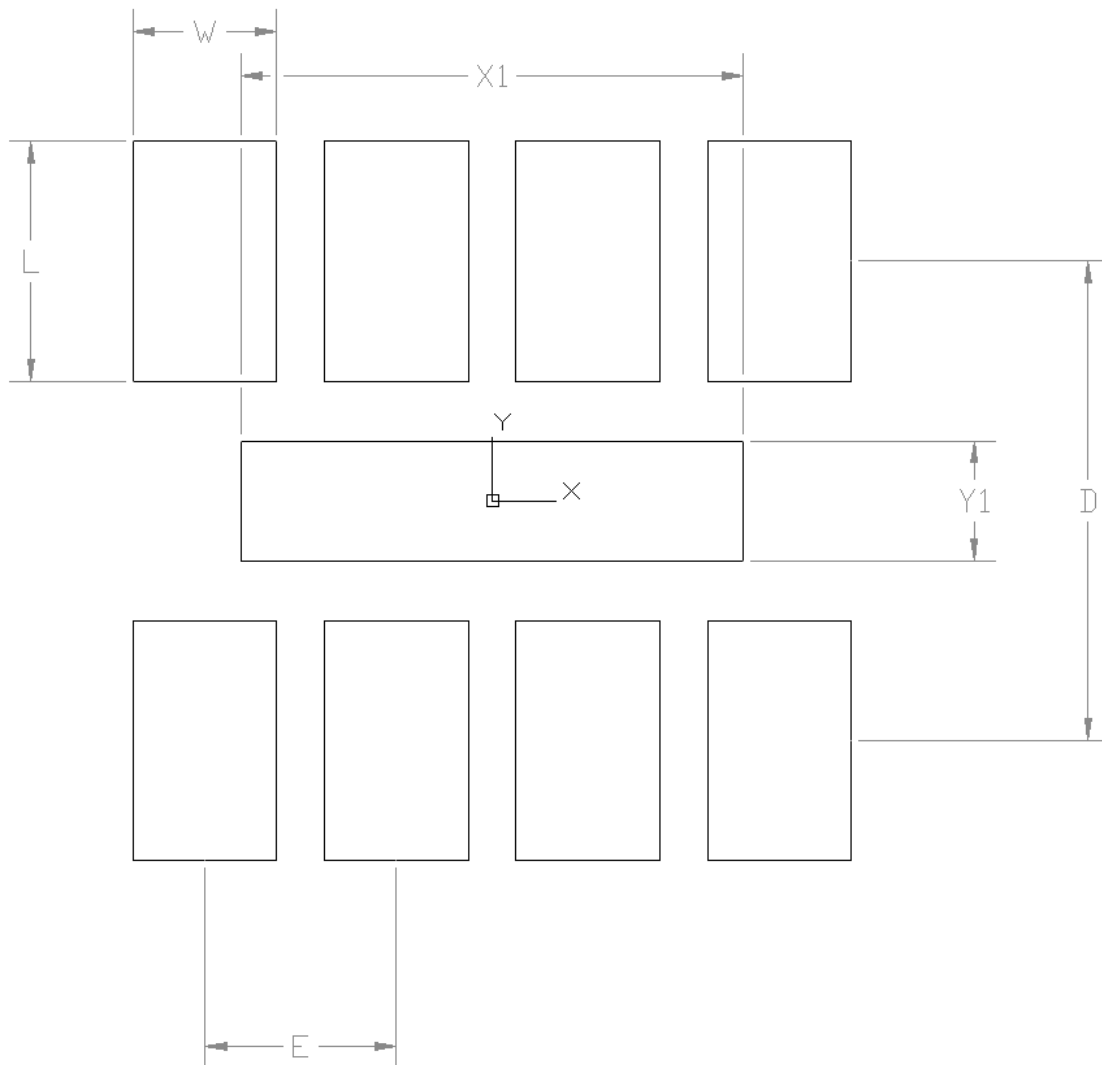


Figure 8.1. Si51211 8-pin TDFN PCB Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Dimension	mm
D	1.00
E	0.40
L	0.5
W	0.3
X1	1.05
Y1	0.25

Dimension	mm
<p><b>Note:</b></p> <p><b>General</b></p> <ol style="list-style-type: none"><li>1. All dimensions shown are in millimeters (mm).</li><li>2. This Land Pattern Design is based on the IPC-7351 guidelines.</li><li>3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication allowance of 0.05 mm.</li></ol> <p><b>Solder Mask Design</b></p> <ol style="list-style-type: none"><li>1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 <math>\mu\text{m}</math> minimum, all the way around the pad.</li></ol> <p><b>Stencil Design</b></p> <ol style="list-style-type: none"><li>1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li><li>2. The stencil thickness should be 0.125 mm (5 mils).</li><li>3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li><li>4. A 2x1 array of 0.55 mm square openings on 0.90 mm pitch should be used for the center ground pad.</li></ol> <p><b>Card Assembly</b></p> <ol style="list-style-type: none"><li>1. A No-Clean, Type-3 solder paste is recommended.</li><li>2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li></ol>	

## 9. Revision History

### 9.1 Revision 1.0

April 20, 2016

- Updated max output frequency to 170 MHz
- Updated max clock input frequency to 165 MHz
- Updated Operating Temperature to Industrial temperature,  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$
- Updated PD programmable active state
- Removed programmable output rise/fall time, SSEL.
- Updated [Table 3.1 DC Electrical Specifications on page 3](#)
- Updated [Table 3.2 AC Electrical Specifications on page 3](#)
- Updated pin descriptions in Pin Descriptions
- Updated customized part numbering nomenclature in [6. Ordering Guide](#)
- Added land pattern drawing

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