Si52212/Si52208/Si52204/Si52202 Data Sheet

12/8/4/2-Output PCI-Express Gen 1/2/3/4/5 and SRIS Clock Generator

The Si52212/08/04/02 are the industry's highest performance and lowest power PCI Express clock generator family for 1.5–1.8 V PCIe Gen 1/2/3/4/5 and SRIS applications. The Si52212, Si52208, and Si52204 can source twelve, eight, and four 100 MHz PCIe differential clock outputs, respectively, plus one 25 MHz LVCMOS reference clock output. The Si52202 can source two 100 MHz PCIe clock outputs only. All differential clock outputs are compliant to PCIe Gen1/2/3/4/5 common clock and separate reference clock architectures specifications.

The Si52212/08/04/02 feature individual hardware control pins for enabling and disabling each output, spread spectrum enable/disable for EMI reduction, and frequency select to select 100, 133, or 200 MHz differential output frequencies. These features can also be controlled via I^2C.

The small footprint and low power consumption make this family of PCIe clock generators ideal for industrial and consumer applications.

For more information about PCI-Express, Silicon Labs' complete PCIe portfolio, application notes, and design tools, including the Silicon Labs PCIe Clock Jitter Tool for PCI-Express compliance, please visit the Silicon Labs PCI Express Learning Center.

Applications

- Servers
- Storage
- Data Centers
- PCIe Add-on Cards
- Network Interface Cards (NIC)
- Graphics Adapter Cards
- Multi-function Printers
- Digital Single-Lens Reflex (DSLR) Cameras
- Digital Still Cameras
- Digital Video Cameras
- Docking Stations

KEY FEATURES

- 12/8/4/2-output low-power, push-pull HCSL compatible PCI-Express Gen 1, Gen 2, Gen 3, Gen 4, Gen 5, and SRIS-compliant outputs
- Low jitter: 0.13 ps rms max, Gen 5
- Individual hardware control pins and I^2C controls for Output Enable, Spread Spectrum Enable and Frequency Select
- Triangular spread spectrum for EMI reduction, down spread 0.25% or 0.5%
- Internal 100 Ω or 85 Ω line matching
- Adjustable output slew rate
- Power down (PWRDNb) function supports Wake-on LAN (except Si52202)
- One non-spread, LVMCOS reference clock output (except Si52202)
- Frequency Select to select 133 MHz or 200 MHz (except Si52202)
- 25 MHz crystal input or clock input
- I^2C support with readback capabilities
- Extended temperature: –40 to 85 °C
- 1.5–1.8 V power supply, with separate VDD and VDD_IO
- Small QFN packages
- Pb-free, RoHS-6 compliant

1. Feature List

- 12/8/4/2-output 100 MHz PCIe Gen 1/2/3/4/5 and SRIS compliant clock generator, with push-pull HCSL output drivers
  - High port count with push-pull HCSL outputs to support highly integrated solution, eliminating external resistors for the HCSL output drivers
- Low jitter of 0.13 ps rms max to meet PCIe Gen5 specifications with design margin
- Low power consumption.
  - Lowest power consumption in the industry for a 2-output PCIe clock generator
- Individual hardware control pins and I^2C controls for Output Enable, Spread Spectrum Enable and Frequency Select
  - Output Enable function easily disables unused outputs for power saving
  - Spread Enable function to turn on/off spread spectrum and to select spread levels, either down spread 0.25% or 0.5%
  - Frequency Select function to select output frequency of 100 MHz, 133 MHz, or 200 MHz (except Si52202 where the output frequency is limited to 100 MHz. Please contact Silicon Labs for 133 MHz or 200 MHz in Si52202)
  - All above functions are controlled by individual hardware pins or I^2C
- Internal 100 Ω or 85 Ω impedance matching
  - Eliminates external line matching resistor to reduce board space
- Adjustable slew rate to improve signal quality for different applications and board designs
- Power down (PWRDNb) function supports Wake-on LAN (except Si52202)
- One non-spread, 25 MHz LVMCOS reference clock output (except Si52202)
  - A buffered 25 MHz LVCMOS clock output to drive ASICS or SoCs on board
- 25 MHz reference input
  - Supports a standard crystal or clock input for flexibility
- I^2C support with readback capabilities
- 1.5–1.8 V power supply with separate VDD and VDD_IO (1.05 to 1.8 V)
- Temperature range: –40 °C to 85 °C
- Small QFN packages to optimize board space. Smallest 2-output PCIe clock generator in the industry
  - 64-pin QFN (9 x 9 mm) : 12-output
  - 48-pin QFN (6 x 6 mm) : 8-output
  - 32-pin QFN (5 x 5 mm) : 4-output
  - 20-pin QFN (3 x 3 mm) : 2-output
- Pb-free, RoHS-6 compliant

2. Ordering Guide

Table 2.1. Si522x Ordering Guide

Number of Outputs	Internal Termination	Part Number	Package Type	Temperature
12-output	100 Ω	Si52212-A01AGM	64-QFN	Extended, –40 to 85 °C
		Si52212-A01AGMR	64-QFN - Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si52212-A02AGM	64-QFN	Extended, –40 to 85 °C
		Si52212-A02AGMR	64-QFN - Tape and Reel	Extended, –40 to 85 °C
8-output	100 Ω	Si52208-A01AGM	48-QFN	Extended, –40 to 85 °C
		Si52208-A01AGMR	48-QFN - Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si52208-A02AGM	48-QFN	Extended, –40 to 85 °C
		Si52208-A02AGMR	48-QFN - Tape and Reel	Extended, –40 to 85 °C
4-output	100 Ω	Si52204-A01BGM	32-QFN	Extended, –40 to 85 °C
		Si52204-A01BGMR	32-QFN - Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si52204-A02BGM	32-QFN	Extended, –40 to 85 °C
		Si52204-A02BGMR	32-QFN - Tape and Reel	Extended, –40 to 85 °C
2-output	100 Ω	Si52202-A01BGM	20-QFN	Extended, –40 to 85 °C
		Si52202-A01BGMR	20-QFN - Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si52202-A02BGM	20-QFN	Extended, –40 to 85 °C
		Si52202-A02BGMR	20-QFN - Tape and Reel	Extended, –40 to 85 °C

2.1 Technical Support

Table 2.2. Technical Support URLs

Frequently Asked Questions	www.silabs.com/Si522xx-FAQ
PCIe Clock Jitter Tool	www.silabs.com/products/timing/pci-express-learning-center
PCIe Learning Center	www.silabs.com/products/timing/pci-express-learning-center
Development Kit	www.silabs.com/products/development-tools/timing/clock/si52204-evb-evaluation-kit.html

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3. Functional Block Diagrams

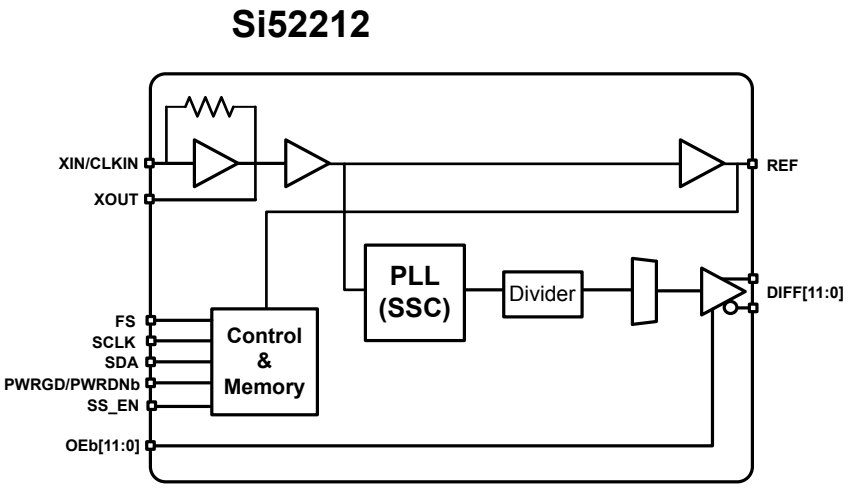


Figure 3.1. Si52212 Block Diagram 12-output, 64-QFN

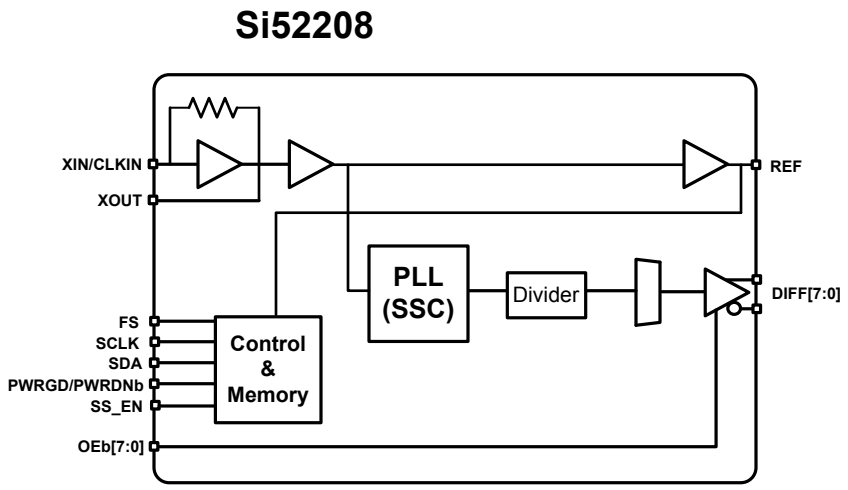


Figure 3.2. Si52208 Block Diagram 8-output, 48-QFN

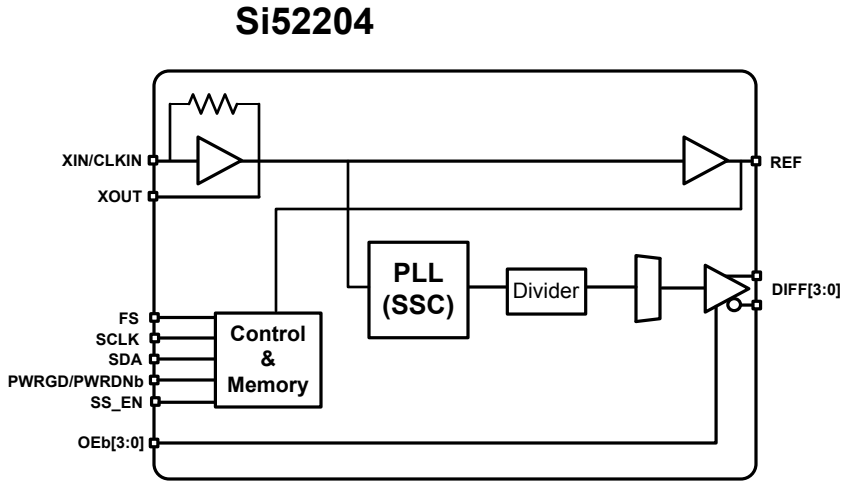


Figure 3.3. Si52204 Block Diagram 4-output, 32-QFN

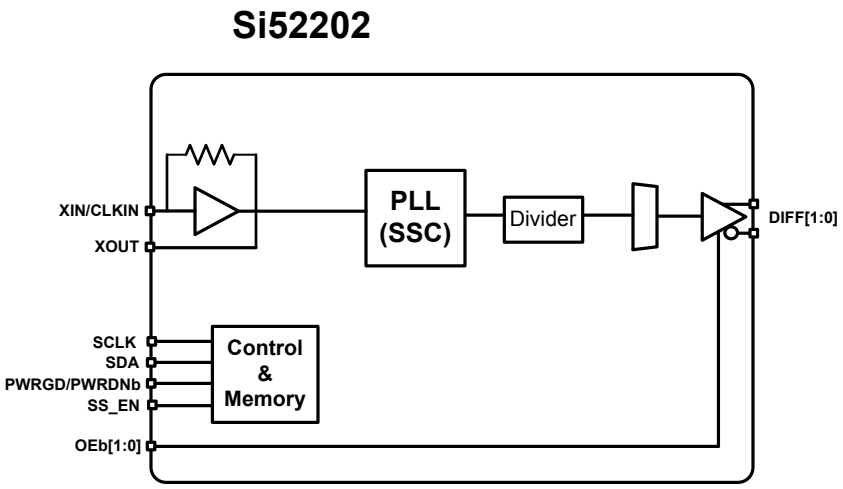


Figure 3.4. Si52202 Block Diagram 2-output, 20-QFN

4. Electrical Specifications

Table 4.1. DC Electrical Specifications (VDD = 1.5 V ±5%)

VDD = VDDR = VDDX = VDDA = 1.5 V ±5%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1.5 V Operating Voltage	VDD	1.5 V ±5%	1.425	1.5	1.575	V
Output Supply Voltage	VDD_IO	Supply voltage for differential Low Power outputs	0.9975	1.05–1.5	1.575	V
1.5 V Input High Voltage	V_{IH}	Control input pins, except SDATA, SCLK	0.75 VDD	—	VDD + 0.3	V
1.5V Input Mid Voltage	V_{IM}	Tri-level control input pins, except SDATA, SCLK	0.4 VDD	0.5 VDD	0.6 VDD	V
1.5 V Input Low Voltage	V_{IL}	Control input pins, except SDA-TA,SCLK	–0.3	—	0.25 VDD	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	1.14	—	3.3	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	—	0.6	V
SDATA, SCLK Sink Current	I_{PULLUP}	At VOL	4	—		mA
Input current	I_{IN}	Single-ended inputs, VIN = GND, VIN = VDD	–5	—	5	uA
	I_{INP}	Single-ended inputs, VIN = 0 V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors	–200	—	200	uA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	LIN		—	—	7	nH
Si52212 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.5 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 0	$I_{DD\_PD\_total}$	All outputs off	—	1.3	1.8	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	1.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.5	mA
Wake-on LAN Current PWRGD_PWRDNb = "0" Byte 2, bit 2 = 1	I_{DD_WOL}	VDD, except VDDA and VDD_IO, all differential outputs off, REF running	—	2.5	3.2	mA
	I_{DD_AWOL}	VDDA, all differential outputs off, REF running	—	0.6	0.75	mA
	I_{DD_IOWOL}	VDD_IO, all differential outputs off, REF running	—	0.3	0.5	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	$I_{DD\_1.5V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	66	77	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	13	14.5	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	46	55.5	mA
Si52208 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.5 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 0	$I_{DD\_PD\_total}$	All outputs off	—	1.3	1.8	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	1.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.5	mA
Wake-on LAN Current PWRGD_PWRDNb = "0" Byte 2, bit 2 = 1	I_{DD_WOL}	VDD, except VDDA and VDD_IO, all differential outputs off, REF running	—	2.5	3.2	mA
	I_{DD_AWOL}	VDDA, all differential outputs off, REF running	—	0.6	0.75	mA
	I_{DD_IOWOL}	VDD_IO, all differential outputs off, REF running	—	0.3	0.5	mA
Dynamic Supply Current	$I_{DD\_1.5V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	48	58.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	11	12.5	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	30	37.5	mA
Si52204 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.5 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 0	$I_{DD\_PD\_total}$	All outputs off	—	1.3	1.8	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	1.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.5	mA
Wake-on LAN Current PWRGD_PWRDNb = "0" Byte 2, bit 2 = 1	I_{DD_WOL}	VDD, except VDDA and VDD_IO, all differential outputs off, REF running	—	2.5	3.2	mA
	I_{DD_AWOL}	VDDA, all differential outputs off, REF running	—	0.6	0.75	mA
	I_{DD_IOWOL}	VDD_IO, all differential outputs off, REF running	—	0.3	0.5	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	$I_{DD\_1.5V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	32	37	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	9.5	11	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	15.5	19	mA
Si52202 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.5 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0"	$I_{DD\_PD\_total}$	All outputs off	—	1.3	1.8	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	1.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.3	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.6	0.5	mA
Dynamic Supply Current	$I_{DD\_1.5V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	22	25.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	7	8	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	8	10	mA

Table 4.2. DC Electrical Specifications (VDD = 1.8 V ±5%)

VDD = VDDR = VDDX = VDDA = 1.8 V ±5%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1.8 V Operating Voltage	VDD	1.8 V ±5%	1.71	1.8	1.89	V
Output Supply Voltage	VDD_IO	Supply voltage for differential Low Power outputs	0.9975	1.05–1.8	1.9	V
1.8 V Input High Voltage	V_{IH}	Control input pins, except SDATA, SCLK	0.75 V_{DD}	—	VDD+0.3	V
1.8 V Input Mid Voltage	V_{IM}	Tri-level control input pins, except SDATA, SCLK	0.4 V_{DD}	0.5 V_{DD}	0.6 VDD	V
1.8 V Input Low Voltage	V_{IL}	Control input pins, except SDA-TA,SCLK	-0.3	—	0.25 VDD	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	1.11	—	3.3	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	—	0.6	V
SDATA, SCLK Sink Current	I_{PULLUP}	At VOL	4	—		mA
Input current	I_{IN}	Single-ended inputs, VIN = GND, VIN = VDD	–5	—	5	uA
	I_{INP}	Single-ended inputs, VIN = 0V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors	–200	—	200	uA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	L_{IN}		—	—	7	nH
Si52212 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.8 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 0	$I_{DD\_PD\_total}$	All outputs off	—	1.4	2.9	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	2.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.9	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.65	mA
Wake-on LAN Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 1	I_{DD_WOL}	VDD, except VDDA and VDD_IO, all differential outputs off, REF running	—	3.0	4.6	mA
	I_{DD_AWOL}	VDDA, all differential outputs off, REF running	—	0.7	0.9	mA
	I_{DD_IOWOL}	VDD_IO, all differential outputs off, REF running	—	0.5	0.65	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	$I_{DD\_1.8V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	67	78	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	13	16	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	47	56.5	mA
Si52208 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.8 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 0	$I_{DD\_PD\_total}$	All outputs off	—	1.4	2.9	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	2.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.9	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.65	mA
Wake-on LAN Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 1	I_{DD_WOL}	VDD, except VDDA and VDD_IO, all differential outputs off, REF running	—	3.0	4.6	mA
	I_{DD_AWOL}	VDDA, all differential outputs off, REF running	—	0.7	0.9	mA
	I_{DD_IOWOL}	VDD_IO, all differential outputs off, REF running	—	0.5	0.65	mA
Dynamic Supply Current	$I_{DD\_1.8V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	49.5	58.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	11.5	14	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	31	38	mA
Si52204 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.8 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 0	$I_{DD\_PD\_total}$	All outputs off	—	1.4	2.9	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	2.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.9	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.65	mA
Wake-on LAN Current PWRGD/PWRDNb = "0" Byte 2, bit 2 = 1	I_{DD_WOL}	VDD, except VDDA and VDD_IO, all differential outputs off, REF running	—	3.0	4.6	mA
	I_{DD_AWOL}	VDDA, all differential outputs off, REF running	—	0.7	0.9	mA
	I_{DD_IOWOL}	VDD_IO, all differential outputs off, REF running	—	0.5	0.65	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	$I_{DD\_1.8V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	33	38	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	10	12	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	16	19.5	mA
Si52202 Current Consumption (VDD = VDDR = VDDX = VDDA = 1.8 V ±5%)						
Power Down Current PWRGD/PWRDNb = "0"	$I_{DD\_PD\_total}$	All outputs off	—	1.4	2.9	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	2.0	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.9	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.65	mA
Dynamic Supply Current	$I_{DD\_1.8V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	24	26.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	8	9	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	7	8.5	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	8	10.5	mA

Table 4.3. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Clock Input						
CLKIN Frequency			—	25	—	MHz
CLKIN Duty Cycle	T_{DC}	Measured at VDD/2	45	—	55	%
CLKIN Rising and Falling Slew Rate	T_R/T_F	Measured between 0.2 VDD and 0.8 VDD	0.5	—	4	V/ns
Input High Voltage	V_{IH}	XIN/CLKIN pin	0.75 V_{DD}	—	—	V
Input Low Voltage	V_{IL}	XIN/CLKIN pin	—	—	0.25 VDD	V
Input Common Mode	V_{COM}	Common mode input voltage	300	—	1000	mV
Input Amplitude	V_{SWING}	Peak to Peak value	300	—	1450	mV
Control Input Pins						
Trise	T_r	Rise time of single-ended control inputs	—	—	5	ns
Tfall	T_f	Fall time of single-ended control inputs	—	—	5	ns
SDATA, SCLK Rise Time	T_{rI2C}	(Max VIL – 0.15) to (Min VIH + 0.15)	—	—	1000	ns
SDATA, SCLK Fall Time	T_{fI2C}	(Min VIH + 0.15) to (Max VIL – 0.15)	—	—	300	ns
I^2C Operating Frequency	F_{maxI^2C}	Maximum I^2C operating frequency	—	—	400	kHz
LVCMOS – REF (VDD = 1.5 V ±5%)						
Long Accuracy	ppm	Variation from reference frequency		0		ppm
Clock Period	T_{PERIOD}	25 MHz output	—	40	—	ns
Slew Rate	T_{rf}	Byte 2[1:0] = 48 (Slowest), 20% to 80% of VDDREF	—	0.5	1.0	V/ns
		Byte 2[1:0] = 49 (Slow), 20% to 80% of VDDREF	—	0.7	1.3	V/ns
		Byte 2[1:0] = 4A (Fast), 20% to 80% of VDDREF	—	0.9	1.5	V/ns
		Byte 2[1:0] = 4B (Fastest), 20% to 80% of VDDREF	—	0.9	1.6	V/ns
Duty Cycle[1]	T_{DC_REF}	VT = VDD/2 V	45	50	55	%
Cycle-to-Cycle Jitter	T_{CCJ_REF}	VT = VDD/2 V using "SLOW" Setting	—	40	70	ps
Phase Jitter	RMS_{REF}	12 kHz to 5 MHz	—	0.35	0.45	ps
REF Noise Floor	T_{J1kHz_REF}	1 kHz offset	—	–132	–124	dBc/Hz
REF Noise Floor	T_{J10kHz_REF}	10 kHz offset to Nyquist	—	–145	–138	dBc/Hz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LVCMOS – REF (VDD = 1.8 V ±5%)						
Long Accuracy	ppm	Variation from reference frequency		0		ppm
Clock Period	T_{PERIOD}	25 MHz output	—	40	—	ns
Slew Rate	T_{rf}	Byte 2[1:0] = 48 (Slowest), 20% to 80% of VDDREF	—	0.7	1.3	V/ns
		Byte 2[1:0] = 49 (Slow), 20% to 80% of VDDREF	—	1.0	1.6	V/ns
		Byte 2[1:0] = 4A (Fast), 20% to 80% of VDDREF	—	1.1	1.9	V/ns
		Byte 2[1:0] = 4B (Fastest), 20% to 80% of VDDREF	—	1.2	2.0	V/ns
Duty Cycle[1]	T_{DC_REF}	VT = VDD/2 V	45	50	55	%
Cycle-to-Cycle Jitter	T_{CCJ_REF}	VT = VDD/2 V using "SLOW" Setting	—	30	50	ps
Phase Jitter	RMS_{REF}	12 kHz to 5 MHz	—	0.3	0.4	ps
REF Noise Floor	TJ_{1kHz_REF}	1 kHz offset	—	–132	–124	dBc
REF Noise Floor	TJ_{10kHz_REF}	10 kHz offset to Nyquist	—	–145	–139	dBc
DIFF HCSL						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	50	55	%
Output-to-Output Skew	T_{SKEW}	Measured at 0 V differential	—	10	50	ps
Slew Rate	T_R/T_F	Measured differentially from ±150 mV (fast setting)	—	2.4	3.7	V/ns
		Measured differentially from ±150 mV (slow setting)	—	1.9	2.9	V/ns
Slew Rate Matching	Delta T_R/T_F		—	2	10	%
Max modulation frequency df/dt	$T_{max\text{-}freqmod\text{-}slew}$		—	—	1250	ppm/usec
Voltage High	V_{HIGH}		600	—	850	mV
Voltage Low	V_{LOW}		–150	—	150	mV
Max Voltage	V_{MAX}		—	750	1150	mV
Min Voltage	V_{MIN}		–300	0	—	mV
Crossing Point Voltage	V_{OX}	Absolute crossing point voltage at 0.7 V Swing	250	—	550	mV
Crossing Point Voltage (var)	V_{OX_DELTA}	Variation of VOX over all rising clock edges	—	35	70	mV
Modulation Frequency	F_{MOD}		30	31.5	33	kHz
Enable/Disable and Setup						
Clock Stabilization from Power-up	T_{STABLE}	Min ramp rate 200V/s	—	1	5	ms

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OE_b Latency	T_{OEBLAT}	Differential outputs start after OE_b assertion Differential outputs stop after OE_b deassertion	—	2	3.5	clocks
PWRDNb Latency to differential outputs enable	T_{PWRDNb}	Differential outputs enable after PD_b de-assertion	—	490	520	µs

Note:
1. This is for XTAL mode only. For CLKIN mode, there would be a duty cycle distortion spec of ±0.5 ns.

Table 4.4. PCIe and Intel QPI Jitter Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Jitter Limit	Unit
DIFF HCSL							
Cycle to Cycle Jitter	J_{CCJ}	Measured at 0 V differential	—	16	23		ps (pk-pk)
PCIe Gen 1 Pk-Pk Jitter	J_{Pk-Pk}	PCIe Gen 1	0	25	33	86	ps (pk-pk)
PCIe Gen 2 Phase Jitter	$J_{RMSGEN2}$	10 kHz < F < 1.5 MHz	0	0.18	0.24	3	ps (RMS)
		1.5 MHz < F < Nyquist	0	1.4	1.7	3.1	ps (RMS)
PCIe Gen 3 Phase Jitter	$J_{RMSGEN3}$	Includes PLL BW 2–4 MHz, CDR = 10 MHz	—	0.3	0.38	1.0	ps (RMS)
PCIe Gen 3 SRIS[1] Phase Jitter	$J_{RMSGen3\_SRIS}$	Includes PLL BW 2–4 MHz, CDR = 10 MHz	—	0.37	0.44	0.7	ps (RMS)
PCIe Gen 4 Phase Jitter	$J_{RMSGen4}$	Includes PLL BW 2–4 MHz, CDR = 10 MHz	—	0.3	0.38	0.5	ps (RMS)
PCIe Gen 4 SRIS[1] Phase Jitter	$J_{RMSGen4\_SRIS}$	Includes PLL BW 2–4 MHz, CDR = 10 MHz	—	0.38	0.45	0.5	ps (RMS)
PCIe Gen 5 [5] Phase Jitter	$J_{RMSGen5}$	Includes PLL BW 500 kHz–1.8 MHz, CDR = 20 MHz	—	0.11	0.135	0.15	ps (RMS)
PCIe Gen 5 SRIS[1] Phase Jitter	$J_{RMSGen5\_SRIS}$	Includes PLL BW 500 kHz–1.8 MHz, CDR = 20 MHz	—	0.11	0.13	0.18	ps (RMS)

Parameter	Symbol	Condition	Min	Typ	Max	Jitter Limit	Unit
PSNR[2]							
Spurs Induced by External Power Supply Noise on VDDA, 100 mVpp Ripple	$PSNR_{1.8V}$	100 kHz	—	–63.4	—	—	dBc
		200 kHz	—	–61.5	—	—	dBc
		300 kHz	—	–59.1	—	—	dBc
		500 kHz	—	–54.5	—	—	dBc
		1 MHz	—	–50.4	—	—	dBc
	$PSNR_{1.5V}$	100 kHz	—	–65.9	—	—	dBc
		200 kHz	—	–63.9	—	—	dBc
		300 kHz	—	–60.3	—	—	dBc
		500 kHz	—	–53.5	—	—	dBc
		1 MHz	—	–46.0	—	—	dBc
Intel QPI Specifications for 100 MHz and 133 MHz							
Intel QPI and SMI REFCLK accummulated jitter[3, 4]	J_{RMSQPI_SMI}	8 Gb/s, 100 MHz, 12UI	—	0.13	0.22	0.3	ps (RMS)
Intel QPI and SMI REFCLK accummulated jitter[3, 4]	J_{RMSQPI_SMI}	9.6 Gb/s, 100 MHz, 12UI	—	0.11	0.19	0.2	ps (RMS)
Intel QPI & SMI REFCLK accummulated jitter[3, 6]	J_{RMSQPI_SMI}	6.4 Gb/s, 100/133 MHz, 12UI, 7.8M	—	0.15	0.35	0.5	ps (RMS)

Note:

1. The SRIS jitter limit is the system RefClk simulation budget divided by sqrt (2) for equal allocation of uncorrelated jitter between two clocks.
2. For PSNR testing methodology, please see "AN491: Power Supply Rejection for Low-Jitter Clocks".
3. Post processed evaluation through Intel supplied Matlab scripts.
4. Measuring on 100 MHz output using the template file in the PCIe Jitter Tool.
5. Based on PCI Express® Base Specifications Revision 5.0 Version 0.7.
6. Measuring on 100 MHz, 133 MHz outputs using the template file in the PCIe Jitter Tool. Visit www.pcisig.com for complete PCIe specifications.

Table 4.5. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Units
Si52202 - 20-QFN				
Thermal Resistance, Junction to Ambient[1]	θ_{JA}	Still Air Air Flow 1 m/s Air Flow 2 m/s	60 56 54.4	°C/W
Thermal Resistance, Junction to Case[1]	θ_{JC}		10.8	°C/W
Thermal Resistance, Junction to Board[1]	θ_{JB}		34.1	°C/W
Thermal Resistance, Junction to Top Center[1]	Ψ_{JT}		3.1	°C/W
Thermal Resistance, Junction to Board[1]	Ψ_{JB}		33.9	°C/W
Si52204 - 32-QFN				
Thermal Resistance, Junction to Ambient[2]	θ_{JA}	Still Air Air Flow 1 m/s Air Flow 2 m/s	50.3 47 45.6	°C/W
Thermal Resistance, Junction to Case[2]	θ_{JC}		10.3	°C/W
Thermal Resistance, Junction to Board[2]	θ_{JB}		30.9	°C/W
Thermal Resistance, Junction to Top Center[2]	Ψ_{JT}		2.3	°C/W
Thermal Resistance, Junction to Board[2]	Ψ_{JB}		30.9	°C/W
Si52208 - 48-QFN				
Thermal Resistance, Junction to Ambient[3]	θ_{JA}	Still Air Air Flow 1 m/s Air Flow 2 m/s	27.9 24.5 23.5	°C/W
Thermal Resistance, Junction to Case[3]	θ_{JC}		17	°C/W
Thermal Resistance, Junction to Board[3]	θ_{JB}		13.4	°C/W
Thermal Resistance, Junction to Top Center[3]	Ψ_{JT}		0.5	°C/W
Thermal Resistance, Junction to Board[3]	Ψ_{JB}		13.1	°C/W
Si52212 - 64-QFN				
Thermal Resistance, Junction to Ambient[4]	θ_{JA}	Still Air Air Flow 1 m/s Air Flow 2 m/s	27.2 23.9 22.5	°C/W
Thermal Resistance, Junction to Case[4]	θ_{JC}		13.7	°C/W
Thermal Resistance, Junction to Board[4]	θ_{JB}		14.4	°C/W
Thermal Resistance, Junction to Top Center[4]	Ψ_{JT}		0.5	°C/W
Thermal Resistance, Junction to Board[4]	Ψ_{JB}		14.2	°C/W

Parameter	Symbol	Test Condition	Value	Units

Note:

1. Based on a 4 layer, PCB with Dimension 3"x4.5". PCB Thickness of 1.6mm. PCB Center Land with 4 Via to top plane.
2. Based on PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm. PCB Center Land with 4 Via to top plane.
3. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm. PCB Center Land with 9 Via to top plane.
4. Based on 4 Layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm. PCB Center Land with 25 Via to top plane.

Table 4.6. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	VDD_1.8V	Functional	—	—	2.5	V
Input Voltage	VIN	Relative to VSS	–0.5	—	VDD + 0.5	V
Input High Voltage I^2C	VIH_I2C	SDATA and SCLK	—		3.6	V
Temperature, Storage	TS	Non-functional	–65	—	150	Celsius
Temperature, Operating Ambient	T_A	Functional	–40	—	85	Celsius
Temperature, Junction	T_J	Functional	—	—	125	Celsius
ESD Protection (Human Body Model)	ESDHBM	JEDEC (JESD 22-A114)	–2000	—	2000	V
Flammability Rating	UL-94	UL (Class)	V–0			

Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

5. Functional Description

5.1 Crystal Recommendations

The clock device requires a parallel resonance crystal.

Table 5.1. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Shunt Cap (max)	Motional (max)	Tolerance (max)	Stability (max)	Aging (max)
25 MHz	AT	Parallel	8–15 pF	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

5.2 Crystal Loading

Crystal loading is critical in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

The figure below shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal.

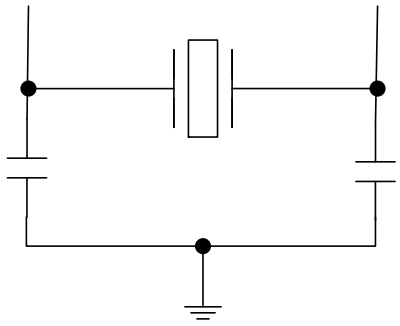


Figure 5.1. Crystal Capacitive Clarification

5.3 Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. The total capacitance on both sides is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

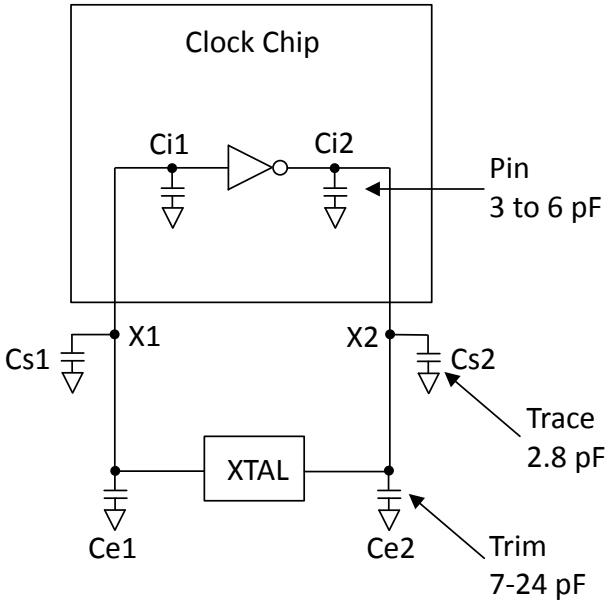


Figure 5.2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2:

Load Capacitance (each side)

$$Ce = 2 \times CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci : Internal capacitance (lead frame, bond wires, etc.)

5.4 Power Supply Filtering Recommendations

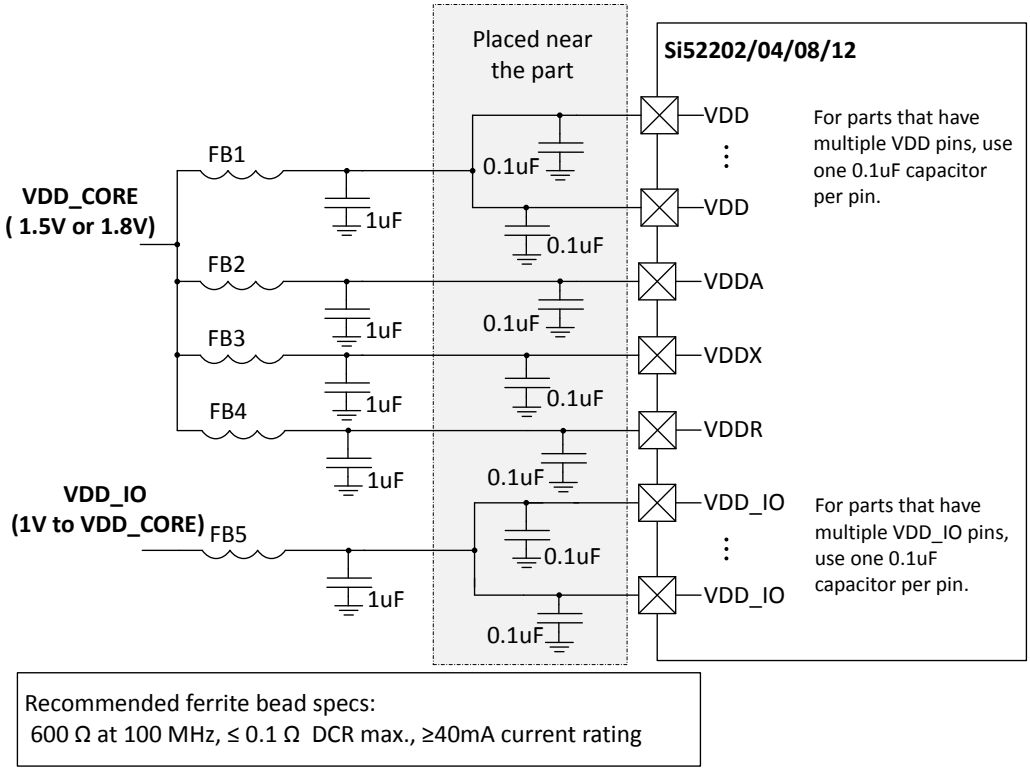


Figure 5.3. Power Supply Filtering

Separate out each type of VDD (VDD, VDDA, VDDX, VDDR, and VDD_IO) using ferrite beads. Then, for each VDD type use one 1 µF bulk capacitor along with an additional 0.1 µF capacitor for each individual VDD pin. All VDD Core (VDD, VDDA, VDDX, and VDDR) pins should be tied to the same voltage, either 1.8 V or 1.5 V. The VDD_IO pins can be tied to a voltage between 1 V and the selected VDD Core voltage. Note, the VDD_IO pins must all be tied to the same voltage.

5.5 PWRGD/PWRDNb (Power Down) Pin

The PWRGD/PWRDNb pin is a dual-function pin. During initial power up, the pin functions as the PWRGD pin. Upon the first power up, if the PWRGD pin is low, all outputs, the crystal oscillator, and the I^2C logics will be disabled. Once the PWRGD pin has been sampled high by the clock chip, the pin assumes a PWRDNb functionality. When the pin has assumed a PWRDNb functionality and is pulled low, the device will be placed in power down mode. The assertion and dessertion of PWRDNb is asynchronous. This pin has a 100 kΩ internal pull-up.

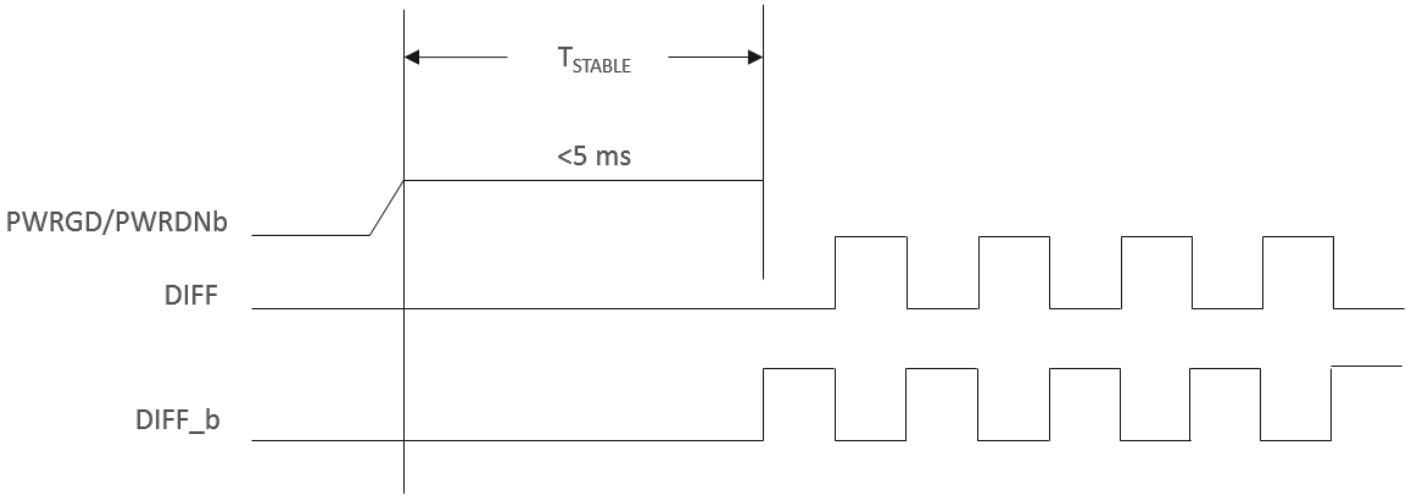


Figure 5.4. Initial Sample High of PWRGD/PWRDNb After Power Up

5.6 PWRDNb (Power Down) Assertion

The PWRDNb pin is an asynchronous active low input used to disable all output clocks in a glitch-free manner. In power down mode, all outputs, the crystal oscillator, and the I^2C logic are disabled. In cases where the REF PWRDN (Byte 2, bit 2) is set to 1, the crystal oscillator and REF output will still be enabled. All disabled outputs will be driven low.

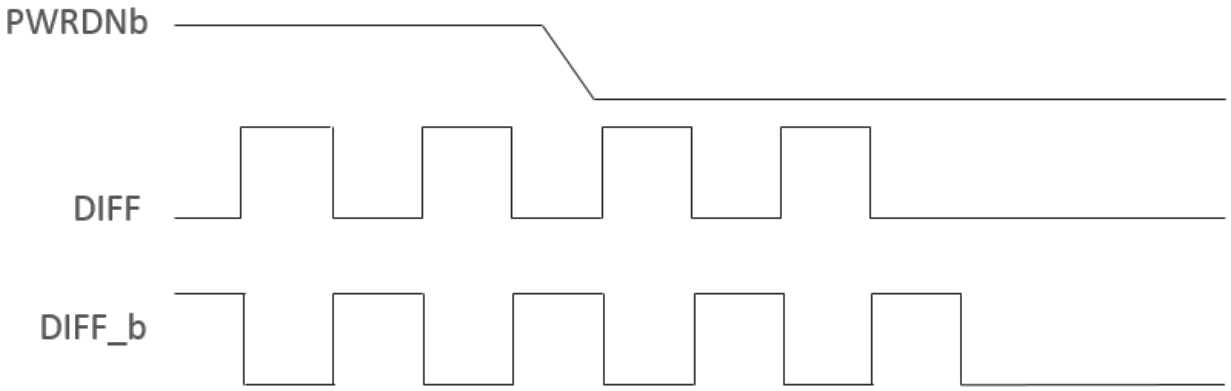


Figure 5.5. PWRDNb Assertion

5.7 PWRDNb (Power Down) Deassertion

When a valid rising edge on PWRGD/PWRDNb pin is applied, all outputs are enabled in a glitch-free manner within 520 µs.

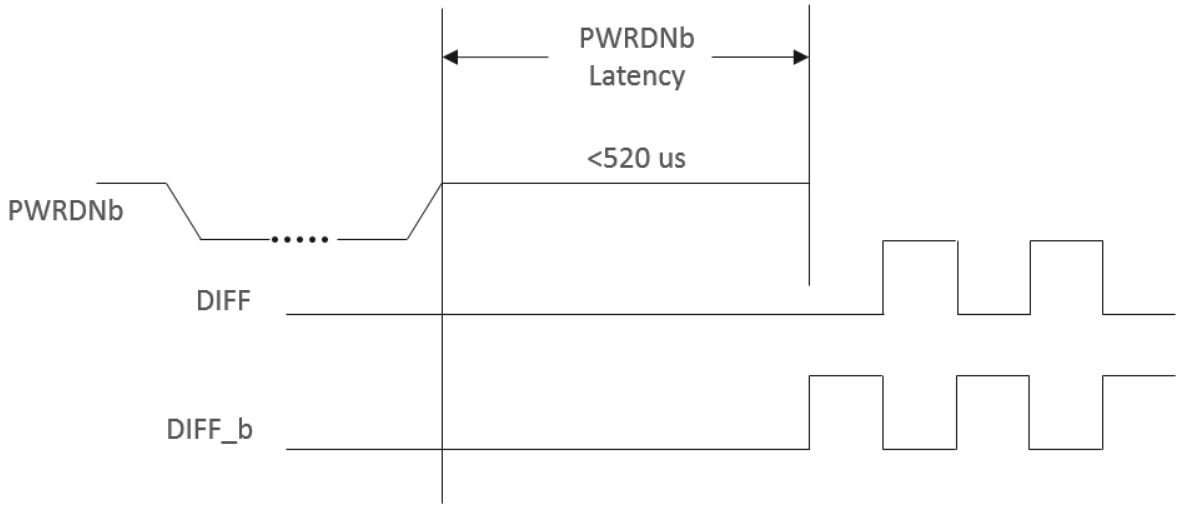


Figure 5.6. Subsequent Deassertion of PWRDNb

5.8 OEb Pin

The OEb pin is an active low input used to enable and disable the output clock. To enable the output clock, the OEb pin needs to be logic low, and I^2C OE bit needs to be logic high. By default, the OEb pin is set to logic low, and I^2C OE bit is set to logic high.There are two methods to disable the output clock: the OEb pin is pulled to a logic high, or the I^2C OE bit is set to a logic low. This pin has a 100 kΩ internal pull-down.

5.9 OEb Assertion

The OEb pin is an active low input used for synchronous stopping and starting the respective output clock while the rest of the clock generator continues to function. The assertion of the OEb function is achieved by pulling the OEb pin low while the I^2C OE bit is high, which causes the respective stopped output to resume normal operation. No short or stretched clock pulses are produced when the clocks resume.

5.10 OEb Deassertion

The OEb function is deasserted by pulling high or writing the I^2C OE bit to a logic low. The corresponding output is stopped cleanly and the final output state is driven low.

5.11 FS Pin

The FS pin will select 0 = 100 MHz, mid = 200 MHz, and 1 = 133 MHz. This is a tri-state pin, which has a weak internal pull-down of approximately 100 kΩ.

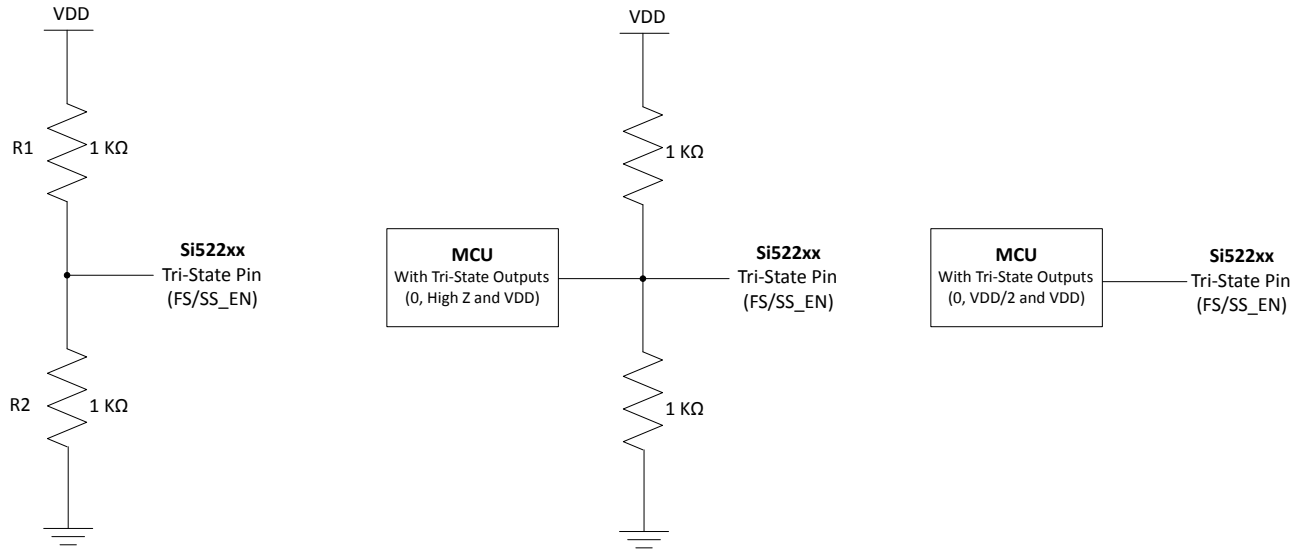
The default output frequency is 100 MHz.

5.12 SS_EN Pin

The SS_EN pin will select 0 = –0.25% spread, mid = Spread is off, and 1 = –0.5% spread. This is a tri-state pin, which has a weak internal pull-up of approximately 100 kΩ.

The default is –0.5% spread.

5.13 Recommendations for Driving Tri-State Pins



Static Option
User can remove either R1, R2, or neither to constantly maintain low, high, or mid levels respectively

Tri-State Dynamic Option
User can use a MCU with strong Tri-State outputs to drive the Tri-State input pin. 1 KΩ resistors should be adequate for most MCU drivers.

3-Level Dynamic Option
A MCU with 3-level output capability can be directly connected to the Tri-State input pin to drive it either low, high, or mid level.

Figure 5.7. Tri-State Pin Schematics

5.14 REF/SA Pin

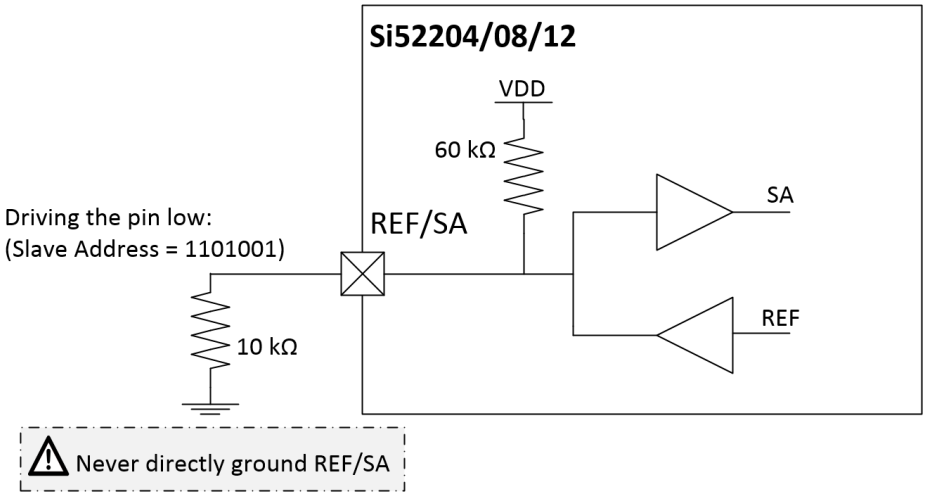


Figure 5.8. REF/SA Pin Function

The REF/SA pin is a dual-function input/output pin.

The SA functionality sets the Slave Address of the part. This address is latched to the value of the pin when the part initially powers up. See Table 8.1 SA State on First Application of PWRDNb on page 32 for the available addresses. By default, the internal 60 kΩ pull-up resistor will set SA to a value of 1. To drive the pin low, use a 10 kΩ pull-down resistor.

After the I^2C address is latched on first power up, the REF/SA pin assumes its REF functionality. In REF mode, it will output a 25 MHz LVCMOS signal.

6. Test and Measurement Setup

The following diagrams show the test load configuration for the differential clock signals.

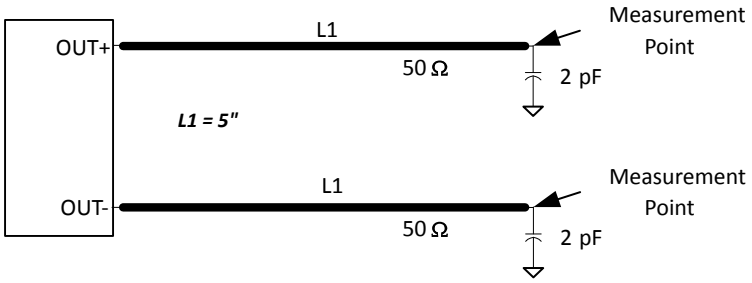


Figure 6.1. 0.7 V Differential Load Configuration

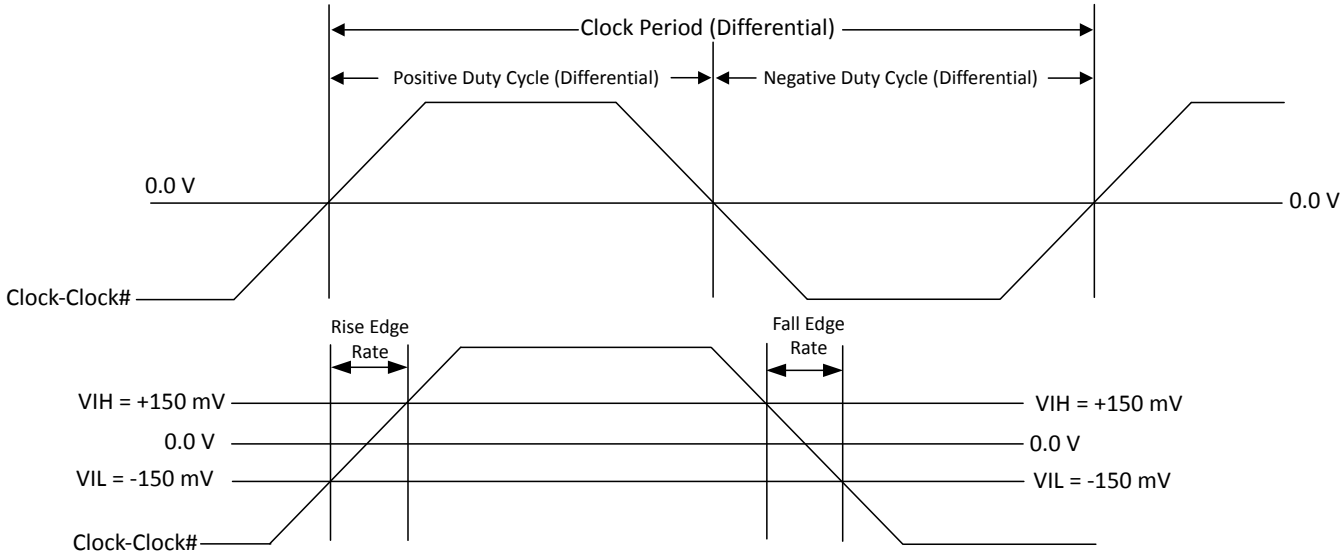


Figure 6.2. Differential Output Signals (for AC Parameters Measurement)

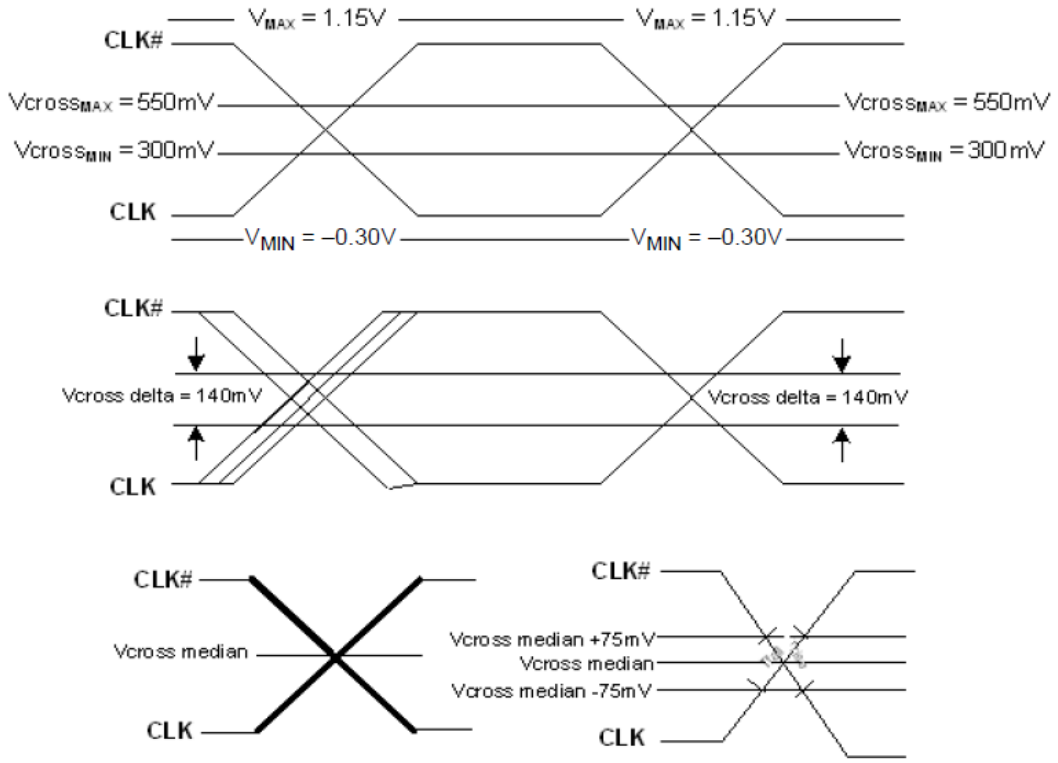


Figure 6.3. Single-Ended Measurement for Differential Output Signals (for AC Parameters Measurement)

7. PCIe Clock Jitter Tool

The PCIe Clock Jitter Tool is designed to enable users to quickly and easily take jitter measurements for PCIe Gen1/2/3/4/5 and SRNS/SRIS. This software removes all the guesswork for PCIe Gen1/2/3/4/5 and SRNS/SRIS jitter measurements and margins in board designs. This software tool will provide accurate results in just a few clicks, and is provided in an executable format to support various common input waveform files, such as .csv, .wfm, and .bin. The easy-to-use GUI and helpful tips guide users through each step. Release notes and other documentation are also included in the software package.

Download it for free at http://www.silabs.com/pcie-learningcenter.

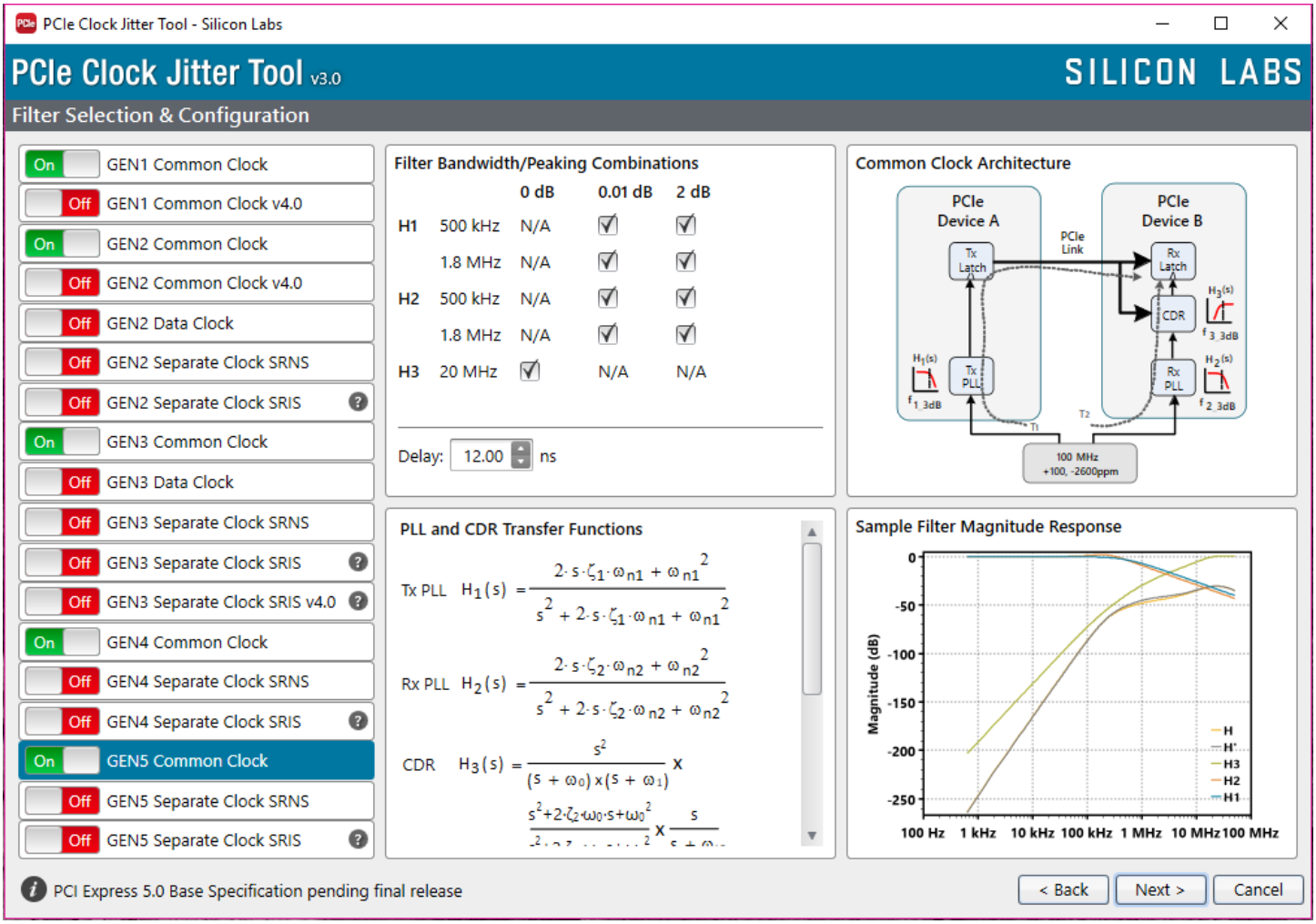


Figure 7.1. PCIe Clock Jitter Tool

8. Control Registers

8.1 I²C Interface

To enhance the flexibility and function of the clock synthesizer, an I²C interface is provided. Through the I²C interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the I²C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

8.2 Block Read/Write

The clock driver I²C protocol accepts block write and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. The block write and block read protocol is outlined in Table 8.2 Block Read and Block Write Protocol on page 32.

8.3 Block Read

After the slave address is sent with the R/W condition bit set, the command byte is sent with the MSB = 0. The slave acknowledges the register index in the command byte. The master sends a repeat start function. After the slave acknowledges this, the slave sends the number of bytes it wants to transfer (>0 and ≤7). The master acknowledges each byte except the last and sends a stop condition.

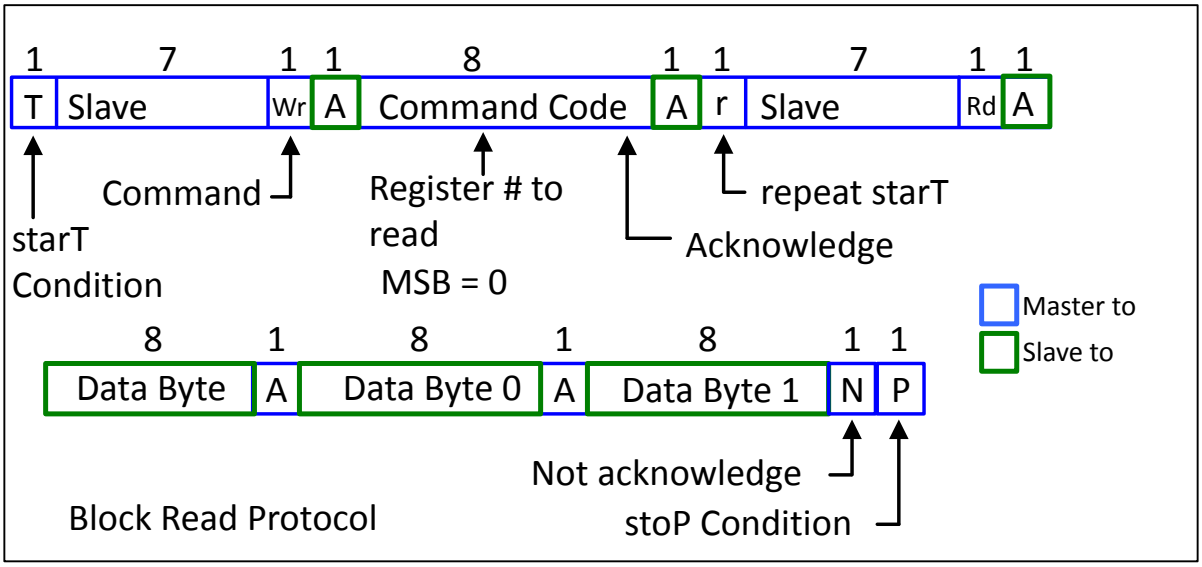


Figure 8.1. Block Read Protocol

8.4 Block Write

After the slave address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate the register at which to start the transfer. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a block write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 7. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

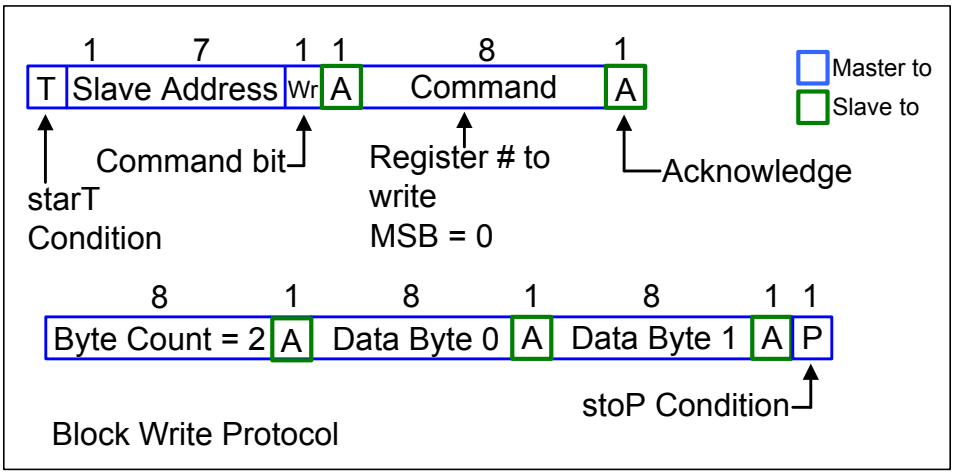


Figure 8.2. Block Write Protocol

8.5 Byte Read/Write

Reading or writing a register in an I^2C slave device in byte mode always involves specifying the register number. Refer to Table 8.3 Byte Read and Byte Write Protocol on page 33 for byte read and byte write protocol.

8.6 Byte Read

The standard byte read is as shown in the figure below. It is an extension of the byte write. The write start condition is repeated; then, the slave device starts sending data, and the master acknowledges it until the last byte is sent. The master terminates the transfer with a Nack, then a stop condition. For byte operation, the MSB bit of the command byte must be set. For block operations, the MSB bit must be set low. If the bit is not set low, the next byte must be the byte transfer count.

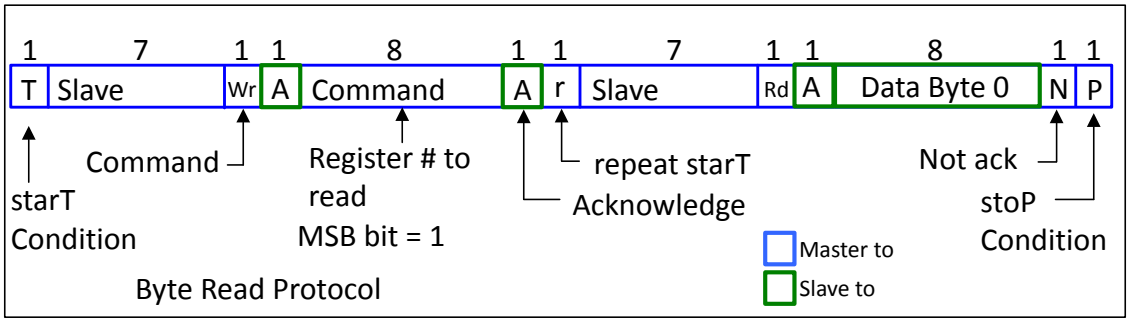


Figure 8.3. Byte Read Protocol

8.7 Byte Write

The figure below illustrates a simple, typical byte write. For byte operation, the MSB bit of the command byte must be set high. For block operations, the MSB bit must be set. If the bit is not set, the next byte must be the byte transfer count. The count can be between 1 and 32. It is not allowed to be zero or to exceed 32.

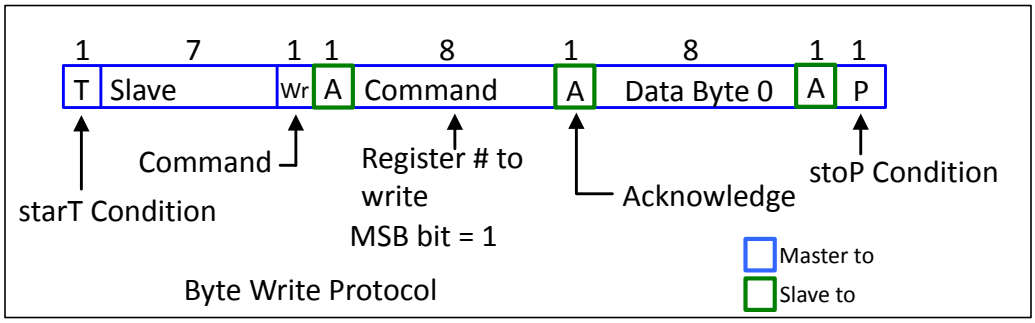


Figure 8.4. Byte Write Protocol

8.8 Data Protocol

The clock driver I^2C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operations, the system controller can access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The block write and block read protocol is outlined in Table 8.2 Block Read and Block Write Protocol on page 32 while Table 8.3 Byte Read and Byte Write Protocol on page 33 outlines byte write and byte read protocol. SA is the address select for I^2C. When the part is powered up, SA will be latched to select the I^2C address.

Table 8.1. SA State on First Application of PWRDNb

Description	SA	Address
State of SA on first deassertion of PWRDNb	0	1101001
	1	1101010

Table 8.2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address—7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code—8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count—8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 8.3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

8.9 Register Tables

8.9.1 Si52212 Registers

Table 8.4. Control Register 0. Byte 0

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	DIFF7_OE	Disabled	Enabled	RW	1	Output enable for DIFF[7]
6	DIFF6_OE	Disabled	Enabled	RW	1	Output enable for DIFF[6]
5	DIFF5_OE	Disabled	Enabled	RW	1	Output enable for DIFF[5]
4	DIFF4_OE	Disabled	Enabled	RW	1	Output enable for DIFF[4]
3	DIFF3_OE	Disabled	Enabled	RW	1	Output enable for DIFF[3]
2	DIFF2_OE	Disabled	Enabled	RW	1	Output enable for DIFF[2]
1	DIFF1_OE	Disabled	Enabled	RW	1	Output enable for DIFF[1]
0	DIFF0_OE	Disabled	Enabled	RW	1	Output enable for DIFF[0]

Table 8.5. Control Register 1. Byte 1

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	DIFF11_OE	Disabled	Enabled	RW	1	Output enable for DIFF[11]
6	DIFF10_OE	Disabled	Enabled	RW	1	Output enable for DIFF[10]
5	DIFF9_OE	Disabled	Enabled	RW	1	Output enable for DIFF[9]
4	DIFF8_OE	Disabled	Enabled	RW	1	Output enable for DIFF[8]
3	Reserved				0	Reserved
2					0	
1	SS_EN_READ1			R	0	Spread Enable software readback 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5% The value of SS_EN_READ is latched on power-up.
0	SS_EN_READ0			R	0	

Table 8.6. Control Register 2. Byte 2

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SS_EN_SW_HW_CTRL	Read back Byte 1[1:0]	SS control by Byte 2 [6:5]	RW	0	Enable software control of spread
6	SS_EN_SW1			RW	0	Software control of spread 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5%
5	SS_EN_SW0			RW	1	
4	Reserved				0	Reserved
3	REF_OE	Disabled	Enabled	RW	1	Output Enable for REF
2	REF PWRDN	REF output is disabled in Power Down.	REF output is enabled in Power Down	RW	0	Wake-on LAN for REF. To have REF output enabled in Power Down, REF_OE needs to be enabled at the same time.

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
1	REF_SLR			RW	0	REF Output Slew Rate Control 00 = Slowest; 01 = Slow; 10 = Fast; 11 = Fastest
0				RW	1	

Table 8.7. Control Register 3. Byte 3

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SR_SEL_DIFF7	Slow setting	Fast setting	RW	1	Slew rate control for DIFF7
6	SR_SEL_DIFF6	Slow setting	Fast setting	RW	1	Slew rate control for DIFF6
5	SR_SEL_DIFF5	Slow setting	Fast setting	RW	1	Slew rate control for DIFF5
4	SR_SEL_DIFF4	Slow setting	Fast setting	RW	1	Slew rate control for DIFF4
3	SR_SEL_DIFF3	Slow setting	Fast setting	RW	1	Slew rate control for DIFF3
2	SR_SEL_DIFF2	Slow setting	Fast setting	RW	1	Slew rate control for DIFF2
1	SR_SEL_DIFF1	Slow setting	Fast setting	RW	1	Slew rate control for DIFF1
0	SR_SEL_DIFF0	Slow setting	Fast setting	RW	1	Slew rate control for DIFF0

Table 8.8. Control Register 4. Byte 4

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SR_SEL_DIFF11	Slow setting	Fast setting	RW	1	Slew rate control for DIFF11
6	SR_SEL_DIFF10	Slow setting	Fast setting	RW	1	Slew rate control for DIFF10
5	SR_SEL_DIFF9	Slow setting	Fast setting	RW	1	Slew rate control for DIFF9
4	SR_SEL_DIFF8	Slow setting	Fast setting	RW	1	Slew rate control for DIFF8
3	AMP			RW	1	DIFF Differential Outputs Amplitude Adjustment. 0110 : 600 mV 0111 : 650 mV 1000 : 700 mV 1001 : 750 mV 1010 : 800 mV 1011 : 850 mV
2	AMP			RW	0	
1	AMP			RW	0	
0	AMP			RW	0	

Table 8.9. Control Register 5. Byte 5

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Rev Code [7:4]			R	0	Revision Code
6				R	0	
5				R	0	
4				R	0	

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
3	Vendor ID[3:0]			R	1	Vendor Identification Code
2				R	0	
1				R	0	
0				R	0	

Table 8.10. Control Register 6. Byte 6

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Programming ID [7:0]			R	0	Programming ID (Internal Only)
6				R	0	
5				R	0	
4				R	0	
3				R	0	
2				R	0	
1				R	0	
0				R	0	

8.9.2 Si52208 Registers

Table 8.11. Control Register 0. Byte 0

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	DIFF4_OE	Disabled	Enabled	RW	1	Output enable for DIFF_4
5	DIFF3_OE	Disabled	Enabled	RW	1	Output enable for DIFF_3
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2	DIFF2_OE	Disabled	Enabled	RW	1	Output enable for DIFF_2
1	DIFF1_OE	Disabled	Enabled	RW	1	Output enable for DIFF_1
0	DIFF0_OE	Disabled	Enabled	RW	1	Output enable for DIFF_0

Table 8.12. Control Register 1. Byte 1

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	DIFF7_OE	Disabled	Enabled	RW	1	Output enable for DIFF_7
6	DIFF6_OE	Disabled	Enabled	RW	1	Output enable for DIFF_6
5	Reserved				0	Reserved
4	DIFF5_OE	Disabled	Enabled	RW	1	Output enable for DIFF_5
3	Reserved				0	Reserved
2					0	
1	SS_EN_READ1			R	0	Spread Enable software readback 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5% The value of SS_EN_READ is latched on power-up.
0	SS_EN_READ0			R	0	

Table 8.13. Control Register 2. Byte 2

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SS_EN_SW_HW_CTRL	Read back Byte 1[1:0]	SS control by Byte 2 [6:5]	RW	0	Enable software control of spread
6	SS_EN_SW1			RW	0	Software control of spread 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5%
5	SS_EN_SW0			RW	1	
4	Reserved				0	Reserved
3	REF_OE	Disabled	Enabled	RW	1	Output Enable for REF
2	REF PWRDN	REF output is disabled in Power Down.	REF output is enabled in Power Down	RW	0	Wake-on LAN for REF. To have REF output enabled in Power Down, REF_OE needs to be enabled at the same time.
1	REF_SLR			RW	0	REF Output Slew Rate Control 00 = Slowest; 01 = Slow; 10 = Fast; 11 = Fastest
0				RW	1	

Table 8.14. Control Register 3. Byte 3

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved			RW	1	Reserved
6	SR_SEL_DIFF_4	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_4
5	SR_SEL_DIFF_3	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_3
4	Reserved			RW	1	Reserved
3	Reserved			RW	1	Reserved
2	SR_SEL_DIFF_2	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_2
1	SR_SEL_DIFF_1	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_1
0	SR_SEL_DIFF_0	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_0

Table 8.15. Control Register 4. Byte 4

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SR_SEL_DIFF_7	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_7
6	SR_SEL_DIFF_6	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_6
5	Reserved			RW	1	Reserved
4	SR_SEL_DIFF_5	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_5
3	AMP			RW	1	DIFF Differential Outputs Amplitude Adjustment. 0110 : 600 mV 0111 : 650 mV 1000 : 700 mV 1001 : 750 mV 1010 : 800 mV 1011 : 850 mV
2	AMP			RW	0	
1	AMP			RW	0	
0	AMP			RW	0	

Table 8.16. Control Register 5. Byte 5

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Rev Code [7:4]			R	0	Revision Code
6				R	0	
5				R	0	
4				R	0	
3	Vendor ID[3:0]			R	1	Vendor Identification Code
2				R	0	
1				R	0	
0				R	0	

Table 8.17. Control Register 6. Byte 6

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Programming ID [7:0]			R	0	Programming ID (Internal Only)
6				R	0	
5				R	0	
4				R	0	
3				R	0	
2				R	0	
1				R	0	
0				R	0	

8.9.3 Si52204 Registers

Table 8.18. Control Register 0. Byte 0

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	DIFF2_OE	Disabled	Enabled	RW	1	Output enable for DIFF_2
5	DIFF1_OE	Disabled	Enabled	RW	1	Output enable for DIFF_1
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2	DIFF0_OE	Disabled	Enabled	RW	1	Output enable for DIFF_0
1	Reserved			RW	0	Reserved
0	Reserved			RW	0	Reserved

Table 8.19. Control Register 1. Byte 1

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	Reserved				0	Reserved
5	Reserved				0	Reserved
4	DIFF3_OE	Disabled	Enabled	RW	1	Output enable for DIFF_3
3	Reserved				0	Reserved
2					0	
1	SS_EN_READ1			R	0	Spread Enable software readback 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5% The value of SS_EN_READ is latched on power-up.
0	SS_EN_READ0			R	0	

Table 8.20. Control Register 2. Byte 2

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SS_EN_SW_HW_CTRL	Read back Byte 1[1:0]	SS control by Byte 2 [6:5]	RW	0	Enable software control of spread
6	SS_EN_SW1			RW	0	Software control of spread 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5%
5	SS_EN_SW0			RW	1	
4	Reserved				0	Reserved
3	REF_OE	Disabled	Enabled	RW	1	Output Enable for REF
2	REF PWRDN	REF output is disabled in Power Down.	REF output is enabled in Power Down	RW	0	Wake-on LAN for REF. To have REF output enabled in Power Down, REF_OE needs to be enabled at the same time.
1	REF_SLR			RW	0	REF Output Slew Rate Control 00 = Slowest; 01 = Slow; 10 = Fast; 11 = Fastest
0				RW	1	

Table 8.21. Control Register 3. Byte 3

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved			RW	1	Reserved
6	SR_SEL_DIFF_2	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_2
5	SR_SEL_DIFF_1	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_1
4	Reserved			RW	1	Reserved
3	Reserved			RW	1	Reserved
2	SR_SEL_DIFF_0	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_0
1	Reserved			RW	1	Reserved
0	Reserved			RW	1	Reserved

Table 8.22. Control Register 4. Byte 4

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved			RW	1	Reserved
6	Reserved			RW	1	Reserved
5	Reserved			RW	1	Reserved
4	SR_SEL_DIFF_3	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_3
3	AMP			RW	1	DIFF Differential Outputs Amplitude Adjustment. 0110 : 600 mV 0111 : 650 mV 1000 : 700 mV 1001 : 750 mV 1010 : 800 mV 1011 : 850 mV
2	AMP			RW	0	
1	AMP			RW	0	
0	AMP			RW	0	

Table 8.23. Control Register 5. Byte 5

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Rev Code [7:4]			R	0	Revision Code
6				R	0	
5				R	0	
4				R	0	
3	Vendor ID[3:0]			R	1	Vendor Identification Code
2				R	0	
1				R	0	
0				R	0	

Table 8.24. Control Register 6. Byte 6

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Programming ID [7:0]			R	0	Programming ID (Internal Only)
6				R	0	
5				R	0	
4				R	0	
3				R	0	
2				R	0	
1				R	0	
0				R	0	

8.9.4 Si52202 Registers

Table 8.25. Control Register 0. Byte 0

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	DIFF0_OE	Disabled	Enabled	RW	1	Output enable for DIFF_0
5	Reserved				0	Reserved
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2	Reserved				0	Reserved
1	Reserved				0	Reserved
0	Reserved				0	Reserved

Table 8.26. Control Register 1. Byte 1

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	Reserved				0	Reserved
5	DIFF1_OE	Disabled	Enabled	RW	1	Output enable for DIFF_1
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2					0	
1	SS_EN_READ1			R	0	Spread Enable software readback 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5% The value of SS_EN_READ is latched on power-up.
0	SS_EN_READ0			R	0	

Table 8.27. Control Register 2. Byte 2

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SS_EN_SW_HW_CTRL	Read back Byte 1[1:0]	SS control by Byte 2 [6:5]	RW	0	Enable software control of spread
6	SS_EN_SW1			RW	0	Software control of spread 00 = –0.25%; 01 = OFF; 10 = OFF; 11 = –0.5%
5	SS_EN_SW0			RW	1	
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2	Reserved				0	Reserved
1	Reserved				0	Reserved
0	Reserved				1	Reserved

Table 8.28. Control Register 3. Byte 3

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				1	Reserved
6	SR_SEL_DIFF_0	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_2
5	Reserved				1	Reserved
4	Reserved				1	Reserved
3	Reserved				1	Reserved
2	Reserved				1	Reserved
1	Reserved				1	Reserved
0	Reserved				1	Reserved

Table 8.29. Control Register 4. Byte 4

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				1	Reserved
6	Reserved				1	Reserved
5	SR_SEL_DIFF_1	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_1
4	Reserved				1	Reserved
3	AMP			RW	1	DIFF Differential Outputs Amplitude Adjustment. 0110 : 600 mV 0111 : 650 mV 1000 : 700 mV 1001 : 750 mV 1010 : 800 mV 1011 : 850 mV
2	AMP			RW	0	
1	AMP			RW	0	
0	AMP			RW	0	

Table 8.30. Control Register 5. Byte 5

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Rev Code [7:4]			R	0	Revision Code
6				R	0	
5				R	0	
4				R	0	
3	Vendor ID[3:0]			R	1	Vendor Identification Code
2				R	0	
1				R	0	
0				R	0	

Table 8.31. Control Register 6. Byte 6

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Programming ID [7:0]			R	0	Programming ID (Internal Only)
6				R	0	
5				R	0	
4				R	0	
3				R	0	
2				R	0	
1				R	0	
0				R	0	

9. Pin Descriptions

9.1 Si52212 Pin Descriptions

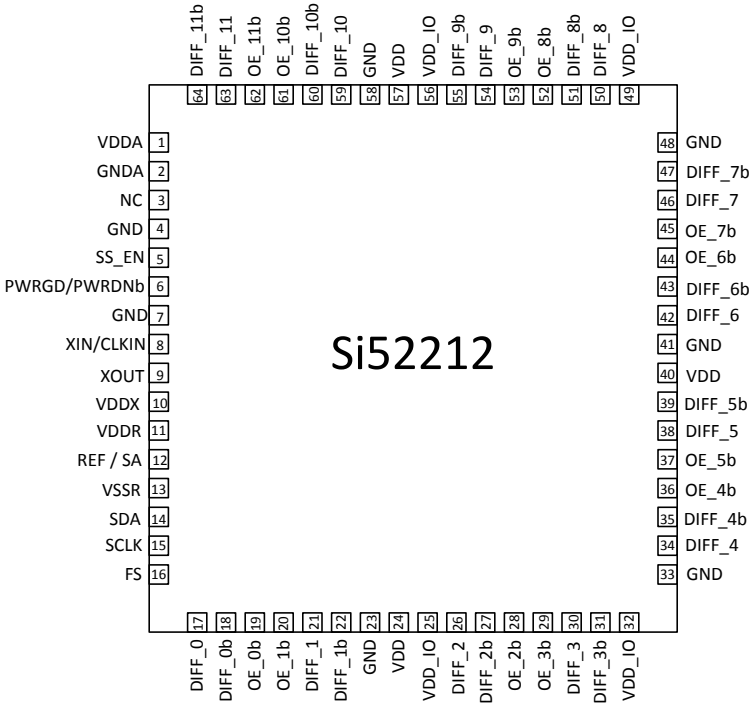


Figure 9.1. 64-Pin QFN

Table 9.1. Si52212 64-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDDA	PWR	Analog Power Supply.
2	GNDA	PWR	Analog Ground.
3	NC		No connect.
4	GND	GND	Ground.
5	SS_EN	I	Spread spectrum enable pin. 0 = –0.25% spread, mid= Off, 1= –0.5% spread (This pin has an internal 100 kΩ pull-up).
6	PWRGD/ PWRDNb	I, PU	Active low input pin asserts power down (PDb) and disables all outputs (This pin has an internal 100 kΩ pull-up). Refer also to settings of Byte 2, Bit2 and Bit3 for REF. Settings for Bit3 (REF_OE) will take precedence for REF.
7	GND	GND	Ground.
8	XIN/CLKIN	I	25.00 MHz crystal input or 25 MHz Clock Input.
9	XOUT	O	25.00 MHz crystal output. Float XOUT if using only CLKIN (Clock input).
10	VDDX	PWR	Power supply for crystal.
11	VDDR	PWR	Power supply for REF output.
12	REF /SA	O/I	REF = 25 MHz LVCMOS output. SA = Address select for I^2C. When part is powered up, SA will be latched to select the I^2C address. Refer to Table 8.1 SA State on First Application of PWRDNb on page 32. Refer also to 5.14 REF/SA Pin for termination. (This pin has an internal 60 kΩ pull-up.)

Pin #	Name	Type	Description
13	VSSR	GND	Ground.
14	SDA	I/O	I^2C compatible SDATA.
15	SCLK	I	I^2C compatible SCLOCK.
16	FS	I	Frequency select pin. 0 = 100 MHz, mid = 200 MHz, 1 = 133 MHz. (This pin has an internal 100 kΩ pull-down.)
17	DIFF_0	O, DIF	0.7 V, 100 MHz differential clock.
18	DIFF_0b	O, DIF	0.7 V, 100 MHz differential clock.
19	OE_0b	I, PD	Output enable for DIFF_0 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
20	OE_1b	I, PD	Output enable for DIFF_1 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
21	DIFF_1	O, DIF	0.7 V, 100 MHz differential clock.
22	DIFF_1b	O, DIF	0.7 V, 100 MHz differential clock.
23	GND	GND	Ground.
24	VDD	PWR	Power supply.
25	VDD_IO	PWR	Output power supply.
26	DIFF_2	O, DIF	0.7 V, 100 MHz differential clock.
27	DIFF_2b	O, DIF	0.7 V, 100 MHz differential clock.
28	OE_2b	I, PD	Output enable for DIFF_2 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.
29	OE_3b	I, PD	Output enable for DIFF_3 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.
30	DIFF_3	O, DIF	0.7 V, 100 MHz differential clock.
31	DIFF_3b	O, DIF	0.7 V, 100 MHz differential clock.
32	VDD_IO	PWR	Output power supply.
33	GND	GND	Ground.
34	DIFF_4	O, DIF	0.7 V, 100 MHz differential clock.
35	DIFF_4b	O, DIF	0.7 V, 100 MHz differential clock.
36	OE_4b	I, PD	Output enable for DIFF_4 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.
37	OE_5b	I, PD	Output enable for DIFF_5 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.
38	DIFF_5	O, DIF	0.7 V, 100 MHz differential clock.
39	DIFF_5b	O, DIF	0.7 V, 100 MHz differential clock.
40	VDD	PWR	Power supply.
41	GND	GND	Ground.
42	DIFF_6	O, DIF	0.7 V, 100 MHz differential clock.
43	DIFF_6b	O, DIF	0.7 V, 100 MHz differential clock.
44	OE_6b	I, PD	Output enable for DIFF_6 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.

Pin #	Name	Type	Description
45	OE_7b	I, PD	Output enable for DIFF_7 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.
46	DIFF_7	O, DIF	0.7 V, 100 MHz differential clock.
47	DIFF_7b	O, DIF	0.7 V, 100 MHz differential clock.
48	GND	GND	Ground.
49	VDD_IO	PWR	Output power supply.
50	DIFF_8	O, DIF	0.7 V, 100 MHz differential clock.
51	DIFF_8b	O, DIF	0.7 V, 100 MHz differential clock
52	OE_8b	I, PD	Output enable for DIFF_8 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.
53	OE_9b	I, PD	Output enable for DIFF_9 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs.
54	DIFF_9	O, DIF	0.7 V, 100 MHz differential clock.
55	DIFF_9b	O, DIF	0.7 V, 100 MHz differential clock.
56	VDD_IO	PWR	Output power supply.
57	VDD	PWR	Power supply.
58	GND	GND	Ground.
59	DIFF_10	O, DIF	0.7 V, 100 MHz differential clock.
60	DIFF_10b	O, DIF	0.7 V, 100 MHz differential clock.
61	OE_10b	I, PD	Output enable for DIFF_10 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
62	OE_11b	I, PD	Output enable for DIFF_11 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
63	DIFF_11	O, DIF	0.7 V, 100 MHz differential clock.
64	DIFF_11b	O, DIF	0.7 V, 100 MHz differential clock
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

9.2 Si52208 Pin Descriptions

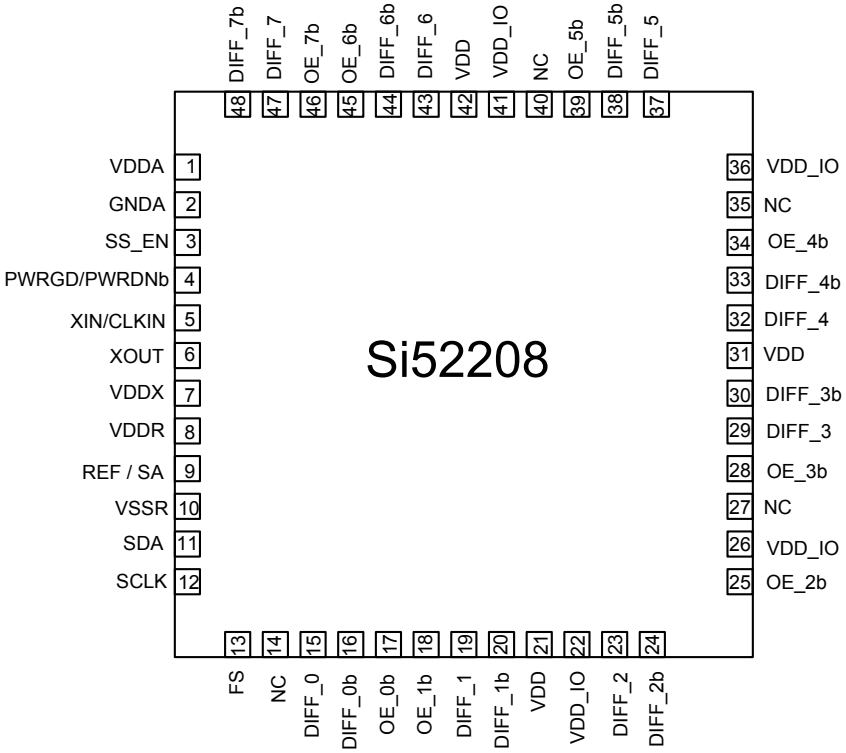


Figure 9.2. 48-pin QFN

Pin	Name	Type	Description
1	VDDA	PWR	Analog Power Supply.
2	GNDA	PWR	Analog Ground.
3	SS_EN	I	Spread spectrum enable pin. 0 = –0.25% spread, mid= Off, 1 = –0.5% spread (This pin has an internal 100 kΩ pull-up).
4	PWRGD/PWRDNb	I, PU	Active low input pin asserts power down (PDb) and disables all outputs. (This pin has an internal 100 kΩ pull-up). Refer also to settings of Byte 2, Bit2 and Bit3 for REF. Settings for Bit3 (REF_OE) will take precedence for REF.
5	XIN/CLKIN	I	25.00 MHz crystal input or 25 MHz Clock Input.
6	XOUT	O	25.00 MHz crystal output. Float XOUT if using only CLKIN (Clock input).
7	VDDX	PWR	Power supply for crystal.
8	VDDR	PWR	Power supply for REF output.
9	REF /SA	O/I	REF = 25 MHz LVCMOS output. SA = Address select for I^2C. When part is powered up, SA will be latched to select the I^2C address. Refer to Table 8.1 SA State on First Application of PWRDNb on page 32. Refer also to 5.14 REF/SA Pin for termination. (This pin has an internal 60 kΩ pull-up.)
10	VSSR	GND	Power supply for crystal.
11	SDA	I/O	I^2C compatible SDATA.
12	SCLK	I	I^2C compatible SCLOCK.

Pin	Name	Type	Description
13	FS	I	Frequency select pin. 0 = 100 MHz, mid = 200 MHz, 1 = 133 MHz (This pin has an internal 100 kΩ pull-down.)
14	NC	NC	No connect.
15	DIFF_0	O, DIF	0.7 V, 100 MHz differential clock.
16	DIFF_0b	O, DIF	0.7 V, 100 MHz differential clock.
17	OE_0b	I, PD	Output enable for DIFF_0 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
18	OE_1b	I, PD	Output enable for DIFF_1 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
19	DIFF_1	O, DIF	0.7 V, 100 MHz differential clock.
20	DIFF_1b	O, DIF	0.7 V, 100 MHz differential clock
21	VDD	PWR	Power supply.
22	VDD_IO	PWR	Output power supply.
23	DIFF_2	O, DIF	0.7 V, 100 MHz differential clock.
24	DIFF_2b	O, DIF	0.7 V, 100 MHz differential clock.
25	OE_2b	I, PD	Output enable for DIFF_2 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
26	VDD_IO	PWR	Output power supply.
27	NC	NC	No connect.
28	OE_3b	I, PD	Output enable for DIFF_3 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
29	DIFF_3	O, DIF	0.7 V, 100 MHz differential clock.
30	DIFF_3b	O, DIF	0.7 V, 100 MHz differential clock.
31	VDD	PWR	Power supply.
32	DIFF_4	O, DIF	0.7 V, 100 MHz differential clock.
33	DIFF_4b	O, DIF	0.7 V, 100 MHz differential clock.
34	OE_4b	I, PD	Output enable for DIFF_4 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
35	NC	NC	No connect.
36	VDD_IO	PWR	Output power supply.
37	DIFF_5	O, DIF	0.7 V, 100 MHz differential clock.
38	DIFF_5b	O, DIF	0.7 V, 100 MHz differential clock.
39	OE_5b	I, PD	Output enable for DIFF_5 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
40	NC	NC	No connect.
41	VDD_IO	PWR	Output power supply.
42	VDD	PWR	Power supply.
43	DIFF_6	O, DIF	0.7 V, 100 MHz differential clock.
44	DIFF_6b	O, DIF	0.7 V, 100 MHz differential clock.

Pin	Name	Type	Description
45	OE_6b	I, PD	Output enable for DIFF_6 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
46	OE_7b	I, PD	Output enable for DIFF_7 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs.
47	DIFF_7	O, DIF	0.7 V, 100 MHz differential clock.
48	DIFF_7b	O, DIF	0.7 V, 100 MHz differential clock.
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

9.3 Si52204 Pin Descriptions

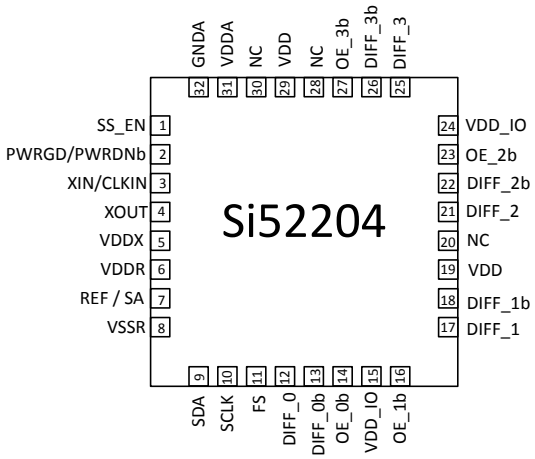


Figure 9.3. 32-pin QFN

Table 9.2. Si52204 32-pin QFN Descriptions

Pin #	Name	Type	Description
1	SS_EN	I	Spread spectrum enable pin. 0 = –0.25% spread; mid = Off; 1 = –0.5% spread. (This pin has an internal 100 kΩ pull-up.)
2	PWRGD/ PWRDNb	I, PU	Active low input pin asserts power down (PDb) and disables all outputs. (This pin has an internal 100 kΩ pull-up.) Refer also to settings of Byte 2, Bit2 and Bit3 for REF. Settings for Bit3 (REF_OE) will take precedence for REF.
3	XIN/CLKIN	I	25.00 MHz crystal input or 25 MHz Clock Input.
4	XOUT	O	25.00 MHz crystal output. Float XOUT if using only CLKIN (Clock input).
5	VDDX	PWR	Power supply for crystal
6	VDDR	PWR	Power supply for REF output
7	REF /SA	O/I	REF = 25 MHz LVCMOS output. SA = Address select for I2C. When part is powered up, SA will be latched to select the I^2C address. Refer to Table 8.1 SA State on First Application of PWRDNb on page 32. Refer also to 5.14 REF/SA Pin for termination. (This pin has an internal 60 kΩ pull-up.)
8	VSSR	GND	Ground
9	SDA	I/O	I^2C compatible SDATA
10	SCLK	I	I^2C compatible SCLOCK
11	FS	I	Frequency select pin. 0 = 100 MHz; mid = 200 MHz; 1 = 133 MHz. (This pin has an internal 100 kΩ pull-down.)
12	DIFF_0	O, DIF	0.7 V, 100 MHz differential clock
13	DIFF_0b	O, DIF	0.7 V, 100 MHz differential clock
14	OE_0b	I, PD	Output enable for DIFF_0 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs
15	VDD_IO	PWR	Output power supply
16	OE_1b	I, PD	Output enable for DIFF_1 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs
17	DIFF_1	O, DIF	0.7 V, 100 MHz differential clock

Pin #	Name	Type	Description
18	DIFF_1b	O, DIF	0.7 V, 100 MHz differential clock
19	VDD	PWR	Power supply
20	NC	NC	No connect
21	DIFF_2	O, DIF	0.7 V, 100 MHz differential clock
22	DIFF_2b	O, DIF	0.7 V, 100 MHz differential clock
23	OE_2b	I, PD	Output enable for DIFF_2 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs
24	VDD_IO	PWR	Output power supply
25	DIFF_3	O, DIF	0.7 V, 100 MHz differential clock
26	DIFF_3b	O, DIF	0.7 V, 100 MHz differential clock
27	OE_3b	I, PD	Output enable for DIFF_3 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs
28	NC	NC	No connect
29	VDD	PWR	Power supply
30	NC	NC	No connect
31	VDDA	PWR	Analog Power Supply
32	GNDA	PWR	Analog Ground
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

9.4 Si52202 Pin Descriptions

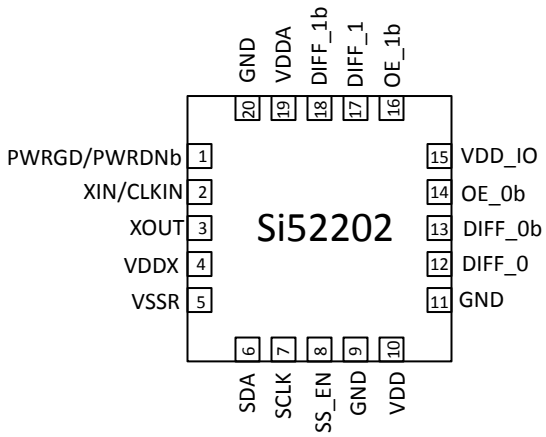


Figure 9.4. 20-pin QFN

Table 9.3. Si52202 20-pin QFN Descriptions[1]

Pin #	Name	Type	Description
1	PWRGD/ PWRDNb	I, PU	Active low input pin asserts power down (PDb) and disables all outputs (This pin has an internal pull-up).
2	XIN/CLKIN	I	25.00 MHz crystal input or 25 MHz Clock Input.
3	XOUT	O	25.00 MHz crystal output. Float XOUT if using only CLKIN (Clock input).
4	VDDX	PWR	Power supply for crystal
5	VSSR	GND	Ground
6	SDA	I/O	I^2C compatible SDATA
7	SCLK	I	I^2C compatible SCLOCK
8	SS_EN	I	Spread spectrum enable pin. 0 = –0.25% spread; mid = Off; 1 = –0.5% spread. (This pin has an internal 100 kΩ pull-up.)
9	GND	GND	Ground
10	VDD	PWR	Power supply
11	GND	GND	Ground
12	DIFF_0	O, DIF	0.7 V, 100 MHz differential clock
13	DIFF_0b	O, DIF	0.7 V, 100 MHz differential clock
14	OE_0b	I, PD	Output enable for DIFF_0 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs
15	VDD_IO	PWR	Output power supply
16	OE_1b	I, PD	Output enable for DIFF_1 pair. (This pin has an internal 100 kΩ pull-down.) 0 = Enable outputs; 1 = Disable outputs
17	DIFF_1	O, DIF	0.7 V, 100 MHz differential clock
18	DIFF_1b	O, DIF	0.7 V, 100 MHz differential clock
19	VDDA	PWR	Analog Power Supply

Pin #	Name	Type	Description
20	GND	GND	Ground
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

Note:

1. Contact factory for 133/200M output frequencies.

10. Packaging

10.1 Si52212 Package

The figure below illustrates the package details for the Si52212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

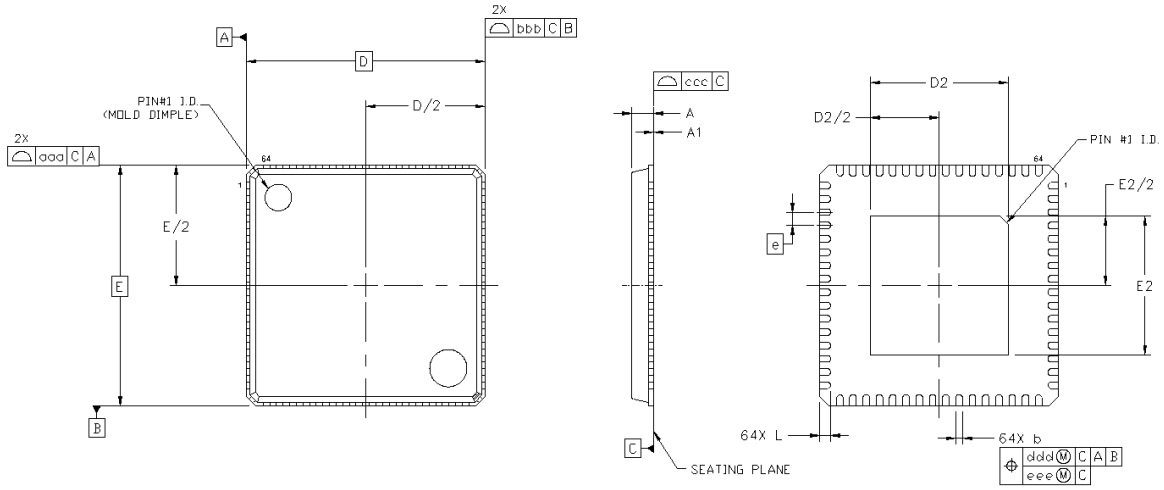


Figure 10.1. 64L 9 x 9 mm QFN Package Diagram

Table 10.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020D specification for Small Body Components.

10.2 Si52212 Land Pattern

The following figure illustrates the land pattern details for the Si52212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

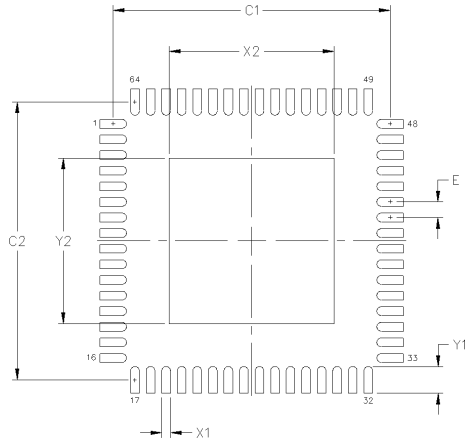


Figure 10.2. 64L 9 x 9 mm QFN Land Pattern

Table 10.2. PCB Land Pattern Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	5.30
Y2	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.25 mm square openings on a 1.80 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 Si52208 Package

The figure below illustrates the package details for the Si52208 in a 48-Lead 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

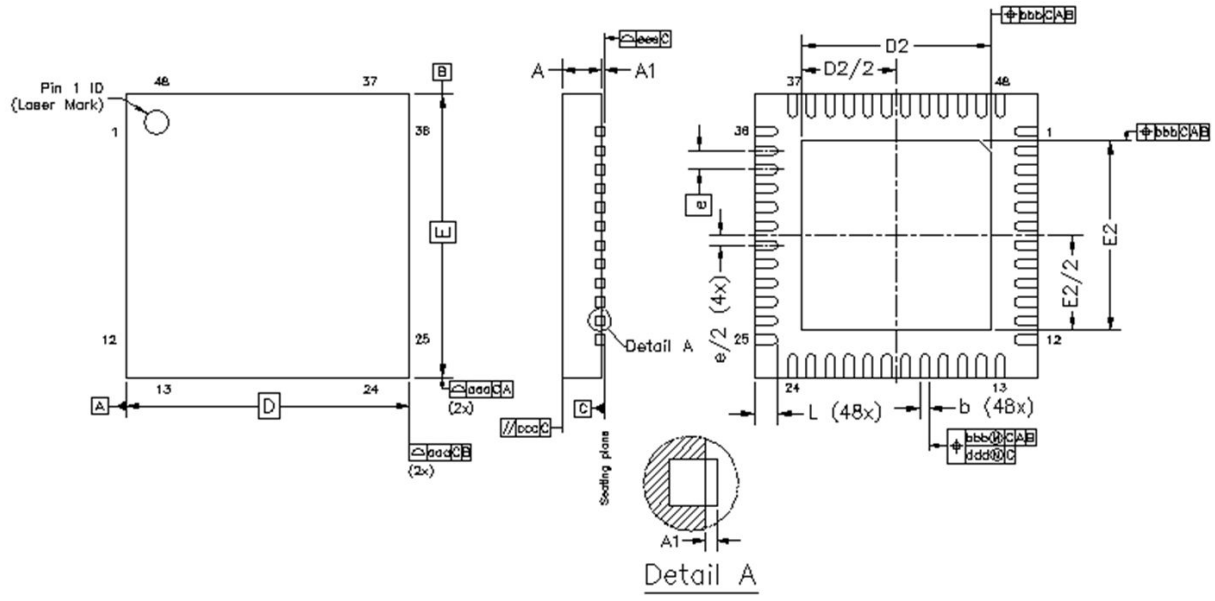


Figure 10.3. 48L 6 x 6 mm QFN Package Diagram

Table 10.3. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		6.00 BSC	
D2	3.5	3.6	3.7
e		0.40 BSC	
E		6.00 BSC	
E2	3.5	3.6	3.7
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components.

10.4 Si52208 Land Pattern

The figure below illustrates the land pattern details for the Si52208 in a 48-Lead, 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

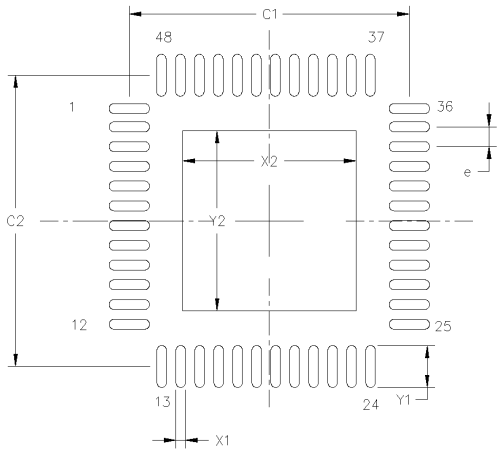


Figure 10.4. 48L 6 x 6 mm QFN Land Pattern

Table 10.4. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
X1	0.20
X2	3.60
Y1	0.85
Y2	3.60
e	0.40 BSC

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 3x3 array of 0.90 mm square openings on 1.15mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.5 Si52204 Package

The figure below illustrates the package details for the Si52204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

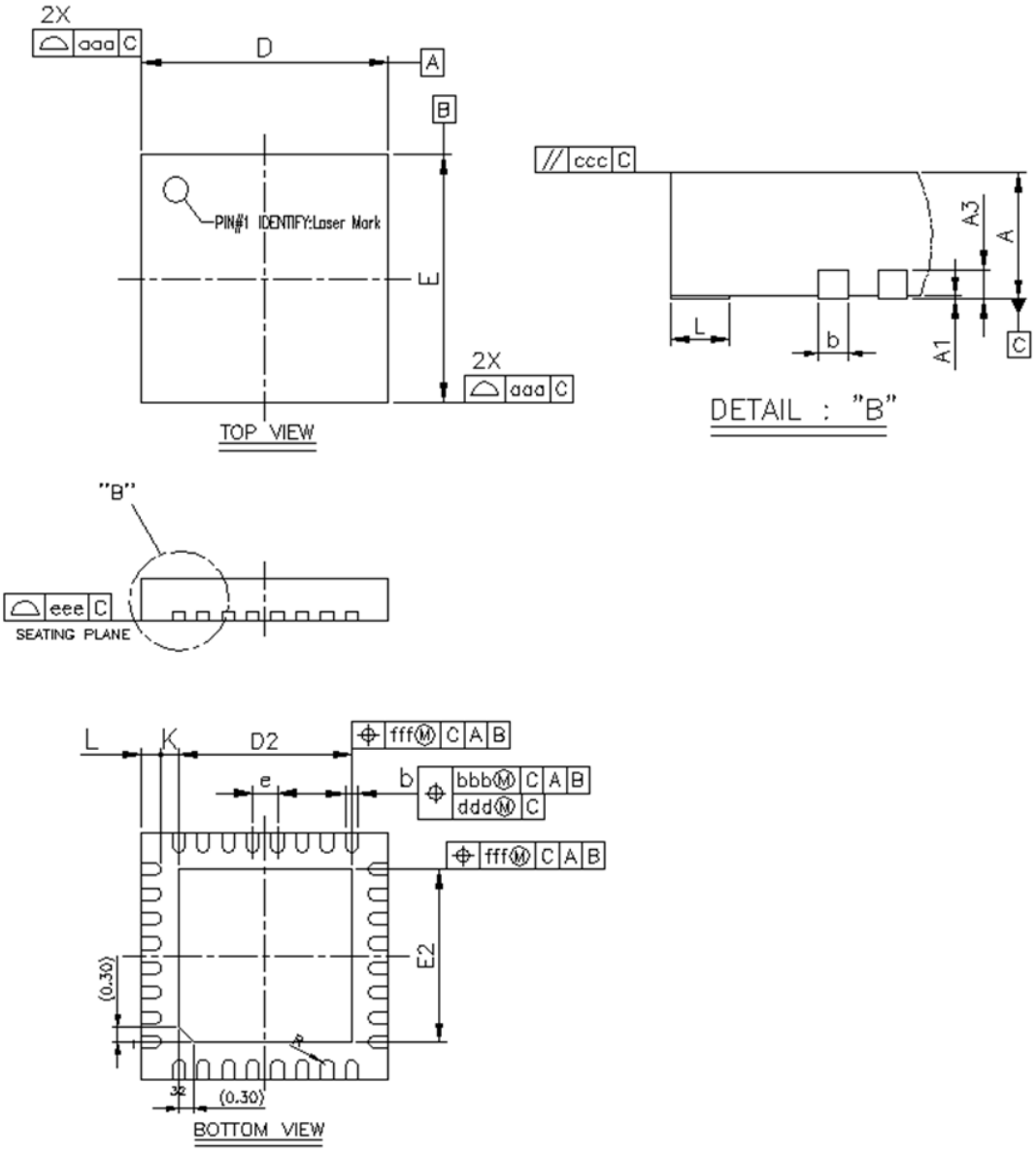


Figure 10.5. 32L 5 x 5 mm QFN Package Diagram

Table 10.5. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
K	0.20	—	—
L	0.30	0.40	0.50
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components.

10.6 Si52204 Land Pattern

The figure below illustrates the land pattern details for the Si52204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

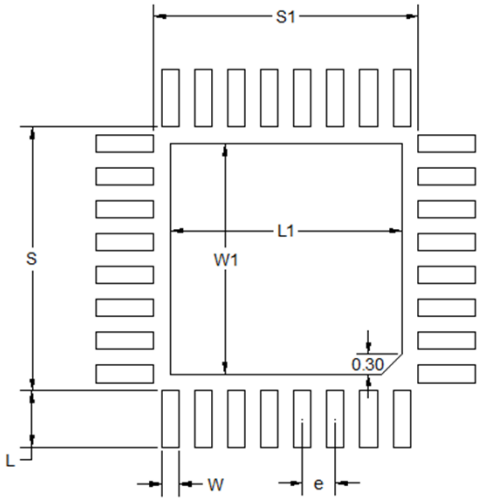


Figure 10.6. 32L 5 x 5 mm QFN Land Pattern

Table 10.6. PCB Land Pattern Dimensions

Dimension	mm
S1	4.01
S	4.01
L1	3.50
W1	3.50
e	0.50
W	0.26
L	0.86

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3x3 array of 0.85 mm square openings on 1.00 mm pitch can be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.7 Si52202 Package

The figure below illustrates the package details for the Si52202 in a 20-Lead, 3 x 3 mm QFN package. The table lists the values for the dimensions shown in the illustration.

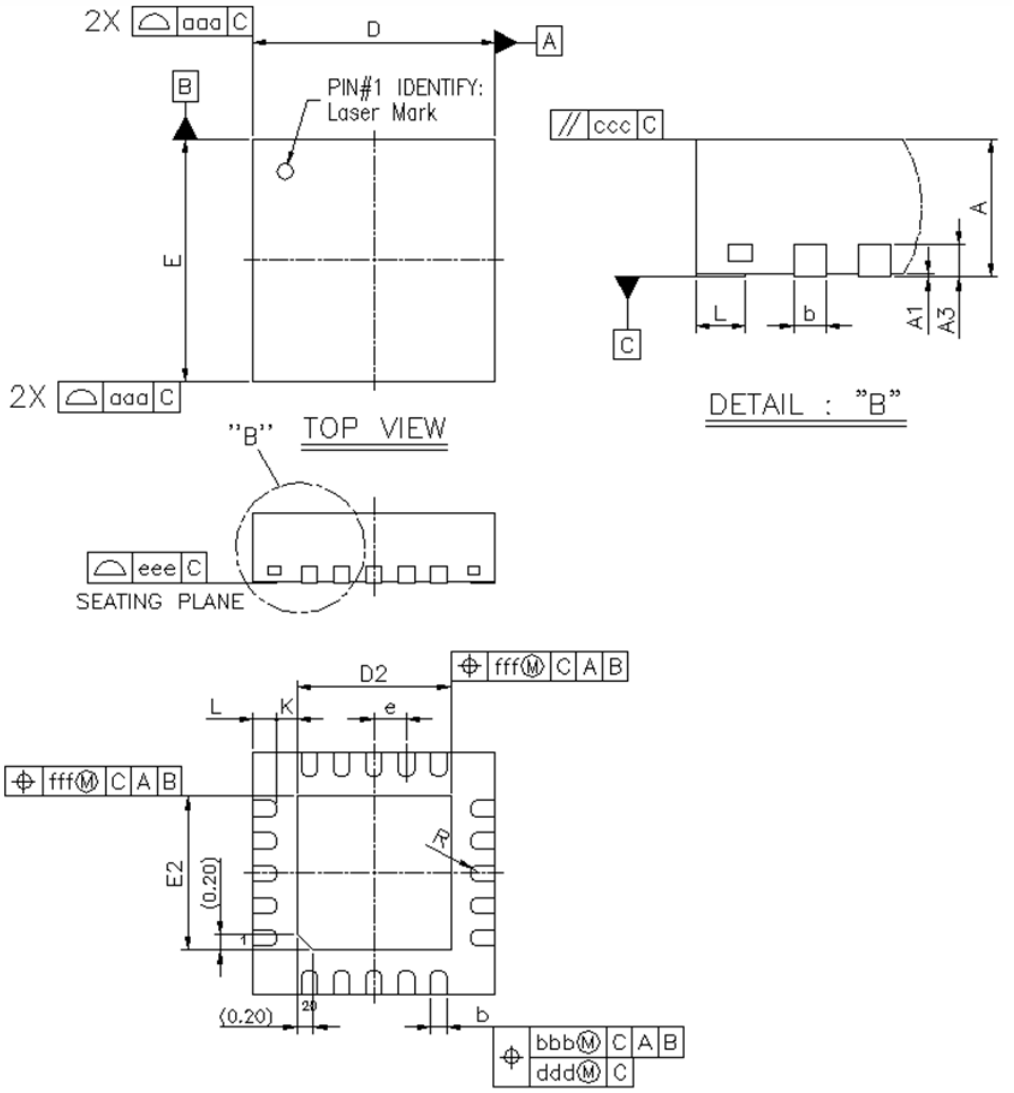


Figure 10.7. 20L 3 x 3 mm QFN Package Diagram

Table 10.7. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	—	0.65	—
A3		0.20 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
D2	1.8	1.9	2.0
E		3.00 BSC	
E2	1.8	1.9	2.0
e		0.40 BSC	
K	0.20	—	—
L	0.20	0.30	0.40
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.8 Si52202 Land Pattern

The figure below illustrates the land pattern details for the Si52202 in a 20-Lead, 3 x 3 mm QFN package. The table lists the values for the dimensions shown in the illustration.

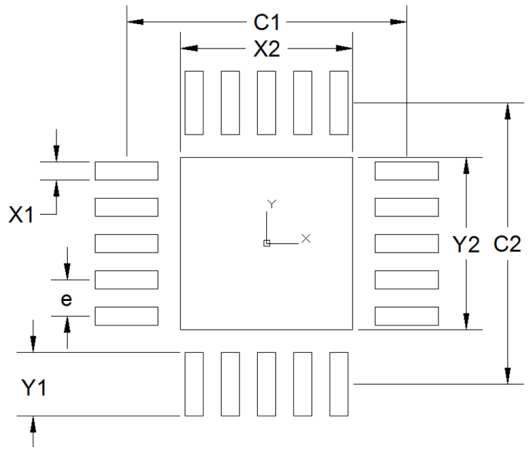


Figure 10.8. 20L 3 x 3 mm QFN Land Pattern

Table 10.8. PCB Land Pattern Dimensions

Dimension	mm
C1	3.10
C2	3.10
X1	0.20
X2	1.90
Y1	0.70
Y2	1.90
e	0.40 BSC

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 3x3 array of 0.90 mm square openings on 1.15 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.9 Si52212 Top Markings

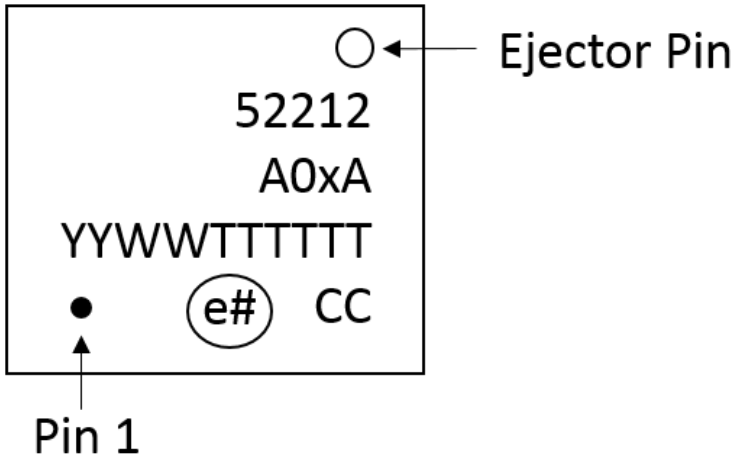


Figure 10.9. Si52212 Top Marking

Table 10.9. Si52212 Top Marking Explanation

Line	Characters	Description
1	52212	Device part number
2	A0xA	Device part number x = 1 = Internal 100 Ω impedance matching x = 2 = Internal 85 Ω impedance matching
3	YYWWTTTTTT	YY = Assembly year WW = Assembly work week TTTTTT = Manufacturing trace code

4	e# CC	e# = Lead finish symbol. # is a number
		CC = Country of origin (ISO abbreviation)

10.10 Si52208 Top Markings

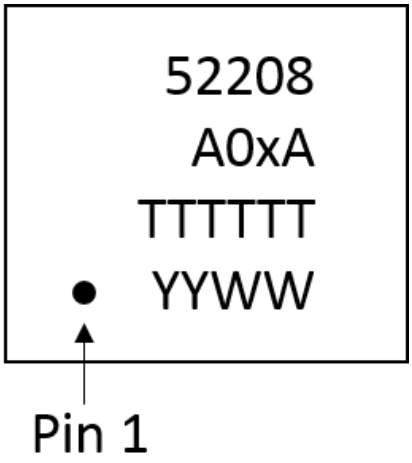


Figure 10.10. Si52208 Top Marking

Table 10.10. Si52208 Top Marking Explanation

Line	Characters	Description
1	52208	Device part number
2	A0xA	Device part number x = 1 = Internal 100 Ω impedance matching x = 2 = Internal 85 Ω impedance matching
3	TTTTTT	TTTTTT = Manufacturing trace code
4	YYWW	YY = Assembly year WW = Assembly work week

10.11 Si52204 Top Markings

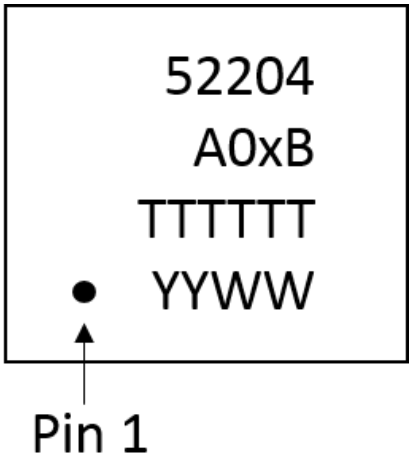


Figure 10.11. Si52204 Top Marking

Table 10.11. Si52204 Top Marking Explanation

Line	Characters	Description
1	52204	Device part number
2	A0xB	Device part number x = 1 = Internal 100 Ω impedance matching x = 2 = Internal 85 Ω impedance matching
3	TTTTTT	TTTTTT = Manufacturing trace code
4	YYWW	YY = Assembly year WW = Assembly work week

10.12 Si52202 Top Markings

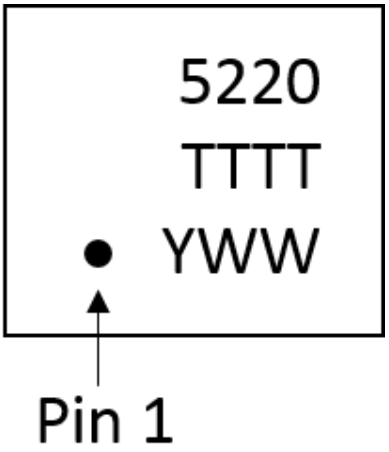


Figure 10.12. Si52202 Top Marking

Table 10.12. Si52202 Top Marking Explanation

Line	Characters	Description
1	5220	Device part number
2	TTTT	TTTT = Manufacturing trace code
3	YWW	Y = Assembly year WW = Assembly work week

11. Revision History

Revision 1.0

March, 2019

- Updated 2. Ordering Guide with new 4-output and 2-output part numbers.
- Updated 4. Electrical Specifications.
  - Updated Table 4.1 DC Electrical Specifications (VDD = 1.5 V ±5%) on page 8.
  - Updated Table 4.2 DC Electrical Specifications (VDD = 1.8 V ±5%) on page 11.
  - Updated Table 4.3 AC Electrical Specifications on page 14.
  - Updated Table 4.4 PCIe and Intel QPI Jitter Specifications on page 16.
- Added 5.4 Power Supply Filtering Recommendations.
- Updated 5.5 PWRGD/PWRDNb (Power Down) Pin.
- Updated 5.6 PWRDNb (Power Down) Assertion.
- Updated 5.7 PWRDNb (Power Down) Deassertion.
- Updated 5.8 OEb Pin.
- Updated 5.11 FS Pin.
- Added 5.12 SS_EN Pin.
- Added 5.13 Recommendations for Driving Tri-State Pins.
- Added 5.14 REF/SA Pin.
- Updated 8.3 Block Read.
- Updated 8.4 Block Write.
- Updated 8.6 Byte Read.
- Updated 8.7 Byte Write.
- Updated 8.8 Data Protocol.
- Updated 8.9 Register Tables.
- Updated 9. Pin Descriptions.

Revision 0.7

September, 2017

- Initial Release.

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