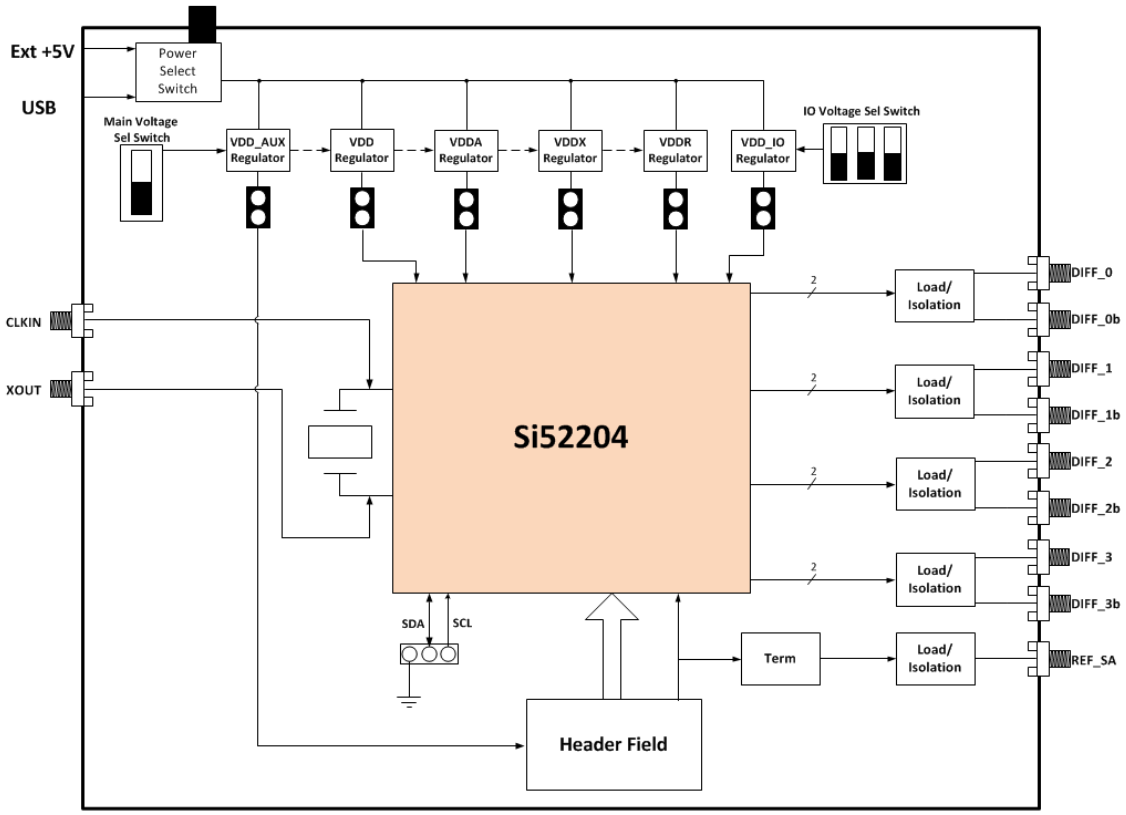
UG277: Si52204-EVB User's Guide

4-Output PCI-Express Gen1/2/3/4 and SRIS Clock Generator Evaluation Board

This document describes operation of the Silicon Laboratories Si52204-EVB evaluation board designed to evaluate the Si52204, 4-output PCI-Express Gen1/2/3/4 and SRIS Clock Generator. Selector switches make it easy to select the voltage for both core and IO supplies. Jumpers allow for easy static configuration of the control inputs as well as provide a port for external test equipment access. Similarly, each regulated supply can be bypassed and driven externally for precise voltage control or to measure PSRR performance. I2C ports allow for communication to the DUT by external I2C bus analyzers/exercisers. Optimal XTAL placement and layout provide excellent phase noise performance. Convenient probe pads and isolation resistors permit on-board single-ended or differential measurements. Finally, the PCB layout optimizes signal integrity and skew which rounds out the capabilities of this EVB.

KEY FEATURES

- Evaluation of Silicon Labs Si52204
- DC-coupled differential output clocks
- DC-coupled single-ended reference clock
- External power or USB powered
- Switchable voltage settings
- Easy manual configuration via jumpers
- I2C port access
- Easy current measurement



1. Functional Description

The Si52204-EVB is an evaluation board designed to support the Si52204 device. The Si52204-EVB is designed to operate in one of two general operational modes:

1. **Stand-alone mode:** The stand-alone mode is for manual evaluation of the device. Control of device pins such as OE_xb, FS, PWRGD, REF_SA, and SS_EN is done via on-board jumpers. The jumper header (J14) also allows the user to test the enable/disable time by providing an access point for external test equipment to easily drive the enable or PWRGD pins. The DUT supply voltages (e.g. VDD, VDDR, VDDX, VDDA, and VDDIO) can be set via on-board switches as shown in Section 2. Each supply can be sourced either by an on-board regulator for nominal values or via an external supply to test the device over a range of voltages (e.g. min/max supply testing).
2. **I2C mode:** The Evaluation Board also allows the user to setup the device via I2C commands using an external I2C driver/analyzer and connecting to the SCL/SDA header (JP7).

2. Power Supply Switch Settings

The device supplies use a linear voltage regulator to drop the externally supplied +5 V (sourced either via USB or an external power supply using switch SW3) voltage to one of the supported nominal VDD voltages (+1.8 V or +1.5 V for VDD, VDDA, VDDR, and VDDX using switch SW1 and +1.8 V, +1.5 V, +1.2 V, or +1.0 V for VDDIO using switch SW2).

2.1 +5 V Selection

The +5 V main supply is sourced by either an external power supply or by USB-B connected to a computer, via switch SW3 located as shown in the figure below. Position the slide in the up position to select the USB port (J13) and in the down position to select the external supply (J11, J12).

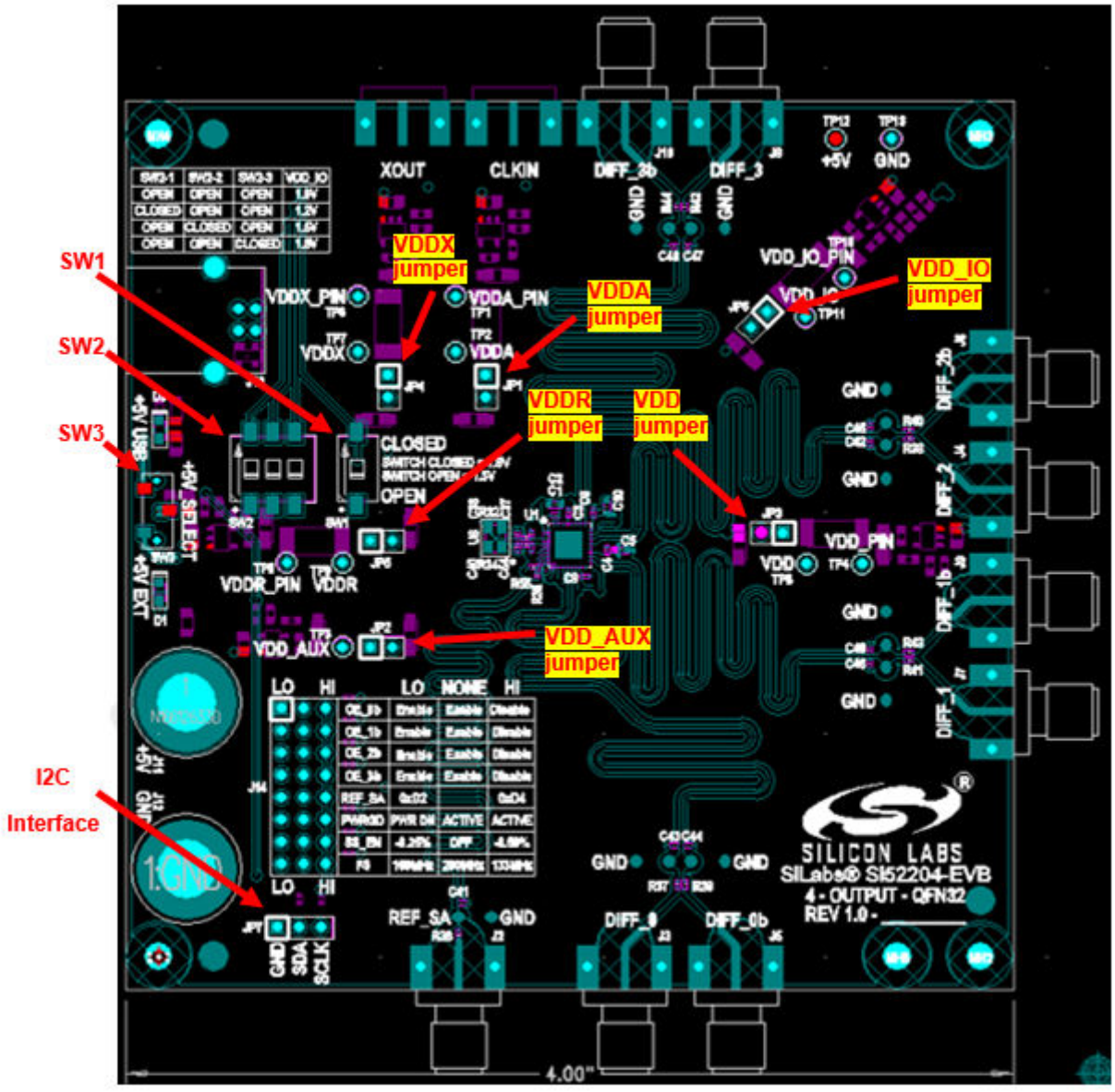


Figure 2.1. Location of EVB Power and Voltage Switches and Jumpers

2.2 Voltage Selection for Non-Output Supplies (VDD, VDDR, VDDX, VDDA, and VDD_AUX)

The nominal voltage setting for all but VDD_IO is controlled by switch SW1 as shown in Figure 2.1 Location of EVB Power and Voltage Switches and Jumpers on page 3. Positioning the switch in the open position selects 1.5 V for all these supplies and positioning the switch in the closed position selects 1.8 V. Jumpers JP1-JP5 should be installed if the on-board regulator is desired. Alternatively, an external voltage source can be connected to a supply by removing the corresponding jumper and connecting the (+) voltage of the supply to pin 2 of the jumper and (-) voltage to GND (TP13). Note that pin 1 of the jumpers is identified by the highlighted square.

2.3 Voltage Selection for Output Supply (VDD_IO)

The nominal voltage setting for VDD_IO is controlled by switch SW2 as shown in Figure 2.1 Location of EVB Power and Voltage Switches and Jumpers on page 3. The table below shows the switch settings for nominal voltages: +1.8 V, +1.5 V, +1.2 V, and +1.0 V. Note that only one switch should be in the "closed" position at any given time. Multiple closed switches at the same time could lead to part damage. Jumper JP6 should be installed if the on-board regulator is desired.

Alternatively, an external voltage source can be connected to this supply by removing this jumper and connecting the (+) voltage of the supply to pin 2 of the jumper and (-) voltage to GND (TP13). Note that this is an excellent way to test the PSRR performance of the part as the dc supply can be modulated with a sinusoidal (noise) waveform and inserted on JP6, pin 2.

Table 2.1. Switch 2 Settings for Output Voltage Supply

SW2-1	SW2-2	SW2-3	VDD_IO
OPEN	OPEN	OPEN	1.0V
CLOSED	OPEN	OPEN	1.2V
OPEN	CLOSED	OPEN	1.5V
OPEN	OPEN	CLOSED	1.8V

2.4 Measuring Supply Currents (IDD, IDD_A, IDD_X, IDD_R, and IDD_{IO})

Measuring the current on any supply rail can be performed by simply measuring the voltage between test points VDDx and VDDx_PIN since between these two test points is a precision (±100 ppm) 1 ohm resistor. Therefore, whatever voltage is measured maps to the equivalent current measurement (e.g., 30 mV →30 mA).

3. Control Signal Jumper Settings

Header J14 is an 8x3, 100 mil header stake that provides access to the eight control input pins allowing these pins to be configured to the low, mid, or high input state. The table below defines how to configure each input

Table 3.1. Control Input Jumper Configuration Settings

Control Input Pin	LO	NONE	HI
OE_0b	Enable	Enable	Disable
OE_1b	Enable	Enable	Disable
OE_2b	Enable	Enable	Disable
OE_3b	Enable	Enable	Disable
REF_SA	0xD2		0xD4
PWRGD	PWRDN	ACTIVE	ACTIVE
SS_EN	-0.25%	OFF	-0.50%
FS	100MHz	200MHz	133MHz

Enable/Disable times can be measured by connecting an external pulse generator to the "B" pin of the header and GND to the "A" pin and sending this signal to trigger a scope. By measuring the time differential between the rising (falling) edge of the trigger and last (first) output clock edge of the corresponding output, the user can determine the disable (enable) time for that output.

4. Output Clock Terminations

4.1 Differential Outputs (DIFF_0:3)

The figure below shows the output termination circuit for each of the four differential clock outputs: Diff_0:3. To simplify on-board probing of the clock, exposed copper pads have been included (PCB11:18 for signals, PCB2:9 for GND) and are spaced to accommodate a differential probe (e.g., Ag1132A). The stock output clock termination is optimized for phase noise measurements. Note that most phase noise analyzers have a single-ended input, so a balun should be added to convert the differential output to single-ended.

To analyze signal integrity instead of phase noise, change resistors R37:R44 from 0 to 953 ohms (all 402 size.) Also, add 2pF capacitors to C43:C48. With this change, remember that if observing the outputs via the SMA connectors to a 50-ohm input scope, the scale is 1:20.

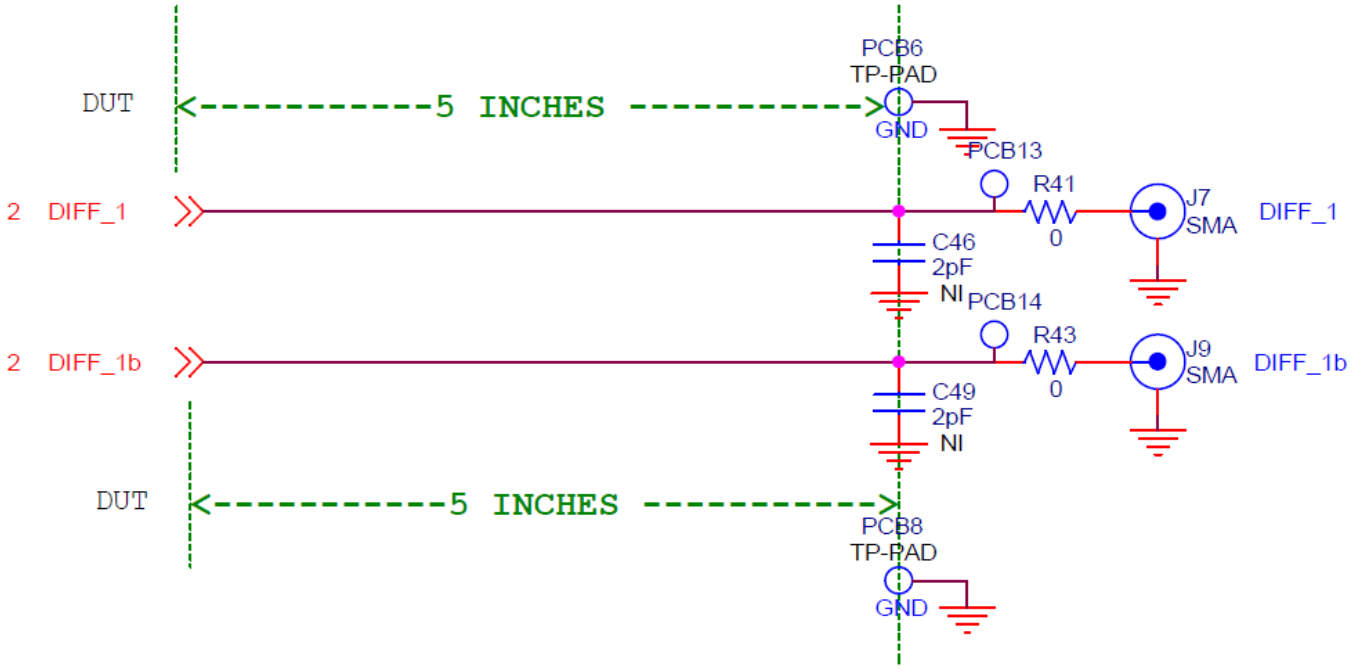


Figure 4.1. Differential Output Clock Termination

4.2 Reference Output (REF_SA)

The figure below shows the output termination circuit for the reference (25 MHz) output: REF_SA. To simplify on-board probing of the clock, exposed copper pads have been included (PCB10 for REF_SA and PCB1 for GND) and are spaced to accommodate a differential probe (e.g., Ag1132A). A series termination resistor (R35) is used to make the total output impedance of the driver match the characteristic impedance of the PCB trace (50 ohms). The reference output is currently optimized for phase noise measurements. For signal integrity measurements, replace the 0 ohm resistor on R36 with a 953 ohm. This will buffer the stub length from the pad to the SMA connector so the user can observe the response after 5 inches of PCB length with a 4.7pF load capacitor. Also, note that this new configuration will require a 20:1 probe ratio using coax cables connected to the 50 ohm input of the scope.

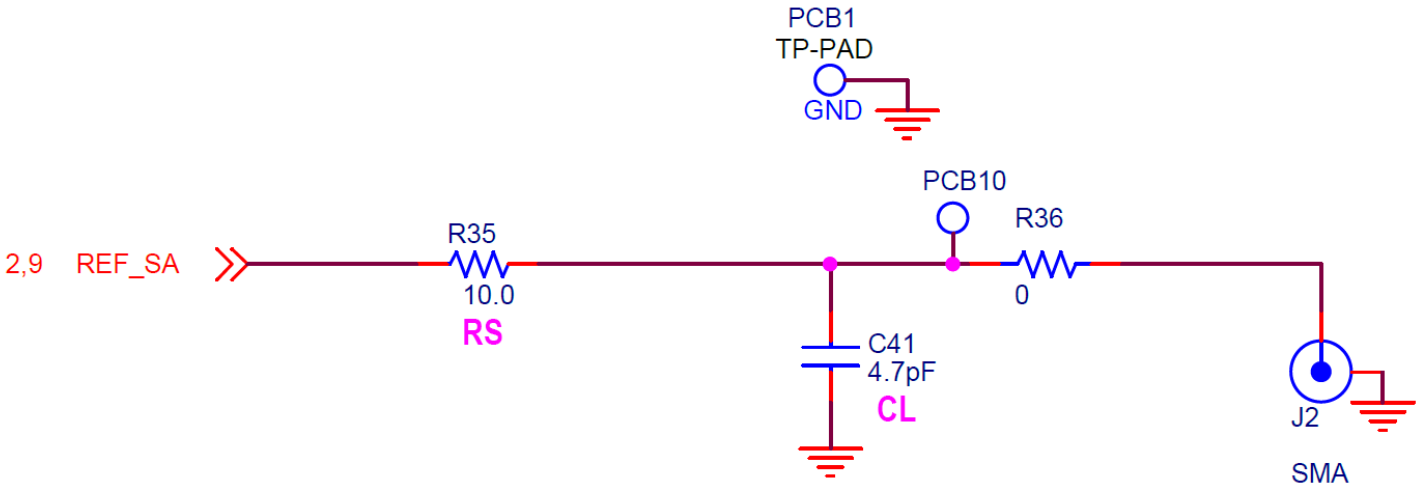


Figure 4.2. Reference Output Clock Termination

5. XTAL and External Input Clock

The on-board crystal (U8) layout will accommodate multiple size packages: 2.5x2.0 mm, 3.2x2.5 mm, and 3.2x5.0 mm so the user can experiment with different sized crystals if he chooses. The crystal used on the CEVB (25 MHz) is from Epson and is 3.2x2.5 mm. Optionally, the user can drive the input clock externally via SMA connector J1 (CLKIN). To switch the DUT input from the crystal to a single-ended external clock, populate R64 (0 ohms 0402 size) and de-populate R32 (0 ohms). If a 50 ohm termination is required, also populate R33 (49.9 ohms) and C39 (0.1µF) (all 0402 size). Refer to the datasheet for clock input specifications.

6. LEDs

The Si52204-EVB has 2 status LEDs as shown in table below. The board silkscreen identifies each LED.

Table 6.1. Status LEDs

LED name	Color	Location	Description
+5V_EXT	Green	D1	External +5 V source is present (independent of +5V_SELECT (SW3) switch setting)
+5V_USB	Blue	D3	USB port is present (independent of +5V_SELECT (SW3) switch setting)

7. I2C Interface

Header JP7 provides header stakes for GND, SCLK, and SDATA (SDA) (See figure below). SCLK and SDA have on-board 1k ohm pull-ups to VDD_AUX (supply that tracks to VDD). The device address is controlled by the jumper setting (at power up) of REF_SA on J14 as shown in Table 3.1 Control Input Jumper Configuration Settings on page 5.

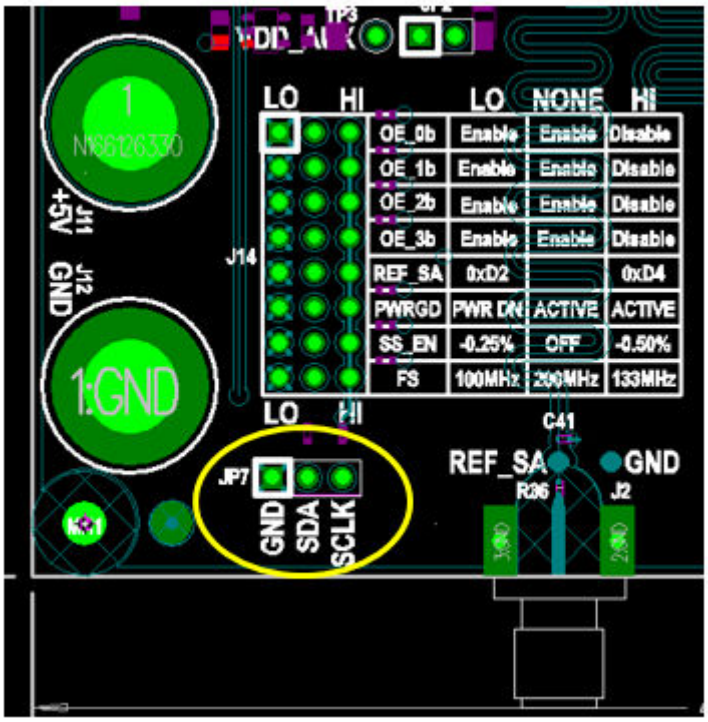


Figure 7.1. I2C Access Header Location

8. Quick Start—Board Configuration Check List

1. Start with EVB board powered down/off.
2. Set the voltage supply DIP switches (described in 2.2 Voltage Selection for Non-Output Supplies (VDD, VDDR, VDDX, VDDA, and VDD_AUX) and 2.3 Voltage Selection for Output Supply (VDD_IO)) according to the following:
   a. Switch SW1 controls the voltage setting (either 1.5 V or 1.8 V) for the following supplies:
      i. VDD
      ii. VDDA
      iii. VDDR
      iv. VDDX
      v. VDD_AUX
   b. Switch SW2 controls the voltage setting (either 1.0 V, 1.2 V, 1.5 V, or 1.8 V) for VDD_IO (voltage supply for output DIFF_0:3).
   c. Make sure that jumpers JP1:6 are installed.
3. Choose clock input source—the board defaults to the 25 MHz XTAL (U8). Refer to 5. XTAL and External Input Clock for instructions on how to switch the input clock source to an external clock.
4. Determine the type of measurement you want to take.
   - For phase noise measurements, no changes are required. Note that most phase noise analyzers have a single ended input, so a balun should be added to convert the differential output to single ended.
   - For signal integrity measurements, change resistors R37:R44 from 0 to 953 ohms (all 402 size.) Also, add 2pF capacitors to C43:C48. With this change, remember that if observing the outputs via the SMA connectors to a 50-ohm input scope, the scale is 1:20.
5. Configure the jumpers at J14 according to how you plan to test the part.
   a. Outputs 0:3 enabled/disabled
   b. I2C address (0xD2 or 0xD4)
   c. Part active or powered-down
   d. Spread-spectrum setting (-0.25%, -0.5%, or OFF)
   e. Output frequency (100, 133, or 200 MHz)
6. Set +5V Select switch (SW3) based on how you will power the EVB, either via USB or via external +5 V supply.
7. Connect power, either via USB port or external +5 V power supply as chosen in previous step.

9. Board Schematic, BOM, and Layout

The schematic, BOM, and layout files for the Si52204-EVB can be found at: https://www.silabs.com/products/development-tools/timing/clock/si52204-evb-evaluation-kit.

10. Appendix: Typical Waveplots

The plots displayed in this section are provided to give the user an example of what they should expect to observe when measuring signals on this evaluation board with a good lab setup. These plots were taken on signals probed on-board using a Keysight 5 GHz differential probe (Ag 1132A) (for the differential waveforms), and Keysight 2 GHz high-impedance FET probe (Keysight N2796A) (for single-ended waveforms) and an 8 GHz bandwidth oscilloscope (Keysight Ag DSA90804A). Also, the EVB was configured with the 953 ohm resistors and the 2pf installed on Diff_0:3 as well as the 953 ohm resistor installed on REF_SA.

10.1 Reference Clock Output (Differential waveform)

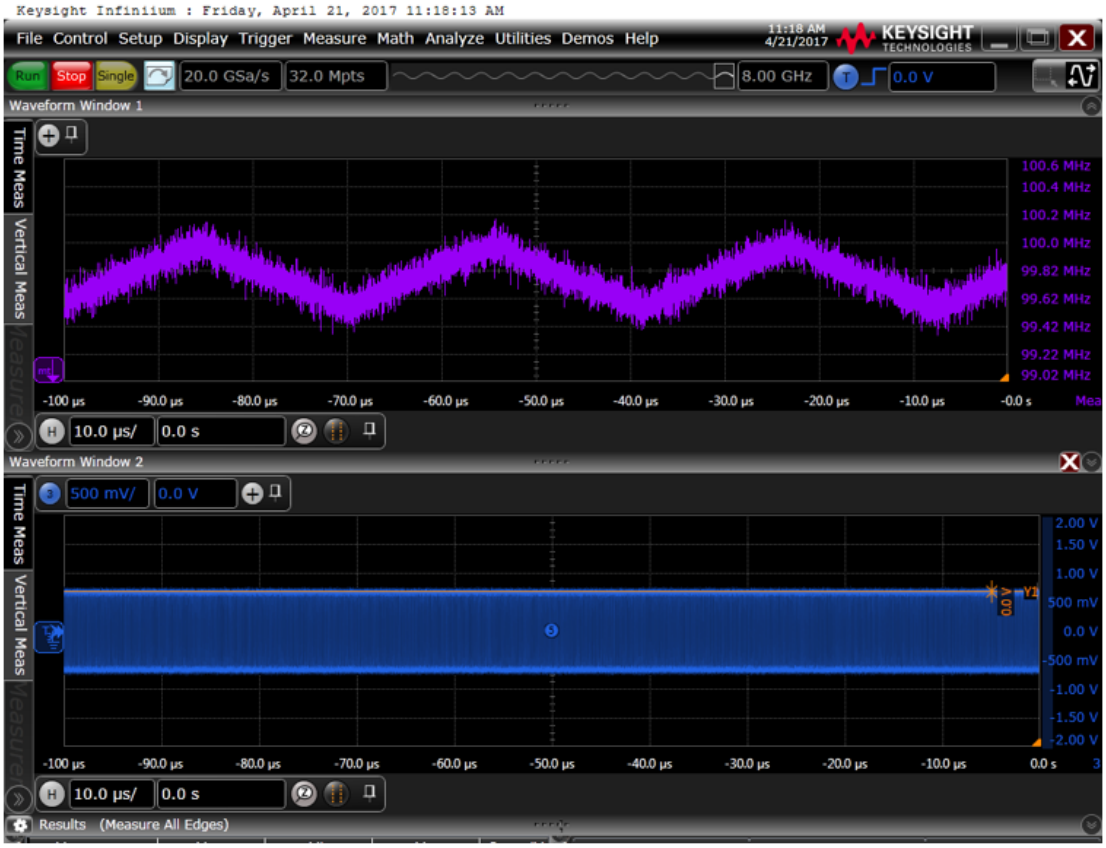
10.2 Differential Clock (DIFF_0) Output (Differential waveform)

10.3 Differential Clock (DIFF_0) Crossing Voltage (100MHz) (Single-ended waveform)

10.4 Differential Clock (DIFF_0) Crossing Voltage (200MHz) (Single-ended waveform)

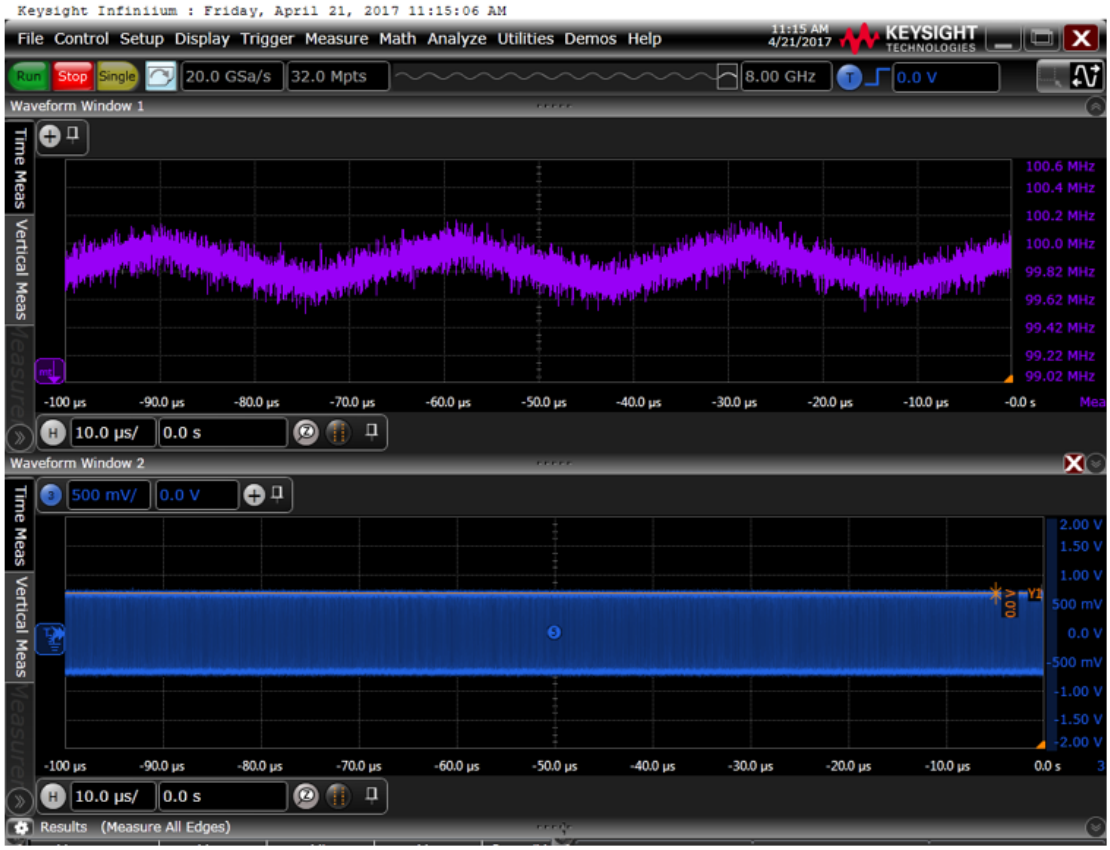
10.5 Spread Spectrum Clock @-0.5% spread (Differential waveform)

Frequency Trend Line



10.6 Spread Spectrum Clock @-0.25% spread (Differential waveform)

Frequency Trend Line



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