



# ITU-T G.8262 SYNCHRONOUS ETHERNET JITTER-ATTENUATING CLOCK MULTIPLIER

### Features

- Fully-compliant with ITU-T G.8262, EEC options 1 and 2.
- Generates any frequency from 8 kHz to 808 MHz.
- Ultra-low jitter clock outputs with jitter generation as low as 0.3 ps rms (12 kHz–20 MHz)
- Integrated loop filter with selectable loop bandwidth (0.1 Hz; 1 to 10 Hz)
- Dual clock inputs with manual or automatically controlled hitless switching
- Dual clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- LOL, LOS, FOS alarm outputs
- I<sup>2</sup>C or SPI programmable
- On-chip voltage regulator for 2.5 ±10% or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

### Applications

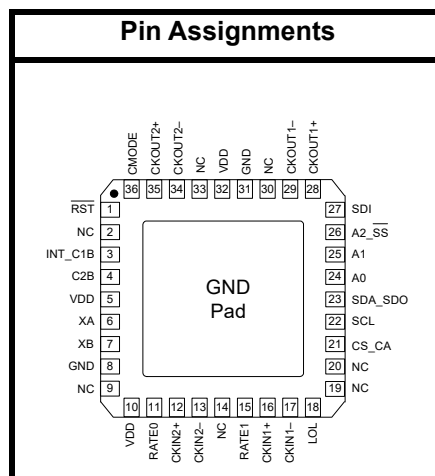
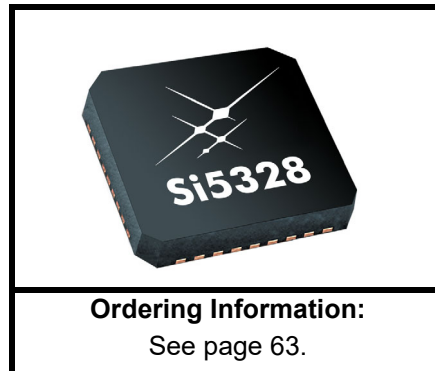
- G.8262 Synchronous Ethernet, EEC options 1 and 2
- GbE/10GbE/100GbE Synchronous Ethernet
- Carrier Ethernet switches, routers

### Description

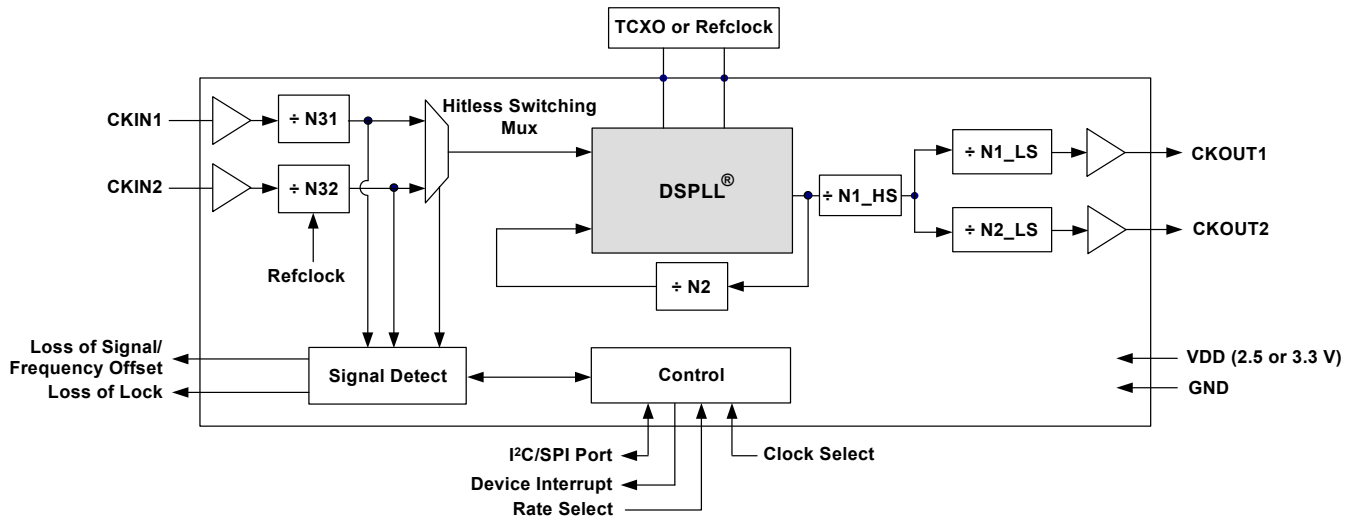
The Si5328 is a jitter-attenuating precision clock multiplier for Synchronous Ethernet applications requiring sub 1 ps jitter performance and ultra-low loop bandwidth. When combined with a low-wander, low-jitter reference oscillator, the Si5328 meets all of the wander, MTIE, TDEV, and other requirements listed in ITU-T G.8262/Y.1362. The Si5328 accepts two input clocks ranging from 8 kHz to 710 MHz and generates two output clocks ranging from 8 kHz to 808 MHz. The two outputs are divided down separately from a common source.

The Si5328 can also use the TCXO as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. The Si5328 input clock frequency and clock multiplication ratio are programmable through an I<sup>2</sup>C or SPI interface.

The Si5328 is based on Skyworks Solutions' third-generation DSPLL<sup>®</sup> technology, which provides frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 2.5 or 3.3 V supply, the Si5328 is ideal for providing clock multiplication and jitter attenuation in high-performance, Synchronous Ethernet timing applications.



## Functional Block Diagram



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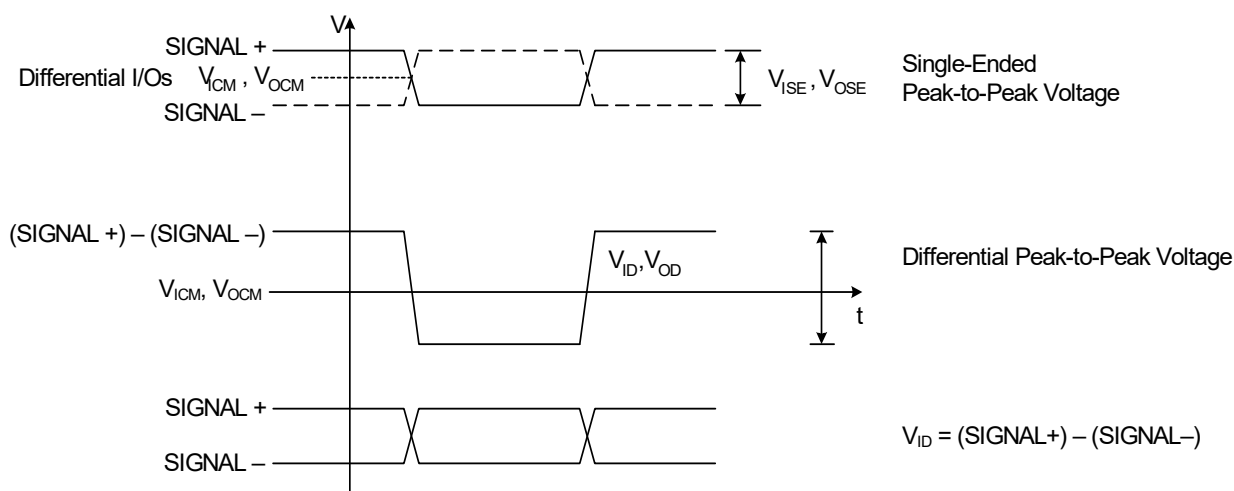
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## 1. Electrical Specifications

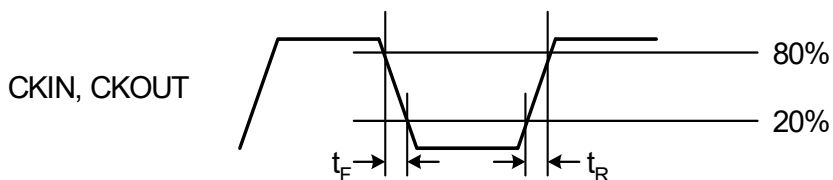
**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	$T_A$		-40	25	85	C
Supply Voltage during Normal Operation	$V_{DD}$	3.3 V Nominal	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V

**Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.



**Figure 1. Differential Voltage Characteristics**



**Figure 2. Rise/Fall Time Characteristics**

**Table 2. DC Characteristics** $(V_{DD} = 2.5\text{ V} \pm 10\%$  or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current <sup>1</sup>	$I_{DD}$	LVPECL Format 808 MHz Out Both CKOUTs Enabled	—	251	279	mA
		LVPECL Format 808 MHz Out 1 CKOUT Enabled	—	217	243	mA
		CMOS Format 25 MHz Out Both CKOUTs Enabled	—	204	234	mA
		CMOS Format 25 MHz Out 1 CKOUT Enabled	—	194	220	mA
		Disable Mode	—	165	—	mA
<b>CKINn Input Pins<sup>2</sup></b>						
Input Common Mode Voltage (Input Threshold Voltage)	$V_{ICM}$	2.5 V $\pm$ 10%	1	—	1.7	V
		3.3 V $\pm$ 10%	1.1	—	1.95	V
Input Resistance	$CKN_{RIN}$	Single-ended	20	40	60	k $\Omega$
Single-Ended Input Voltage Swing (See Absolute Specs)	$V_{ISE}$	$f_{CKIN} < 212.5\text{ MHz}$ See Figure 1.	0.2	—	—	$V_{PP}$
		$f_{CKIN} > 212.5\text{ MHz}$ See Figure 1.	0.25	—	—	$V_{PP}$
Differential Input Voltage Swing (See Absolute Specs)	$V_{ID}$	$f_{CKIN} < 212.5\text{ MHz}$ See Figure 1.	0.2	—	—	$V_{PP}$
		$f_{CKIN} > 212.5\text{ MHz}$ See Figure 1.	0.25	—	—	$V_{PP}$
<b>Notes:</b>						
1. Current draw is independent of supply voltage						
2. No under- or overshoot is allowed.						
3. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 312.5\text{ MHz}$ .						
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.						

**Table 2. DC Characteristics (Continued)**

( $V_{DD} = 2.5\text{ V} \pm 10\%$  or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Output Clocks (CKOUTn)</b>						
Common Mode	$CKO_{VCM}$	LVPECL 100 $\Omega$ load line-to-line	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
Differential Output Swing <sup>3</sup>	$CKO_{VD}$	LVPECL 100 $\Omega$ load line-to-line	1.1	—	1.9	$V_{PP}$
Single Ended Output Swing <sup>3</sup>	$CKO_{VSE}$	LVPECL 100 $\Omega$ load line-to-line	0.5	—	0.93	$V_{PP}$
Differential Output Voltage <sup>3</sup>	$CKO_{VD}$	CML 100 $\Omega$ load line-to-line	350	425	500	$mV_{PP}$
Common Mode Output Voltage <sup>3</sup>	$CKO_{VCM}$	CML 100 $\Omega$ load line-to-line	—	$V_{DD} - 0.36$	—	V
Differential Output Voltage <sup>3</sup>	$CKO_{VD}$	LVDS 100 $\Omega$ load line-to-line	500	700	900	$mV_{PP}$
		Low Swing LVDS 100 $\Omega$ load line-to-line	350	425	500	$mV_{PP}$
Common Mode Output Voltage <sup>3</sup>	$CKO_{VCM}$	LVDS 100 $\Omega$ load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	$CKO_{RD}$	CML, LVPECL, LVDS	—	200	—	$\Omega$
Output Voltage Low	$CKO_{VOLLH}$	CMOS	—	—	0.4	V
Output Voltage High	$CKO_{VOHLH}$	$V_{DD} = 2.25\text{ V}$ CMOS	$0.8 \times V_{DD}$	—	—	V
<b>Notes:</b>						
1. Current draw is independent of supply voltage						
2. No under- or overshoot is allowed.						
3. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 312.5\text{ MHz}$ .						
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.						

**Table 2. DC Characteristics (Continued)** $(V_{DD} = 2.5\text{ V} \pm 10\%$  or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Drive Current (CMOS driving into $CKO_{VOL}$ for output low or $CKO_{VOH}$ for output high. $CKOUT+$ and $CKOUT-$ shorted externally)	$CKO_{IO}$	$ICMOS[1:0] = 11$ $V_{DD} = 2.5\text{ V}$	—	20	—	mA
		$ICMOS[1:0] = 10$ $V_{DD} = 2.5\text{ V}$	—	15	—	mA
		$ICMOS[1:0] = 01$ $V_{DD} = 2.5\text{ V}$	—	10	—	mA
		$ICMOS[1:0] = 00$ $V_{DD} = 2.5\text{ V}$	—	5	—	mA
		$ICMOS[1:0] = 11$ $V_{DD} = 3.3\text{ V}$	—	32	—	mA
		$ICMOS[1:0] = 10$ $V_{DD} = 3.3\text{ V}$	—	24	—	mA
		$ICMOS[1:0] = 01$ $V_{DD} = 3.3\text{ V}$	—	16	—	mA
		$ICMOS[1:0] = 00$ $V_{DD} = 3.3\text{ V}$	—	8	—	mA
<b>2-Level LVCMOS Input Pins</b>						
Input Voltage Low	$V_{IL}$	$V_{DD} = 2.25\text{ V}$	—	—	0.7	V
		$V_{DD} = 2.97\text{ V}$	—	—	0.8	V
Input Voltage High	$V_{IH}$	$V_{DD} = 2.25\text{ V}$	1.8	—	—	V
		$V_{DD} = 3.63\text{ V}$	2.5	—	—	V
<b>Notes:</b>						
1. Current draw is independent of supply voltage						
2. No under- or overshoot is allowed.						
3. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 312.5\text{ MHz}$ .						
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.						

**Table 2. DC Characteristics (Continued)**

( $V_{DD} = 2.5\text{ V} \pm 10\%$  or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>3-Level Input Pins<sup>4</sup></b>						
Input Voltage Low	$V_{ILL}$		—	—	$0.15 \times V_{DD}$	V
Input Voltage Mid	$V_{IMM}$		$0.45 \times V_{DD}$	—	$0.55 \times V_{DD}$	V
Input Voltage High	$V_{IHH}$		$0.85 \times V_{DD}$	—	—	V
Input Low Current	$I_{ILL}$	See Note 4	-20	—	—	$\mu\text{A}$
Input Mid Current	$I_{IMM}$	See Note 4	-2	—	+2	$\mu\text{A}$
Input High Current	$I_{IHH}$	See Note 4	—	—	20	$\mu\text{A}$
<b>LVC MOS Output Pins</b>						
Output Voltage Low	$V_{OL}$	$I_O = 2\text{ mA}$ $V_{DD} = 2.25\text{ V}$	—	—	0.4	V
Output Voltage Low		$I_O = 2\text{ mA}$ $V_{DD} = 2.97\text{ V}$	—	—	0.4	V
Output Voltage High	$V_{OH}$	$I_O = -2\text{ mA}$ $V_{DD} = 2.25\text{ V}$	$V_{DD} - 0.4$	—	—	V
Output Voltage High		$I_O = -2\text{ mA}$ $V_{DD} = 2.97\text{ V}$	$V_{DD} - 0.4$	—	—	V
Disabled Leakage Current	$I_{OZ}$	RSTb = 0	-100	—	100	$\mu\text{A}$
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>1. Current draw is independent of supply voltage</li> <li>2. No under- or overshoot is allowed.</li> <li>3. LVPECL, CML, LVDS and low-swing LVDS measured with <math>F_o = 312.5\text{ MHz}</math>.</li> <li>4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.</li> </ol>						



**Table 3. AC Characteristics** $(V_{DD} = 2.5 \pm 10\%$  or  $3.3 \text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Single-Ended Reference Clock Input Pin XA (XB with cap to GND)</b>						
Input Resistance	$XA_{RIN}$	RATE[1:0] = LM, ML, MH, ac coupled	—	12	—	k $\Omega$
Input Voltage Swing	$XA_{VPP}$	RATE[1:0] = LM, ML, MH, ac coupled	0.5	—	1.2	$V_{PP}$
<b>Differential Reference Clock Input Pins (XA/XB)</b>						
Input Voltage Swing	$XA/XB_{VPP}$	RATE[1:0] = LM, ML, MH	0.5	—	1.2	$V_{PP}$ , each.
<b>CKINn Input Pins</b>						
Input Frequency	$CKN_F$		0.008	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	$CKN_{DC}$	Input frequency > 225 MHz	40	—	60	%
		Input frequency < 225 MHz refers to both high and low widths	2	—	—	ns
Input Capacitance	$CKN_{CIN}$		—	—	3	pF
Input Rise/Fall Time	$CKN_{TRF}$	20–80% See Figure 2	—	—	11	ns
<b>CKOUTn Output Pins</b>						
(See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not configured for CMOS)	$CKO_F$	$N1 \geq 6$	0.008	—	808	MHz
Maximum Output Frequency in CMOS Format	$CKO_F$		—	—	212.5	MHz
Output Rise/Fall (20–80%) @ 212.5 MHz output	$CKO_{TRF}$	CMOS Output $V_{DD} = 2.25$ $C_{LOAD} = 5 \text{ pF}$	—	—	8	ns
Output Rise/Fall (20–80%) @ 212.5 MHz output	$CKO_{TRF}$	CMOS Output $V_{DD} = 2.97$ $C_{LOAD} = 5 \text{ pF}$	—	—	2	ns
<b>Notes:</b>						
1. Lock and settle times may change with different f3, loop BW, and VCO frequency values. Contact Skyworks Solutions for further details.						
2. See Section 9 of "AN775: Si5328 Synchronous Ethernet Compliance Test Report" for more details.						

**Table 3. AC Characteristics (Continued)**

( $V_{DD} = 2.5 \pm 10\%$  or  $3.3 \text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall (20–80%) @ 312.5 MHz output	$CKO_{TRF}$	LVPECL, LVDS or CML Output	—	230	350	ps
Output Duty Cycle Uncertainty @ 808 MHz	$CKO_{DC}$	100 $\Omega$ Load Line-to-Line Measured at 50% Point (Not for CMOS)	45	—	55	%
<b>LVC MOS Input Pins</b>						
Minimum Reset Pulse Width	$t_{RSTMN}$		1			$\mu\text{s}$
Reset to Microprocessor Access Ready	$t_{READY}$				10	ms
Input Capacitance	$C_{in}$		—	—	3	pF
<b>LVC MOS Output Pins</b>						
Rise/Fall Times	$t_{RF}$	$C_{LOAD} = 20\text{pf}$ See Figure 2	—	25	—	ns
LOS <sub>n</sub> Trigger Window	$LOS_{TRIG}$	From last $CKIN_n \uparrow$ to $\downarrow$ Internal detection of LOS <sub>n</sub> $N3 \neq 1$	—	—	$4.5 \times N3$	$T_{CKIN}$
Time to Clear LOL after LOS Cleared	$t_{CLRLOL}$	$\downarrow$ LOS to $\downarrow$ LOL Fold = Fnew Stable Xa/XB reference	—	10	—	ms
<b>Device Skew</b>						
Output Clock Skew	$t_{SKEW}$	$\uparrow$ of $CKOUT_n$ to $\uparrow$ of $CKOUT\_m$ , $CKOUT_n$ and $CKOUT\_m$ at same frequency and signal format <u>PHASEOFFSET = 0</u> <u>CKOUT_ALWAYS_ON = 1</u> <u>SQ_ICAL = 1</u>	—	—	100	ps
Phase Change due to Temperature Variation	$t_{TEMP}$	Max phase changes from – 40 to +85 $^\circ\text{C}$ , stable XAXB reference	—	300	500	ps
<b>Notes:</b>						
1. Lock and settle times may change with different f <sub>3</sub> , loop BW, and VCO frequency values. Contact Skyworks Solutions for further details.						
2. See Section 9 of “AN775: Si5328 Synchronous Ethernet Compliance Test Report” for more details.						

**Table 3. AC Characteristics (Continued)**(V<sub>DD</sub> = 2.5 ±10% or 3.3 V ±10%, T<sub>A</sub> = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>PLL Performance</b> (f <sub>in</sub> = f <sub>out</sub> = 346 MHz; BW = 0.088 Hz; LVPECL)						
Lock Time <sup>1</sup>	t <sub>LOCKMP</sub>	Start of ICAL to LOL low, LOCKT = 4, FASTLOCK enabled	—	2	—	s
		Start of ICAL to LOL low, LOCKT = 1, FASTLOCK enabled	—	12.5	—	s
Settle Time <sup>1</sup>	t <sub>SETTLE</sub>	Start of ICAL to output phase within 45 degrees of final value, LOCKT = 4, FASTLOCK enabled	—	1	—	s
		Start of ICAL to output phase within 45 degrees of final value, LOCKT = 1, FASTLOCK enabled	—	1	—	s
Output Clock Phase Change	t <sub>P_STEP</sub>	After clock switch f <sub>3</sub> ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J <sub>PK</sub>		—	0.05	0.2	dB
Jitter/Wander Tolerance <sup>2</sup>	J <sub>TOL</sub>	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise f <sub>out</sub> = 156.25 MHz	CKO <sub>PN</sub>	1 kHz Offset	—	-120	—	dBc/Hz
		10 kHz Offset	—	-128	—	dBc/Hz
		100 kHz Offset	—	-130	—	dBc/Hz
		1 MHz Offset	—	-144	—	dBc/Hz
Subharmonic Noise	SP <sub>SUBH</sub>	Phase Noise @ 100 kHz Offset	—	-88	—	dBc
Spurious Noise	SP <sub>SPUR</sub>	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	-93	—	dBc
<b>Notes:</b>						
1. Lock and settle times may change with different f <sub>3</sub> , loop BW, and VCO frequency values. Contact Skyworks Solutions for further details.						
2. See Section 9 of “AN775: Si5328 Synchronous Ethernet Compliance Test Report” for more details.						

**Table 4. Microprocessor Control**

( $V_{DD} = 2.5 \pm 10\%$  or  $3.3 \text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>I<sup>2</sup>C Bus Lines (SDA, SCL)</b>						
Input Voltage Low	$V_{IL_{I2C}}$		—	—	$0.25 \times V_{DD}$	V
Input Voltage High	$V_{IH_{I2C}}$		$0.7 \times V_{DD}$	—	$V_{DD}$	V
Input Current	$I_{I2C}$	$V_{IN} = 0.1 \times V_{DD}$ to $0.9 \times V_{DD}$	-10	—	10	$\mu\text{A}$
Hysteresis of Schmitt trigger inputs	$V_{HYS_{I2C}}$		$0.05 \times V_{DD}$	—	—	V
Output Voltage Low	$V_{OL_{I2C}}$	$I_O = 3 \text{ mA}$	—	—	0.4	V

**Table 4. Microprocessor Control (Continued)**(V<sub>DD</sub> = 2.5 ±10% or 3.3 V ±10%, T<sub>A</sub> = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SPI Specifications</b>						
Duty Cycle, SCLK	t <sub>DC</sub>	SCLK = 10 MHz	40	—	60	%
Cycle Time, SCLK	t <sub>c</sub>		100	—	—	ns
Rise Time, SCLK	t <sub>r</sub>	20–80%	—	—	25	ns
Fall Time, SCLK	t <sub>f</sub>	20–80%	—	—	25	ns
Low Time, SCLK	t <sub>lsc</sub>	20–20%	30	—	—	ns
High Time, SCLK	t <sub>hsc</sub>	80–80%	30	—	—	ns
Delay Time, SCLK Fall to SDO Active	t <sub>d1</sub>		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	t <sub>d2</sub>		—	—	25	ns
Delay Time, SS Rise to SDO Tri-state	t <sub>d3</sub>		—	—	25	ns
Setup Time, SS to SCLK Fall	t <sub>su1</sub>		25	—	—	ns
Hold Time, SS to SCLK Rise	t <sub>h1</sub>		20	—	—	ns
Setup Time, SDI to SCLK Rise	t <sub>su2</sub>		25	—	—	ns
Hold Time, SDI to SCLK Rise	t <sub>h2</sub>		20	—	—	ns
Delay Time between Slave Selects	t <sub>cs</sub>		25	—	—	ns

**Table 5. Jitter Generation<sup>1,2,3,4,5,6</sup>**

Symbol	Filter	Output Frequency	Min	Typ	Max	Unit
JGEN	12 kHz to 20 MHz	125 MHz	—	331	—	fs, RMS
JGEN	10 kHz to 1 MHz	125 MHz	—	287	—	fs, RMS
JGEN	12 kHz to 20 MHz	156.25 MHz	—	308	—	fs, RMS
JGEN	10 kHz to 1 MHz	156.25 MHz	—	263	—	fs, RMS

**Notes:**

1. Input frequency = 25 MHz.
2. XAXB reference = Rakon 40 MHz TCXO model RTX7050A, part number 509768.
3. Vdd = 3.3 V.
4. Clock output = LVPECL.
5. Loop bandwidth = 0.085 Hz.
6. Using Agilent E5052B.

**Table 6. Thermal Characteristics**(V<sub>DD</sub> = 2.5 ±10% or 3.3 V ±10%, T<sub>A</sub> = -40 to 85 °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still Air	32	C°/W
Thermal Resistance Junction to Case	$\theta_{JC}$	Still Air	14	C°/W

**Table 7. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage	V <sub>DD</sub>		-0.5	—	3.8	V
LVC MOS Input Voltage	V <sub>DIG</sub>		-0.3		V <sub>DD</sub> +0.3	V
CKINn Voltage Level Limits	CKN <sub>VIN</sub>		0	—	V <sub>DD</sub>	V
XA/XB Voltage Level Limits	XA <sub>VIN</sub>		0	—	1.2	V
Operating Junction Temperature	T <sub>JCT</sub>		-55	—	150	°C
Storage Temperature Range	T <sub>STG</sub>		-55	—	150	°C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN-			2	—	—	kV
ESD MM Tolerance; All pins except CKIN+/CKIN-			150	—	—	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN-			750	—	—	V
ESD MM Tolerance; CKIN+/CKIN-			100	—	—	V
Latch-up Tolerance			JESD78 Compliant			
<p><b>*Note:</b> Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.</p>						

## 2. Typical Phase Noise Performance

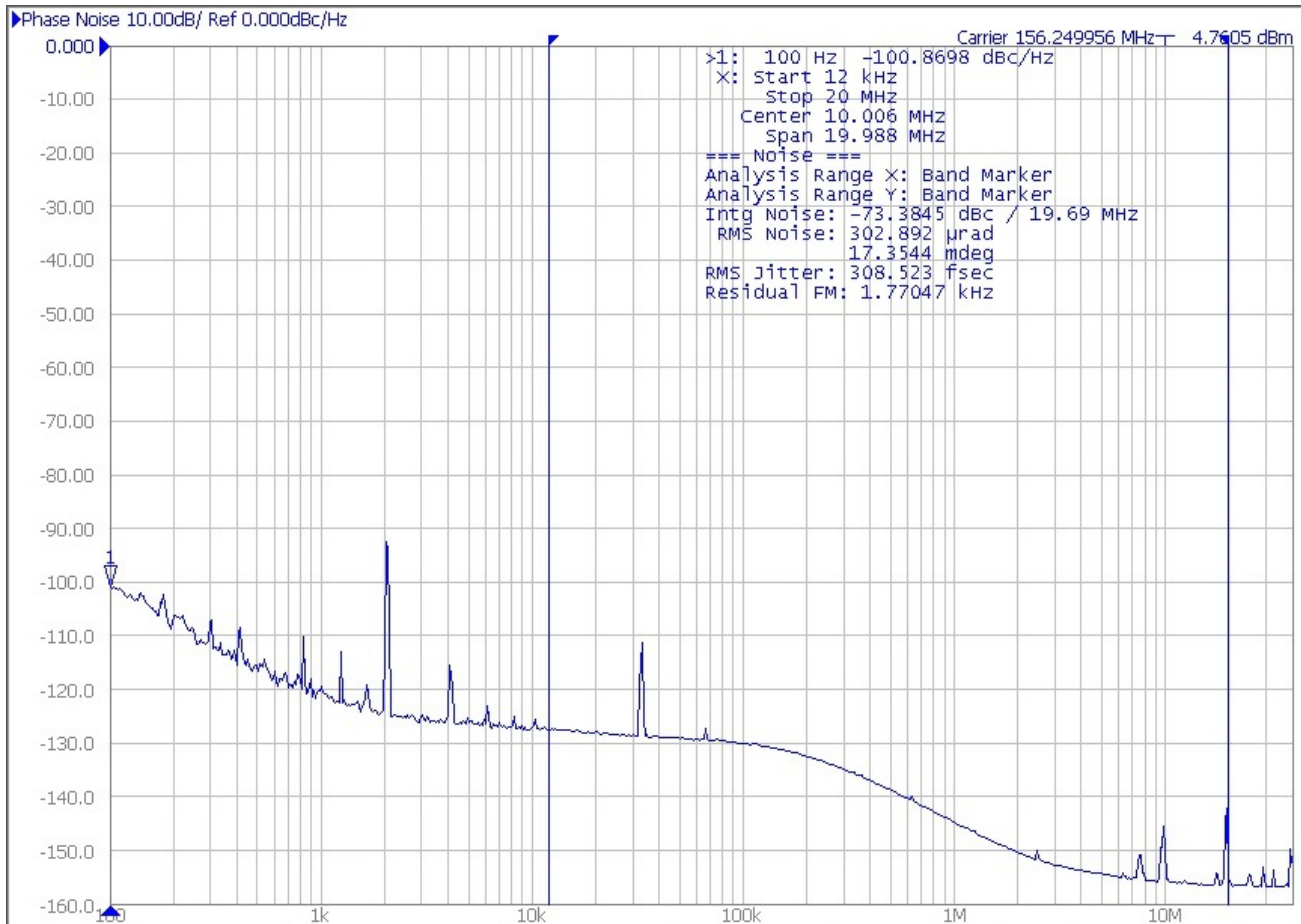


Figure 3. Typical Phase Noise Plot

Table 8. RMS Jitter Values

Jitter Band	Jitter (rms)
10 kHz to 1 MHz	263 fs
12 kHz to 20 MHz	309 fs

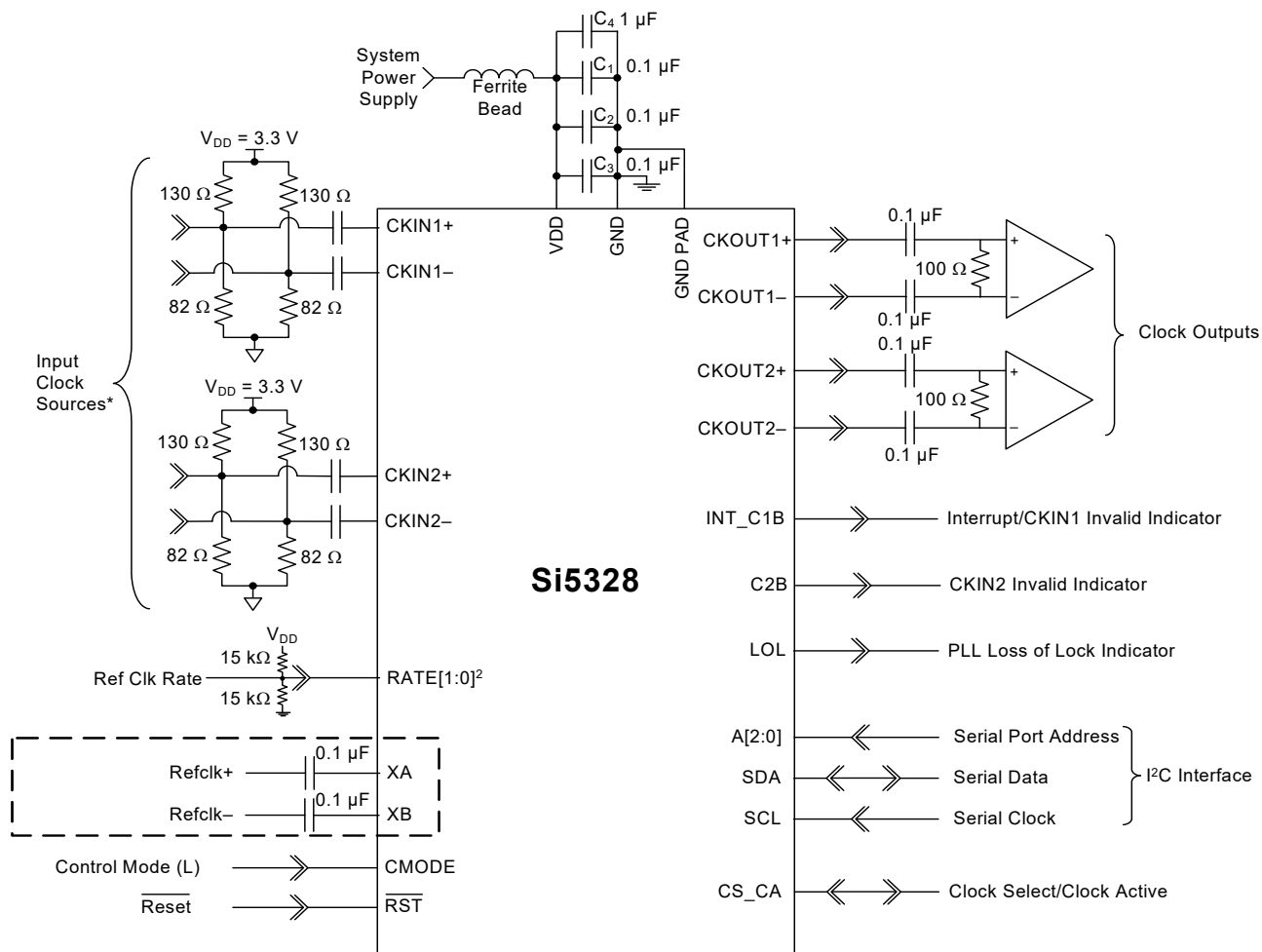
**Notes:**

- input frequency = 25 MHz.
- XAXB reference = Rakon 40 MHz TCXO model RTX7050A, part number 509768.
- Vdd = 3.3 V.
- Clock output = LVPECL.
- Loop bandwidth = 0.085 Hz.
- Using Agilent E5052B.



### 3. Typical Application Circuit

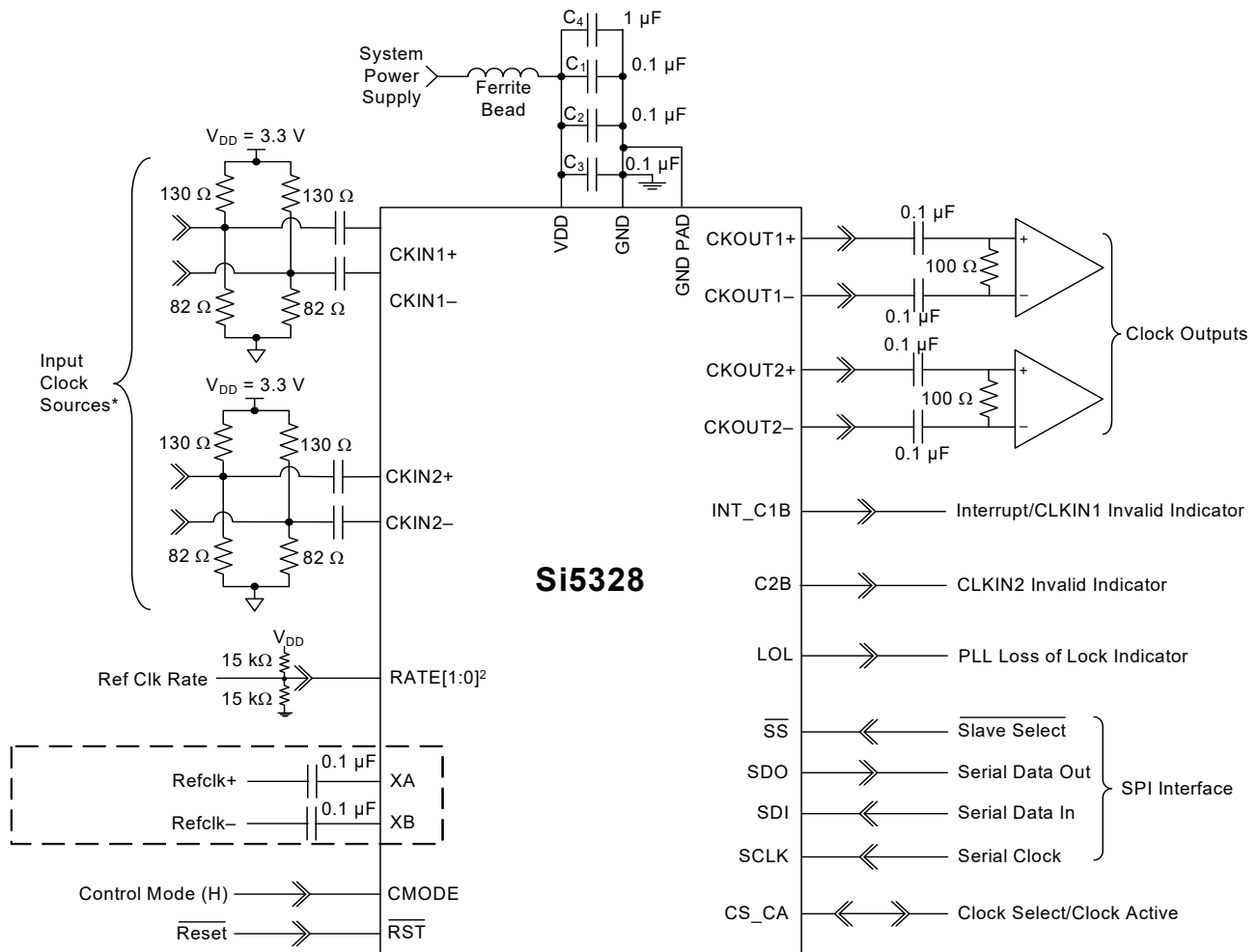
**Note:** For an example schematic and layout, refer to the Si5328-EVB User's Guide.



**Notes:**

1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (V<sub>DD</sub>/2), and H (V<sub>DD</sub>).
3. I<sup>2</sup>C-required pull-up resistors not shown.

**Figure 4. Si5328 Typical Application Circuit (I<sup>2</sup>C Control Mode)**

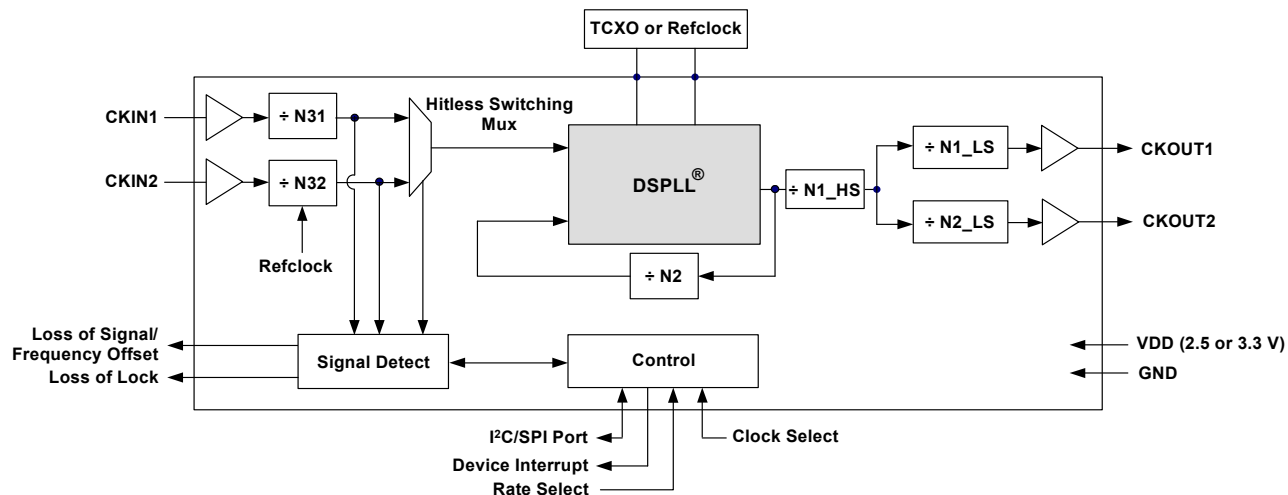


**Notes:**

1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).

**Figure 5. Si5328 Typical Application Circuit (SPI Control Mode)**

## 4. Functional Description



**Figure 6. Functional Block Diagram**

The Si5328 is a jitter-attenuating precision clock multiplier for Synchronous Ethernet applications requiring sub 1 ps jitter performance and ultra-low loop bandwidth. When combined with a low-wander reference oscillator, the Si5328 meets all of the wander, MTIE, TDEV, and other requirements that are listed in ITU-T G.8262/Y.1362. The Si5328 accepts two input clocks ranging from 8 kHz to 710 MHz and generates two output clocks ranging from 8 kHz to 808 MHz. The Si5328 can also use its TCXO as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for each input clock and output clock, so the Si5328 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5328 input clock frequency and clock multiplication ratio are programmable through an I<sup>2</sup>C or SPI interface. Skyworks Solutions offers a PC-based software utility, DSPLLsim, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption.

This utility can be downloaded from <https://www.skyworksinc.com/en/Application-Pages/DSPLL>.

The Si5328 is based on Skyworks Solutions' 3rd-generation DSPLL<sup>®</sup> technology, which provides any frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5328 PLL loop bandwidth is digitally programmable and supports a range from less than 0.1 Hz to 6 Hz. The DSPLLsim software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5328 supports hitless switching between the two synchronous input clocks in compliance with G.8262 that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (maximum 200 ps phase transient). Manual and automatic revertive and non-revertive input clock switching options are available. The Si5328 monitors both input clocks for loss-of-signal (LOS) and provides a LOS alarm (INT\_C1B and C2B) when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5328 also monitors frequency offset alarms (FOS), which indicate if an input clock is within a specified frequency band relative to the frequency of a reference clock. Both Stratum 3/3E and SONET Minimum Clock (SMC) FOS thresholds are supported. The Si5328 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average frequency that existed for a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5328 has two differential clock outputs. The electrical format of each clock output is independently programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption.

The phase of one output clock may be adjusted in relation to the phase of the other output clock with resolution that varies from 800 ps to 2.2 ns, depending on the PLL divider settings. See Table 9 for instructions on ensuring output-to-output alignment. The input to output skew is not specified or controlled. The DSPLLsim software utility determines the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 2.5 or 3.3 V supply.

## 4.1. External XAXB Reference

In order to achieve the levels of performance required by G.8262, care must be exercised when selecting an XA/XB reference. To meet the wander specifications in G.8262, a TCXO or OCXO will be needed.

“AN775: Si5328 ITU-T G.8262 SyncE Compliance Test

Report” is a G.8262 test report using a 40 MHz Rakon RTX7050A-109 TCXO. See “AN776: Using the Si5328 in a G.8262 Compliant SyncE Application” for a discussion of how to select and best use a TCXO as well as a list of other potential TCXO sources.

## 4.2. Further Documentation

Consult the Skyworks Solutions Si53xx Any Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5328 functions. Additional design support is available from Skyworks Solutions through your distributor.

Skyworks Solutions has developed a PC-based software utility called DSPLLsim to simplify device configuration, including frequency planning and loop bandwidth selection.

The FRM and this utility can be downloaded from <https://www.skyworksinc.com/en/Application-Pages/DSPLL>.

**Table 9. CKOUT\_ALWAYS\_ON and SQ\_ICAL Truth Table**

CKOUT_ALWAYS_ON	SQ_ICAL	Results
0	0	CKOUT OFF until after the first ICAL
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)
1	0	CKOUT always ON, including during an ICAL
1	1	CKOUT always ON, including during an ICAL. Use these settings to preserve output-to-output skew

## 5. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written.

Register	D7	D6	D5	D4	D3	D2	D1
0		FREE_RUN	CKOUT_ALWAYS_ON				BYPASS
1					CK_PRIOR2[1:0]		
2	BWSEL_REG[3:0]						
3	CKSEL_REG[1:0]		DHOLD	SQ_ICAL			
4	AUTOSEL_REG[1:0]			HST_DEL[4:0]			
5	ICMOS[1:0]						
6		SLEEP	SFOUT2_REG[2:0]				SFOUT1
7							FOSREN
8	HLOG_2[1:0]		HLOG_1[1:0]				
9	HIST_AVG[4:0]						
10					DSBL2_REG	DSBL1_REG	
11							PD_C
19	FOS_EN	FOS_THR[1:0]		VALTIME[1:0]			LOCK
20					CK2_BAD_PIN	CK1_BAD_PIN	LOL_
21							CK1_AC
22					CK_ACTV_POL	CK_BAD_POL	LOL_
23						LOS2_MSK	LOS1_
24						FOS2_MSK	FOS1_
25	N1_HS[2:0]						
31						NC1_LS[19:16]	
32					NC1_LS[15:8]		
33					NC1_LS[7:0]		
34						NC2_LS[19:16]	

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Register	D7	D6	D5	D4	D3	D2	D1	
35	NC2_LS[15:8]							
36	NC2_LS[7:0]							
40	N2_HS[2:0]			N2_LS[19:16]				
41	N2_LS[15:8]							
42	N2_LS[7:0]							
43	N31[19:16]							
44	N31[15:8]							
45	N31[7:0]							
46	N32[19:16]							
47	N32[15:8]							
48	N32[7:0]							
55	CLKIN2RATE[2:0]			CLKIN1RATE[2:0]				
128	CK2_ACT							
129						LOS2_INT	LOS1_INT	
130	DIGHOLDVALID						FOS2_INT	FOS1_INT
131						LOS2_FLG	LOS1_FLG	
132						FOS2_FLG	FOS1_FLG	
134	PARTNUM_RO[11:4]							
135	PARTNUM_RO[3:0]				REVID_RO[3:0]			
136	RST_REG	ICAL						
137								
138	LOS2_EN[19:16]							
139	LOS2_EN[0:0]			LOS1_EN[0:0]		FOS2_EN[0:0]		
142	INDEPENDENTSKEW1[7:0]							
143	INDEPENDENTSKEW2[7:0]							

## 6. Register Descriptions

### Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FREE_RUN	CKOUT_ALWAYS_ON				BYPASS_REG	
Type	R	R/W	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7	Reserved	<b>Reserved.</b>
6	FREE_RUN	<b>Free Run.</b> Internal to the device, route XA/XB to CKIN2. This allows the device to lock to its XA-XB reference. 0: Disable 1: Enable
5	CKOUT_ALWAYS_ON	<b>CKOUT Always On.</b> This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 9 on page 20. 0: Squelch output until part is calibrated (ICAL). 1: Provide an output. Note: The frequency may be significantly off and variable until the part is calibrated.
4:2	Reserved	<b>Reserved.</b>
1	BYPASS_REG	<b>Bypass Register.</b> This bit enables or disables the PLL bypass mode. Use only when the device is in digital hold or before the first ICAL. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing the PLL. Bypass mode does not support CMOS clock outputs.
0	Reserved	<b>Reserved.</b>

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## Register 1.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				CK_PRIOR2 [1:0]		CK_PRIOR1 [1:0]	
Type	R				R/W		R/W	

Reset value = 1110 0100

Bit	Name	Function
7:4	Reserved	<b>Reserved.</b>
3:2	CK_PRIOR2 [1:0]	<b>CK_PRIOR 2.</b> Selects which of the input clocks will be 2nd priority in the autoselection state machine. 00: CKIN1 is 2nd priority. 01: CKIN2 is 2nd priority. 10: Reserved 11: Reserved
1:0	CK_PRIOR1 [1:0]	<b>CK_PRIOR 1.</b> Selects which of the input clocks will be 1st priority in the autoselection state machine. 00: CKIN1 is 1st priority. 01: CKIN2 is 1st priority. 10: Reserved 11: Reserved

## Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]				Reserved			
Type	R/W				R			

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	<b>BWSEL_REG.</b> Selects nominal f3dB bandwidth for PLL. See <i>DSPLLsim</i> for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	Reserved	<b>Reserved.</b>



**Register 3.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	CKSEL_REG [1:0]		DHOLD	SQ_ICAL	Reserved			
<b>Type</b>	R/W		R/W	R/W	R			

Reset value = 0000 0101

Bit	Name	Function
7:6	CKSEL_REG [1:0]	<p><b>CKSEL_REG.</b></p> <p>If the device is operating in register-based manual clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1 and AUTOSEL_REG = 00, the CS_CA input pin continues to control clock selection and CKSEL_REG is of no consequence.</p> <p>00: CKIN_1 selected. 01: CKIN_2 selected. 10: Reserved 11: Reserved</p>
5	DHOLD	<p><b>DHOLD.</b></p> <p>Forces the part into digital hold. This bit overrides all other manual and automatic clock selection controls.</p> <p>0: Normal operation. 1: Force digital hold mode. Overrides all other settings and ignores the quality of all of the input clocks.</p>
4	SQ_ICAL	<p><b>SQ_ICAL.</b></p> <p>This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 9 on page 20.</p> <p>0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.</p>
3:0	Reserved	<b>Reserved.</b>

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## Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	AUTOSEL_REG [1:0]		Reserved	HIST_DEL [4:0]				
<b>Type</b>	R/W		R	R/W				

Reset value = 0001 0010

Bit	Name	Function
7:6	AUTOSEL_REG [1:0]	<b>AUTOSEL_REG [1:0].</b> Selects method of input clock selection to be used. 00: Manual (either register or pin controlled, see CKSEL_PIN) 01: Automatic Non-Revertive 10: Automatic Revertive 11: Reserved See the Si53xx Family Reference Manual for a detailed description.
5	Reserved	<b>Reserved.</b>
4:0	HIST_DEL [4:0]	<b>HIST_DEL [4:0].</b> Selects amount of delay to be used in generating the history information used for Digital Hold. See the Si53xx Family Reference Manual for a detailed description.

## Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	ICMOS [1:0]		Reserved					
<b>Type</b>	R/W		R					

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	<b>ICMOS [1:0].</b> When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 2.5 V operation. These values assume CKOUT+ is tied to CKOUT-. 00: 8 mA/5 mA 01: 16 mA/10 mA 10: 24 mA/15 mA 11: 32 mA/20 mA
5:0	Reserved	<b>Reserved.</b>

**Register 6.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved	SLEEP	SFOUT2_REG [2:0]			SFOUT1_REG [2:0]		
<b>Type</b>	R	R/W	R/W			R/W		

Reset value = 0010 1101

Bit	Name	Function
7	Reserved	<b>Reserved.</b>
6	SLEEP	<b>SLEEP.</b> In sleep mode, all clock outputs are disabled and the maximum amount of internal circuitry is powered down to reduce power dissipation and noise generation. This bit overrides the SFOUTn_REG[2:0] output signal format settings. 0: Normal operation 1: Sleep mode
5:3	SFOUT2_REG [2:0]	<b>SFOUT2_REG [2:0].</b> Controls output signal format and disable for CKOUT2 output buffer. 000: Reserved 001: Disable 010: CMOS (Bypass mode not supported) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS
2:0	SFOUT1_REG [2:0]	<b>SFOUT1_REG [2:0].</b> Controls output signal format and disable for CKOUT1 output buffer. 000: Reserved 001: Disable 010: CMOS (Bypass mode not supported) 011: Low swing LVDS 100: Reserved 101: LVPECL 111: LVDS

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## Register 7.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					FOSREFSEL [2:0]		
Type	R					R/W		

Reset value = 0010 1010

Bit	Name	Function
7:3	Reserved.	<b>Reserved.</b>
2:0	FOSREFSEL [2:0]	<b>FOSREFSEL [2:0].</b> Selects which input clock is used as the reference frequency for frequency offset (FOS) alarms. 000: XA/XB (External reference) 001: CKIN1 010: CKIN2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

**Register 8.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	HLOG_2[1:0]		HLOG_1[1:0]		Reserved			
<b>Type</b>	R/W		R/W		R			

Reset value = 0000 0000

Bit	Name	Function
7:6	HLOG_2 [1:0]	<b>HLOG_2 [1:0].</b> 00: Normal operation 01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
5:4		<b>HLOG_1 [1:0].</b> 00: Normal operation 01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
3:0	Reserved	<b>Reserved.</b>

**Register 9.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	HIST_AVG [4:0]					Reserved		
<b>Type</b>	R/W					R	R	R

Reset value = 1100 0000

Bit	Name	Function
7:3	HIST_AVG [4:0]	<b>HIST_AVG [4:0].</b> Selects amount of averaging time to be used in generating the history information for Digital Hold. See the Si53xx Family Reference Manual for a detailed description
2:0	Reserved	<b>Reserved.</b>

## Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				DSBL2_REG	DSBL1_REG	Reserved	Reserved
Type	R				R/W	R/W	R	R

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	<b>Reserved.</b>
3	DSBL2_REG	<b>DSBL2_REG.</b> This bit controls the powerdown of the CKOUT2 output buffer. If disable mode is selected, the N2_LS output divider is also powered down. 0: CKOUT2 enabled 1: CKOUT2 disabled
2	DSBL1_REG	<b>DSBL1_REG.</b> This bit controls the powerdown of the CKOUT1 output buffer. If disable mode is selected, the N1_LS output divider is also powered down. 0: CKOUT1 enabled 1: CKOUT1 disabled
1:0	Reserved	<b>Reserved.</b>

**Register 11.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved						PD_CK2	PD_CK1
<b>Type</b>	R						R/W	R/W

Reset value = 0100 0000

Bit	Name	Function
7:2	Reserved	<b>Reserved.</b>
1	PD_CK2	<b>PD_CK2.</b> This bit controls the powerdown of the CKIN2 input buffer. 0: CKIN2 enabled 1: CKIN2 disabled
0	PD_CK1	<b>PD_CK1.</b> This bit controls the powerdown of the CKIN1 input buffer. 0: CKIN1 enabled 1: CKIN1 disabled

## Register 19.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	FOS_EN	FOS_THR [1:0]		VALTIME [1:0]		LOCKT [2:0]		
<b>Type</b>	R/W	R/W		R/W		R/W		

Reset value = 0010 1100

Bit	Name	Function
7	FOS_EN	<p><b>FOS_EN.</b></p> <p>Frequency Offset Enable globally disables FOS. See the individual FOS enables (FOSX_EN, register 139).</p> <p>0: FOS disable</p> <p>1: FOS enabled by FOSx_EN</p>
6:5	FOS_THR [1:0]	<p><b>FOS_THR [1:0].</b></p> <p>Frequency Offset at which FOS is declared (relative to the selected FOS reference):</p> <p>00: ± 11 to 12 ppm (Stratum 3/3E compliant, with a Stratum 3/3E used for REFCLK)</p> <p>01: ± 48 to 49 ppm (SMC)</p> <p>10: ± 30 ppm (SONET Minimum Clock (SMC), with a Stratum 3/3E used for REFCLK.</p> <p>11: ± 200 ppm</p>
4:3	VALTIME [1:0]	<p><b>VALTIME [1:0].</b></p> <p>Sets amount of time for input clock to be valid before the associated alarm is removed.</p> <p>00: 2 ms</p> <p>01: 100 ms</p> <p>10: 200 ms</p> <p>11: 13 seconds</p>
2:0	LOCKT [2:0]	<p><b>LOCKT [2:0].</b></p> <p>Sets retrigger interval for one shot monitoring phase detector output. One shot is triggered by phase slip in DSPLL. Refer to the Si53xx Family Reference Manual for more details.</p> <p>000: 106 ms</p> <p>001: 53 ms</p> <p>010: 26.5 ms</p> <p>011: 13.3 ms</p> <p>100: 6.6 ms</p> <p>101: 3.3 ms</p> <p>110: 1.66 ms</p> <p>111: .833 ms</p>



**Register 20.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved				CK2_BAD_PIN	CK1_BAD_PIN	LOL_PIN	INT_PIN
<b>Type</b>	R				R/W	R/W	R/W	R/W

Reset value = 0011 1110

Bit	Name	Function
7:4	Reserved	<b>Reserved.</b>
3	CK2_BAD_PIN	<b>CK2_BAD_PIN.</b> The CK2_BAD status can be reflected on the C2B output pin. 0: C2B output pin tristated 1: C2B status reflected to output pin
2	CK1_BAD_PIN	<b>CK1_BAD_PIN.</b> Either LOS1 or INT (see INT_PIN) status can be reflected on the INT_C1B output pin. 0: INT_C1B output pin tristated 1: LOS1 or INT (see INT_PIN) status reflected to output pin
1	LOL_PIN	<b>LOL_PIN.</b> The LOL_INT status bit can be reflected on the LOL output pin. 0: LOL output pin tristated 1: LOL_INT status reflected to output pin
0	INT_PIN	<b>INT_PIN.</b> Reflects the interrupt status on the INT_C1B output pin. 0: Interrupt status not displayed on INT_C1B output pin. Instead, the INT_C1B pin indicates when CKIN1 is bad. If CK1_BAD_PIN = 0, INT_C1B output pin is tristated. 1: Interrupt status reflected to output pin.

## Register 21.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved	Reserved					CK1_ACTV_PIN	CKSEL_PIN
<b>Type</b>	R	Force 1	R	R	R	R	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:2	Reserved	<b>Reserved.</b>
1	CK1_ACTV_PIN	<p><b>CK1_ACTV_PIN.</b></p> <p>The CK1_ACTV_REG status bit can be reflected to the CS_CA output pin using the CK1_ACTV_PIN enable function. CK1_ACTV_PIN is of consequence only when pin controlled clock selection is not being used. (See CKSEL_PIN)</p> <p>0: CS_CA output pin tristated. 1: Clock Active status reflected to output pin.</p>
0	CKSEL_PIN	<p><b>CKSEL_PIN.</b></p> <p>If manual clock selection is being used, clock selection can be controlled via the CKSEL_REG[1:0] register bits or the CS_CA input pin. This bit is only active when AUTOSEL_REG = Manual.</p> <p>0: CS_CA pin is ignored. CKSEL_REG[1:0] register bits control clock selection. 1: CS_CA input pin controls clock selection.</p>

**Register 22.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved				CK_ACTV_POL	CK_BAD_POL	LOL_POL	INT_POL
<b>Type</b>	R				R/W	R/W	R/W	R/W

Reset value = 1101 1111

Bit	Name	Function
7:4	Reserved	<b>Reserved.</b>
3	CK_ACTV_POL	<b>CK_ACTV_POL.</b> Sets the active polarity for the CS_CA signals when reflected on an output pin. 0: Active low 1: Active high
2	CK_BAD_POL	<b>CK_BAD_POL.</b> Sets the active polarity for the INT_C1B and C2B signals when reflected on output pins. 0: Active low 1: Active high
1	LOL_POL	<b>LOL_POL.</b> Sets the active polarity for the LOL status when reflected on an output pin. 0: Active low 1: Active high
0	INT_POL	<b>INT_POL.</b> Sets the active polarity for the interrupt status when reflected on the INT_C1B output pin. 0: Active low 1: Active high

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## Register 23.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					LOS2_MSK	LOS1_MSK	LOSX_MSK
Type	R					R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	<b>Reserved.</b>
2	LOS2_MSK	<b>LOS2_MSK.</b> Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register. 0: LOS2 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: LOS2_FLG ignored in generating interrupt output.
1	LOS1_MSK	<b>LOS1_MSK.</b> Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register. 0: LOS1 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: LOS1_FLG ignored in generating interrupt output.
0	LOSX_MSK	<b>LOSX_MSK.</b> Determines if a LOS on XA/XB(LOSX_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOSX_FLG register. 0: LOSX alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: LOSX_FLG ignored in generating interrupt output.

**Register 24.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved					FOS2_MSK	FOS1_MSK	LOL_MSK
<b>Type</b>	R					R/W	R/W	R/W

Reset value = 0011 1111

Bit	Name	Function
7:3	Reserved	<b>Reserved.</b>
2	FOS2_MSK	<b>FOS2_MSK.</b> Determines if the FOS2_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS2_FLG register. 0: FOS2 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: FOS2_FLG ignored in generating interrupt output.
1	FOS1_MSK	<b>FOS1_MSK.</b> Determines if the FOS1_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS1_FLG register. 0: FOS1 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: FOS1_FLG ignored in generating interrupt output.
0	LOL_MSK	<b>LOL_MSK.</b> Determines if the LOL_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the LOL_FLG register. 0: LOL alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: LOL_FLG ignored in generating interrupt output.

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## Register 25.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N1_HS [2:0]				Reserved			
<b>Type</b>	R/W				R			

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	<b>N1_HS [2:0].</b> Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 2) low-speed divider. 000: N1 = 4 001: N1 = 5 010: N1 = 6 011: N1 = 7 100: N1 = 8 101: N1 = 9 110: N1 = 10 111: N1 = 11
4:0	Reserved	<b>Reserved.</b>

## Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved				NC1_LS [19:16]			
<b>Type</b>	R				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	<b>Reserved.</b>
3:0	NC1_LS [19:16]	<b>NC1_LS [19:16].</b> Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2 <sup>20</sup> Valid divider values=[1, 2, 4, 6, ..., 2 <sup>20</sup> ]

**Register 32.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC1_LS [15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	<p><b>NC1_LS [15:8].</b> Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2<sup>20</sup> Valid divider values=[1, 2, 4, 6, ..., 2<sup>20</sup>]</p>

**Register 33.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC1_LS [7:0]							
<b>Type</b>	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [19:0]	<p><b>NC1_LS [7:0].</b> Sets value for N1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2<sup>20</sup> Valid divider values=[1, 2, 4, 6, ..., 2<sup>20</sup>]</p>

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## Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved				NC2_LS [19:16]			
<b>Type</b>	R				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	<b>Reserved.</b>
3:0	NC2_LS [19:16]	<b>NC2_LS [19:16].</b> Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000=1 00000000000000000001=2 00000000000000000011=4 00000000000000000101=6 ... 11111111111111111111=2 <sup>20</sup> Valid divider values=[1, 2, 4, 6, ..., 2 <sup>20</sup> ]

## Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC2_LS [15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC2_LS [15:8]	<b>NC2_LS [15:8].</b> Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2 <sup>20</sup> Valid divider values=[1, 2, 4, 6, ..., 2 <sup>20</sup> ]



**Register 36.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC2_LS [7:0]							
<b>Type</b>	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC2_LS [7:0]	<p><b>NC2_LS [7:0].</b></p> <p>Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd.</p> <p>00000000000000000000 = 1</p> <p>00000000000000000001 = 2</p> <p>00000000000000000011 = 4</p> <p>00000000000000000101 = 6</p> <p>...</p> <p>11111111111111111111 = <math>2^{20}</math></p> <p>Valid divider values = [1, 2, 4, 6, ..., <math>2^{20}</math>]</p>

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## Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N2_HS [2:0]			Reserved	N2_LS [19:16]			
<b>Type</b>	R/W			R	R/W			

Reset value = 1100 0000

Bit	Name	Function
7:5	N2_HS [2:0]	<b>N2_HS [2:0].</b> Sets value for N2 high speed divider, which drives N2LS low-speed divider. 000: 4 001: 5 010: 6 011: 7 100: 8 101: 9 110: 10 111: 11
4	Reserved	<b>Reserved.</b>
3:0	N2_LS [19:16]	<b>N2_LS [19:16].</b> Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = $2^{20}$ Valid divider values = [2, 4, 6, ..., $2^{20}$ ]

**Register 41.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N2_LS [15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	<p><b>N2_LS [15:8].</b>  Sets value for N2 low-speed divider, which drives phase detector.  00000000000000000001 = 2  00000000000000000011 = 4  00000000000000000101 = 6  ...  11111111111111111111 = <math>2^{20}</math>  Valid divider values = [2, 4, 6, ..., <math>2^{20}</math>]</p>

**Register 42.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N2_LS [7:0]							
<b>Type</b>	R/W							

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	<p><b>N2_LS [7:0].</b>  Sets value for N2 low-speed divider, which drives phase detector.  00000000000000000001 = 2  00000000000000000011 = 4  00000000000000000101 = 6  ...  11111111111111111111 = <math>2^{20}</math>  Valid divider values = [2, 4, 6, ..., <math>2^{20}</math>]</p>

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## Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					N31 [18:16]		
Type	R					R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	<b>Reserved.</b>
2:0	N31 [18:16]	<b>N31 [18:16].</b> Sets value for input divider for CKIN1. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values=[1, 2, 3, ..., $2^{19}$ ]

## Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N31_[15:8]	<b>N31_[15:8].</b> Sets value for input divider for CKIN1. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values=[1, 2, 3, ..., $2^{19}$ ]

**Register 45.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N31_[7:0]							
<b>Type</b>	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N31_[7:0]	<b>N31_[7:0].</b> Sets value for input divider for CKIN1. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values=[1, 2, 3, ..., $2^{19}$ ]

**Register 46.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved					N32_[18:16]		
<b>Type</b>	R					R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	<b>Reserved.</b>
2:0	N32_[18:16]	<b>N32_[18:16].</b> Sets value for input divider for CKIN2. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values=[1, 2, 3, ..., $2^{19}$ ]

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## Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N32_[15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N32_[15:8]	<b>N32_[15:8].</b> Sets value for input divider for CKIN2. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values=[1, 2, 3, ..., $2^{19}$ ]

## Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N32_[7:0]							
<b>Type</b>	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N32_[7:0]	<b>N32_[7:0].</b> Sets value for input divider for CKIN1. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values=[1, 2, 3, ..., $2^{19}$ ]

**Register 55.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved		CLKIN2RATE_[2:0]			CLKIN1RATE[2:0]		
<b>Type</b>	R		R/W			R/W		

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	<b>Reserved.</b>
5:3	CLKIN2RATE[2:0]	<b>CLKIN2RATE[2:0].</b> CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 010: 50–105 MHz 011: 95–215 MHz 100: 190–435 MHz 101: 375–710 MHz 110: Reserved 111: Reserved
2:0	CLKIN1RATE [2:0]	<b>CLKIN1RATE[2:0].</b> CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 010: 50–105 MHz 011: 95–215 MHz 100: 190–435 MHz 101: 375–710 MHz 110: Reserved 111: Reserved

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**Register 128.**

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Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						CK2_ACTV_REG	CK1_ACTV_REG
Type	R						R	R

Reset value = 0010 0000

Bit	Name	Function
7:2	Reserved	<b>Reserved.</b>
1	CK2_ACTV_REG	<b>CK2_ACTV_REG.</b> Indicates if CKIN2 is currently the active clock for the PLL input. 0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1. 1: CKIN2 is the active input clock.
0	CK1_ACTV_REG	<b>CK1_ACTV_REG.</b> Indicates if CKIN1 is currently the active clock for the PLL input. 0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1. 1: CKIN1 is the active input clock.



**Register 129.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved					LOS2_INT	LOS1_INT	LOSX_INT
<b>Type</b>	R					R	R	R

Reset value = 0000 0110

Bit	Name	Function
7:3	Reserved	<b>Reserved.</b>
2	LOS2_INT	<b>LOS2_INT.</b> Indicates the LOS status on CKIN2. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN2 input.
1	LOS1_INT	<b>LOS1_INT.</b> Indicates the LOS status on CKIN1. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN1 input.
0	LOSX_INT	<b>LOSX_INT.</b> Indicates the LOS status of the external reference on the XA/XB pins. 0: Normal operation. 1: Internal loss-of-signal alarm on XA/XB reference clock input.

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## Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	DIGHOLDVALID	Reserved			FOS2_INT	FOS1_INT	LOL_INT
Type	R	R	R			R	R	R

Reset value = 0000 0001

Bit	Name	Function
7	Reserved	<b>Reserved.</b>
6	DIGHOLDVALID	<b>Digital Hold Valid.</b> Indicates if the digital hold circuit has enough samples of a valid clock to meet digital hold specifications. 0: Indicates digital hold history registers have not been filled. The digital hold output frequency may not meet specifications. 1: Indicates digital hold history registers have been filled. The digital hold output frequency is valid.
5:3	Reserved	<b>Reserved.</b>
2	FOS2_INT	<b>CKIN2 Frequency Offset Status.</b> 0: Normal operation. 1: Internal frequency offset alarm on CKIN2 input.
1	FOS1_INT	<b>CKIN1 Frequency Offset Status.</b> 0: Normal operation. 1: Internal frequency offset alarm on CKIN1 input.
0	LOL_INT	<b>PLL Loss of Lock Status.</b> 0: PLL locked. 1: PLL unlocked.

**Register 131.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved					LOS2_FLG	LOS1_FLG	LOSX_FLG
<b>Type</b>	R					R/W	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	<b>Reserved.</b>
2	LOS2_FLG	<b>CKIN2 Loss-of-Signal Flag.</b> 0: Normal operation. 1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS2_MSK bit. Flag cleared by writing 0 to this bit.
1	LOS1_FLG	<b>CKIN1 Loss-of-Signal Flag.</b> 0: Normal operation 1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS1_MSK bit. Flag cleared by writing 0 to this bit.
0	LOSX_FLG	<b>External Reference (signal on pins XA/XB) Loss-of-Signal Flag.</b> 0: Normal operation 1: Held version of LOSX_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOSX_MSK bit. Flag cleared by writing 0 to this bit.

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## Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved				FOS2_FLG	FOS1_FLG	LOL_FLG	Reserved
<b>Type</b>	R				R/W	R/W	R/W	R

Reset value = 0000 0010

Bit	Name	Function
7:4	Reserved	<b>Reserved.</b>
3	FOS2_FLG	<b>CLKIN_2 Frequency Offset Flag.</b> 0: Normal operation. 1: Held version of FOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS2_MSK bit. Flag cleared by writing 0 to this bit.
2	FOS1_FLG	<b>CLKIN_1 Frequency Offset Flag.</b> 0: Normal operation 1: Held version of FOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS1_MSK bit. Flag cleared by writing 0 to this bit.
1	LOL_FLG	<b>PLL Loss of Lock Flag.</b> 0: PLL locked 1: Held version of LOL_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOL_MSK bit. Flag cleared by writing 0 to this bit.
0	Reserved	<b>Reserved.</b>

**Register 134.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	PARTNUM_RO [11:4]							
<b>Type</b>	R							

Reset value = 0000 0001

Bit	Name	Function
7:0	PARTNUM_RO [11:0]	<b>Device ID (1 of 2).</b> 0000 0001 1100: Si5328

**Register 135.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	PARTNUM_RO [3:0]				REVID_RO [3:0]			
<b>Type</b>	R				R			

Reset value = 1100 0010

Bit	Name	Function
7:4	PARTNUM_RO [11:0]	<b>Device ID (2 of 2).</b> 0000 0001 1100: Si5328
3:0	REVID_RO [3:0]	<b>Device Revision.</b> 0010: Revision C Others: Reserved

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## Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	RST_REG	ICAL	Reserved					
<b>Type</b>	R/W	R/W	R					

Reset value = 0000 0000

Bit	Name	Function
7	RST_REG	<p><b>Internal Reset (Same as Pin Reset).</b></p> <p><b>Note:</b> The I<sup>2</sup>C (or SPI) port may not be accessed until 10 ms after RST_REG is asserted.</p> <p>0: Normal operation. 1: Reset of all internal logic. Outputs disabled or tristated during reset.</p>
6	ICAL	<p><b>Start an Internal Calibration Sequence.</b></p> <p>For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a "1" to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low.</p> <p>0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, LOL will go low.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. A valid stable clock (within 100 ppm) must be present to begin ICAL.</li> <li>2. If the input changes by more than 500 ppm, the part may do an autonomous ICAL.</li> <li>3. See Table 10, "Register Locations Requiring ICAL," on page 62 for register changes that require an ICAL.</li> </ol>
5:0	Reserved	<b>Reserved.</b>

## Register 137.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>								FASTLOCK
<b>Type</b>	R	R	R	R	R	R	R	R/W

Reset value = 0000 0000

Bit	Name	Function
7:1	Reserved	Do not modify.
0	FASTLOCK	This bit must be set to 1 to enable FASTLOCK. This improves initial lock time by dynamically changing the loop bandwidth.

**Register 138.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved						LOS2_EN[1:1]	LOS1_EN [1:1]
<b>Type</b>	R						R/W	R/W

Reset value = 0000 1111

Bit	Name	Function
7:2	Reserved	<b>Reserved.</b>
1	LOS2_EN [1:0]	<p><b>Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).</b></p> <p><b>Note:</b> LOS2_EN is split between two registers.            00: Disable LOS monitoring            01: Reserved            10: Enable LOSA monitoring            11: Enable LOS monitoring            LOSA is a slower and less sensitive version of LOS. SEE the Si53xx Family Reference Manual for details.</p>
0	LOS1_EN [1:0]	<p><b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b></p> <p><b>Note:</b> LOS1_EN is split between two registers.            00: Disable LOS monitoring            01: Reserved            10: Enable LOSA monitoring            11: Enable LOS monitoring            LOSA is a slower and less sensitive version of LOS. See the Si53xx Family Reference Manual for details.</p>

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## Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	Reserved		LOS2_EN [0:0]	LOS1_EN [0:0]	Reserved		FOS2_EN	FOS1_EN
<b>Type</b>	R		R/W	R/W	R		R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:6	Reserved	<b>Reserved.</b>
5	LOS2_EN [1:0]	<p><b>Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).</b></p> <p><b>Note:</b> LOS2_EN is split between two registers.            00: Disable LOS monitoring            01: Reserved            10: Enable LOSA monitoring            11: Enable LOS monitoring            LOSA is a slower and less sensitive version of LOS. See the Si53xx Family Reference Manual for details</p>
4	LOS1_EN [1:0]	<p><b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b></p> <p><b>Note:</b> LOS1_EN is split between two registers.            00: Disable LOS monitoring            01: Reserved            10: Enable LOSA monitoring            11: Enable LOS monitoring            LOSA is a slower and less sensitive version of LOS. See the Si53xx Family Reference Manual for details.</p>
3:2	Reserved	<b>Reserved.</b>
1	FOS2_EN	<p><b>Enables FOS on a Per Channel Basis.</b></p> <p>0: Disable FOS monitoring            1: Enable FOS monitoring</p>
0	FOS1_EN	<p><b>Enables FOS on a Per Channel Basis.</b></p> <p>0: Disable FOS monitoring            1: Enable FOS monitoring</p>



**Register 142.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	INDEPENDENTSKEW1 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPEND-ENTSKEW1 [7:0]	<b>INDEPENDENTSKEW1.</b> Eight-bit field that represents a 2's complement of the phase offset in terms of clocks from the high speed output divider.

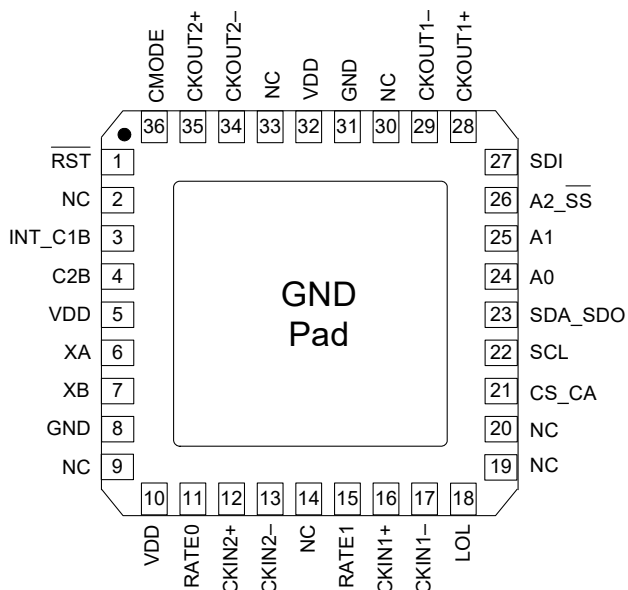
**Register 143.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	INDEPENDENTSKEW2 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPEND-ENTSKEW2 [7:0]	<b>INDEPENDENTSKEW2.</b> Eight-bit field that represents a 2's complement of the phase offset in terms of clocks from the high speed output divider.

## 7. Pin Descriptions: Si5328



Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{RST}$	I	LVC MOS	<b>External Reset.</b> Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. The part must be programmed after a reset or power on to get a clock output. See the Si53xx Family Reference Manual for details. This pin has a weak pull-up.
2, 9, 14, 19, 20, 30, 33	NC	—	—	<b>No Connection.</b> Leave floating. Make no external connections to this pin for normal operation.
3	INT_C1B	O	LVC MOS	<b>Interrupt/CKIN1 Invalid Indicator.</b> This pin functions as a device interrupt output or an alarm output for CKIN1. If used as an interrupt output, <i>INT_PIN</i> must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the <i>INT_POL</i> register bit. If used as an alarm output, the pin functions as a LOS (and optionally FOS) alarm indicator for CKIN1. Set <i>CK1_BAD_PIN</i> = 1 and <i>INT_PIN</i> = 0. 0 = CKIN1 present 1 = LOS (FOS) on CKIN1 The active polarity is controlled by <i>CK_BAD_POL</i> . If no function is selected, the pin tristates.
<b>Note:</b> Internal register names are indicated by underlined italics, e.g., <i>INT_PIN</i> . See Section "5. Register Map".				

Pin #	Pin Name	I/O	Signal Level	Description
4	C2B	O	LVC MOS	<p><b>CKIN2 Invalid Indicator.</b></p> <p>This pin functions as a LOS (and optionally FOS) alarm indicator for CKIN2 if <math>CK2\_BAD\_PIN = 1</math>.</p> <p>0 = CKIN2 present 1 = LOS (FOS) on CKIN2</p> <p>The active polarity can be changed by <math>CK\_BAD\_POL</math>. If <math>CK2\_BAD\_PIN = 0</math>, the pin tristates.</p>
5, 10, 32	V <sub>DD</sub>	V <sub>DD</sub>	Supply	<p><b>Supply.</b></p> <p>The device operates from a 2.5 or 3.3 V supply. Bypass capacitors should be associated with the following V<sub>DD</sub> pins:</p> <p>5      0.1 μF 10     0.1 μF 32     0.1 μF</p> <p>A 1.0 μF should also be placed as close to the device as is practical.</p>
7 6	XB XA	I	Analog	<p><b>Reference Clock.</b></p> <p>A TCXO or OCXO should be connected to these pins. Refer to the Si53xx Family Reference Manual for interfacing to the external reference. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by RATE[1:0] pins.</p>
8, 31	GND	GND	Supply	<p><b>Ground.</b></p> <p>Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device. Grounding these pins does not eliminate the requirement to ground the GND PAD on the bottom of the package.</p>
11 15	RATE0 RATE1	I	3-Level	<p><b>Reference Clock Rate.</b></p> <p>Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Si53xx Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down; they default to M.</p> <p>L setting corresponds to ground. M setting corresponds to V<sub>DD</sub>/2. H setting corresponds to V<sub>DD</sub>.</p> <p>Some designs may require an external resistor voltage divider when driven by an active device that will tristate.</p>
16 17	CKIN1+ CKIN1-	I	Multi	<p><b>Clock Input 1.</b></p> <p>Differential input clock. This input can also be driven with a single-ended signal.</p>
12 13	CKIN2+ CKIN2-	I	Multi	<p><b>Clock Input 2.</b></p> <p>Differential input clock. This input can also be driven with a single-ended signal.</p>
<p><b>Note:</b> Internal register names are indicated by underlined italics, e.g., <i>INT_PIN</i>. See Section "5.Register Map".</p>				

Pin #	Pin Name	I/O	Signal Level	Description
18	LOL	O	LVC MOS	<p><b>PLL Loss of Lock Indicator.</b></p> <p>This pin functions as the active high PLL loss of lock indicator if the <u>LOL_PIN</u> register bit is set to 1.</p> <p>0 = PLL locked 1 = PLL unlocked</p> <p>If <u>LOL_PIN</u> = 0, this pin will tristate. Active polarity is controlled by the <u>LOL_POL</u> bit. The PLL lock status will always be reflected in the <u>LOL_INT</u> read only register bit.</p>
21	CS_CA	I/O	LVC MOS	<p><b>Input Clock Select/Active Clock Indicator.</b></p> <p><b>Input:</b> In manual clock selection mode, this pin functions as the manual input clock selector if the <u>CKSEL_PIN</u> is set to 1.</p> <p>0 = Select CKIN1 1 = Select CKIN2</p> <p>If <u>CKSEL_PIN</u> = 0, the <u>CKSEL_REG</u> register bit controls this function and this input tristates. If configured for input, must be tied high or low.</p> <p><b>Output:</b> In automatic clock selection mode, this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both clocks, <u>CK_ACTV</u> will indicate the last active clock that was used before entering the digital hold state. The <u>CK_ACTV_PIN</u> register bit must be set to 1 to reflect the active clock status to the <u>CK_ACTV</u> output pin.</p> <p>0 = CKIN1 active input clock 1 = CKIN2 active input clock</p> <p>If <u>CK_ACTV_PIN</u> = 0, this pin will tristate. The <u>CK_ACTV</u> status will always be reflected in the <u>CK_ACTV_REG</u> read only register bit.</p>
22	SCL	I	LVC MOS	<p><b>Serial Clock.</b></p> <p>This pin functions as the serial clock input for both SPI and I<sup>2</sup>C modes.</p> <p>This pin has a weak pull-down.</p>
23	SDA_SDO	I/O	LVC MOS	<p><b>Serial Data.</b></p> <p>In I<sup>2</sup>C control mode (CMODE = 0), this pin functions as the bidirectional serial data port.</p> <p>In SPI control mode (CMODE = 1), this pin functions as the serial data output.</p>
25 24	A1 A0	I	LVC MOS	<p><b>Serial Port Address.</b></p> <p>In I<sup>2</sup>C control mode (CMODE = 0), these pins function as hardware controlled address bits. The I<sup>2</sup>C address is 1101 [A2] [A1] [A0].</p> <p>In SPI control mode (CMODE = 1), these pins are ignored.</p> <p>These pins have a weak pull-down.</p>
<p><b>Note:</b> Internal register names are indicated by underlined italics, e.g., <u>INT_PIN</u>. See Section “5.Register Map”.</p>				

Pin #	Pin Name	I/O	Signal Level	Description
26	<u>A2_SS</u>	I	LVC MOS	<b>Serial Port Address/Slave Select.</b> In I <sup>2</sup> C control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2]. In SPI control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pull-down.
27	SDI	I	LVC MOS	<b>Serial Data In.</b> In I <sup>2</sup> C control mode (CMODE = 0), this pin is ignored. In SPI control mode (CMODE = 1), this pin functions as the serial data input. This pin has a weak pull-down.
29 28	CKOUT1– CKOUT1+	O	Multi	<b>Output Clock 1.</b> Differential output clock with a frequency range of 8 kHz to 808 MHz. Output signal format is selected by <i>SFOUT1_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
34 35	CKOUT2– CKOUT2+	O	Multi	<b>Output Clock 2.</b> Differential output clock with a frequency range of 8 kHz to 808 MHz. Output signal format is selected by <i>SFOUT2_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
36	CMODE	I	LVC MOS	<b>Control Mode.</b> Selects I <sup>2</sup> C or SPI control mode. 0 = I <sup>2</sup> C Control Mode 1 = SPI Control Mode This pin must not be NC. Tie either high or low. See the Si53xx Family Reference Manual for details on I <sup>2</sup> C or SPI operation.
GND PAD	GND	GND	Supply	<b>Ground Pad.</b> The ground pad must provide a low thermal and electrical impedance to a ground plane.
<b>Note:</b> Internal register names are indicated by underlined italics, e.g., <i>INT_PIN</i> . See Section “5.Register Map”.				

Table 10 lists all of the register locations that should be followed by an ICAL after their contents are changed.

**Table 10. Register Locations Requiring ICAL**

Addr	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
1	CK_PRIOR2
1	CK_PRIOR1
2	BWSEL_REG
4	HIST_DEL
5	ICMOS
7	FOSREFSEL
9	HIST_AVG
10	DSBL2_REG
10	DSBL1_REG
11	PD_CK2
11	PD_CK1
19	FOS_EN
19	FOS_THR
19	VALTIME
19	LOCKT
25	N1_HS
31	NC1_LS
34	NC2_LS
40	N2_HS
40	N2_LS
43	N31
46	N32
55	CLKIN2RATE
55	CLKIN1RATE

**Table 11. Si5328 Pull up/Pull down**

Pin #	Si5328	Pull up/Pull down
1	RST	U
11	RATE0	U, D
15	RATE1	U, D
21	CS_CA	U, D
22	SCL	D
24	A0	D
25	A1	D
26	A2_SS	D
27	SDI	D
36	CMODE	U, D

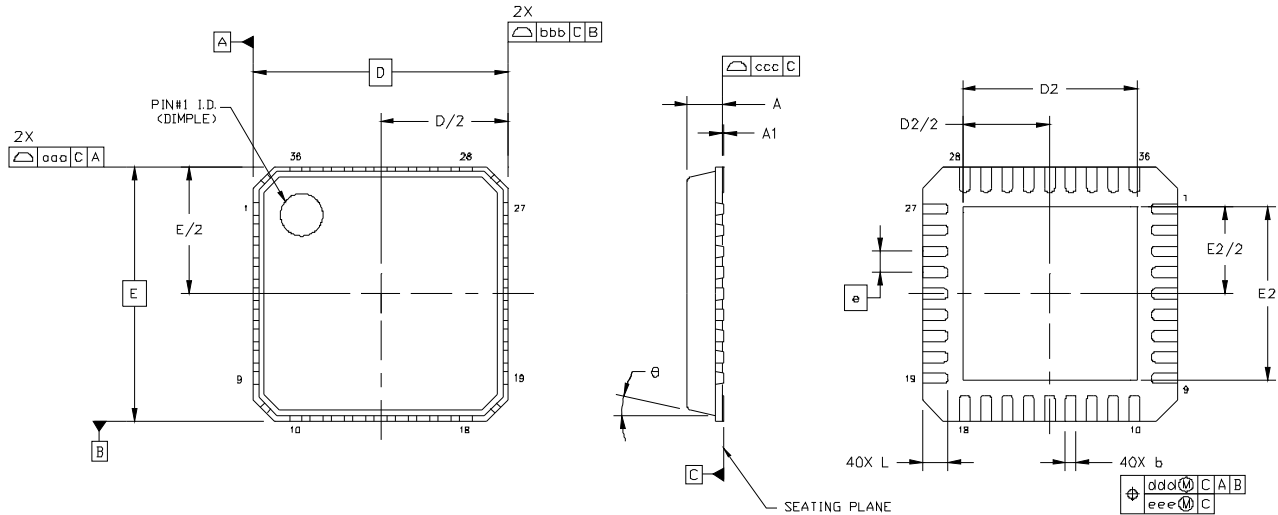
## 8. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	ROHS6, Pb-Free	Temperature Range
Si5328B-C-GM	8 kHz–808 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5328C-C-GM	8 kHz–346 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5328-EVB	8 kHz–808 MHz	Evaluation Board	—	–40 to 85 °C

**Note:** Add an R at the end of the device to denote tape and reel options.

## 9. Package Outline: 36-Pin QFN

Figure 7 illustrates the package details for the Si5328. Table 12 lists the values for the dimensions shown in the illustration.



**Figure 7. 36-Pin Quad Flat No-lead (QFN)**

**Table 12. Package Dimensions**

Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.80	0.85	0.90	L	0.50	0.60	0.70
A1	0.00	0.02	0.05	$\theta$	—	—	12°
b	0.18	0.25	0.30	aaa	—	—	0.10
D	6.00 BSC			bbb	—	—	0.10
D2	3.95	4.10	4.25	ccc	—	—	0.08
e	0.50 BSC			ddd	—	—	0.10
E	6.00 BSC			eee	—	—	0.05
E2	3.95	4.10	4.25				

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



## 10. Recommended PCB Layout

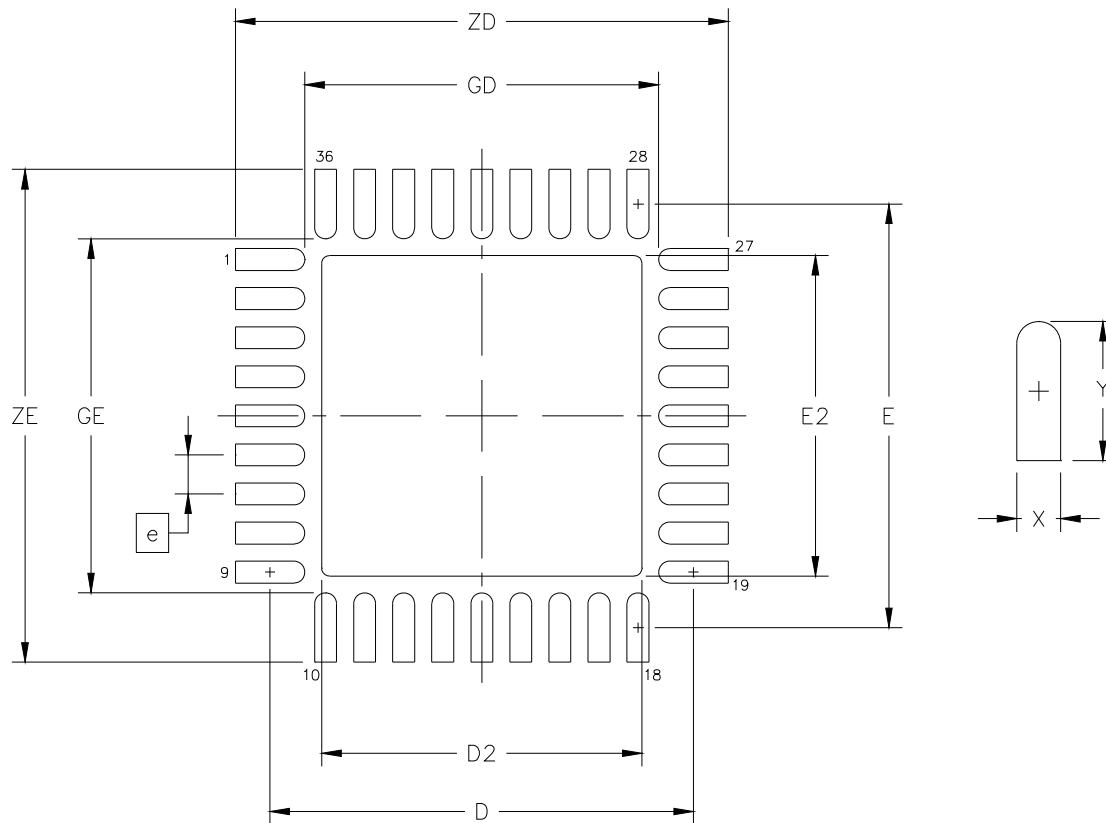


Figure 8. PCB Land Pattern Diagram

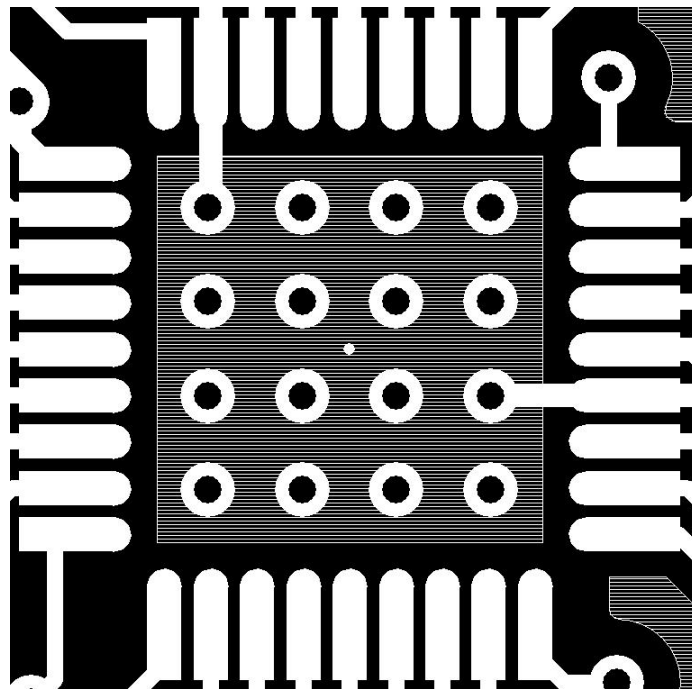


Figure 9. Ground Pad Recommended Layout

Table 13. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

**Notes:****General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.

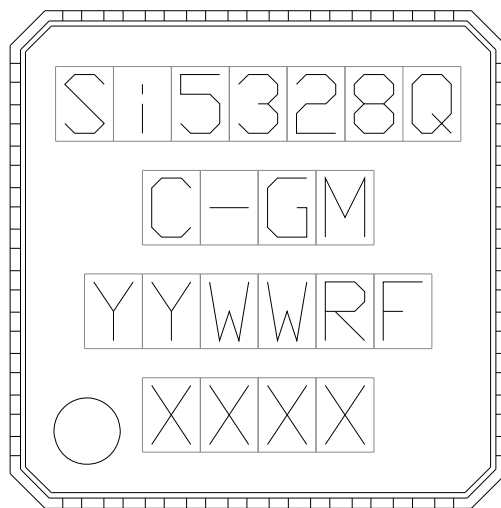
**Stencil Design**

6. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

**Card Assembly**

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 11. Si5328 Device Top Mark



<b>Mark Method:</b>	Laser	
<b>Font Size:</b>	0.80 mm Right-Justified	
<b>Line 1 Marking:</b>	Si5328Q	Customer Part Number Q = Speed Code: C See "8.Ordering Guide" for options
<b>Line 2 Marking:</b>	C-GM	C = Product Revision G = Temperature Range -40 to 85 °C (RoHS6) M = QFN Package
<b>Line 3 Marking:</b>	YYWWRF	YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
<b>Line 4 Marking:</b>	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	XXXX	Internal Code

## DOCUMENT CHANGE LIST

### Revision 0.9 to Revision 1.0

- Removed Vdd of 1.8 V.
- Updated lock and settling time specs.
- Added B speed grade with 808 MHz output frequency.

**NOTES:**



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