Si5341/40

LOW-JITTER, 10-OUTPUT, ANY-FREQUENCY, ANY-OUTPUT CLOCK GENERATOR

Features

- Generates free-running or synchronous output clocks
- MultiSynth™ technology enables any-frequency synthesis on any-output with 0 ppm frequency accuracy with respect to the input
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, HCSL, or programmable voltage swing and common mode
- Excellent jitter: <100 fs RMS typ
- Input frequency range:
  - External crystal: 25, 48-54 MHz
  - Differential clock: 10 to 750 MHz
  - LVCMOS clock: 10 to 250 MHz
- Output frequency range:
  - Differential: 100 Hz to 800 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Output-output skew: <100 ps
- Adjustable output-output delay
- Optional zero delay mode
- Independent glitchless on-the-fly output frequency changes
- DCO mode with frequency increment and decrement as low as 0.001 ppb/step
- Core voltage:
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output supply pins: 3.3V, 2.5V, or 1.8V
- Built-in power supply filtering
- Status monitoring: LOS, LOL
- Serial Interface: I^2C or SPI (3-wire or 4-wire)
- In-circuit programmable with non-volatile OTP memory (2x programmable)
- ClockBuilder Pro™ software utility simplifies device configuration and assigns customer part numbers
- **Si5341**: 4 input, 10 output, 64 QFN
- **Si5340**: 4 input, 4 output, 44 QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

Applications

- Clock tree generation replacing XOs, buffers, signal format translators
- Any-frequency synchronous clock translation
- Clocking for FPGAs, processors, memory
- Ethernet switches/routers
- OTN framers/mappers/processors
- Test equipment & instrumentation
- Broadcast video

Description

The any-frequency, any-output Si5341/40 clock generators combine a wide-band PLL with proprietary MultiSynth fractional synthesizer technology to offer a versatile and high performance clock generator platform. This highly flexible architecture is capable of synthesizing a wide range of integer and non-integer related frequencies up to 800 MHz on 10 differential clock outputs while delivering sub-100 fs rms phase jitter performance and 0 ppm error. Each of the clock outputs can be assigned its own format and output voltage enabling the Si5341/40 to replace multiple clock ICs and oscillators with a single device making it a true “clock tree in a chip”.

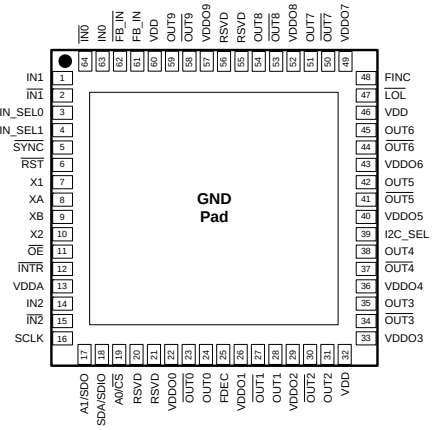
The Si5341/40 can be quickly and easily configured using ClockBuilder Pro software. Custom part numbers are automatically assigned using a ClockBuilderPro for fast, free, and easy factory programming, or the Si5341/40 can be programmed in-circuit via I^2C and SPI serial interface.

Ordering Information:

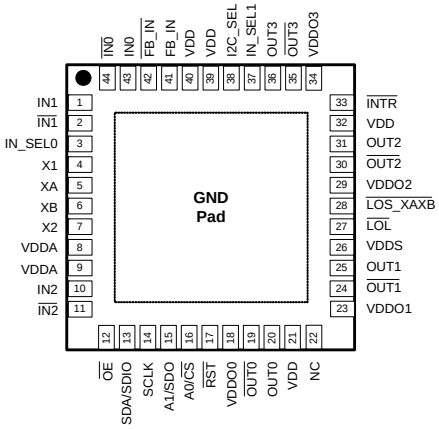
See section 7

Pin Assignments

Si5341 64QFN
Top View



Si5340 44QFN
Top View



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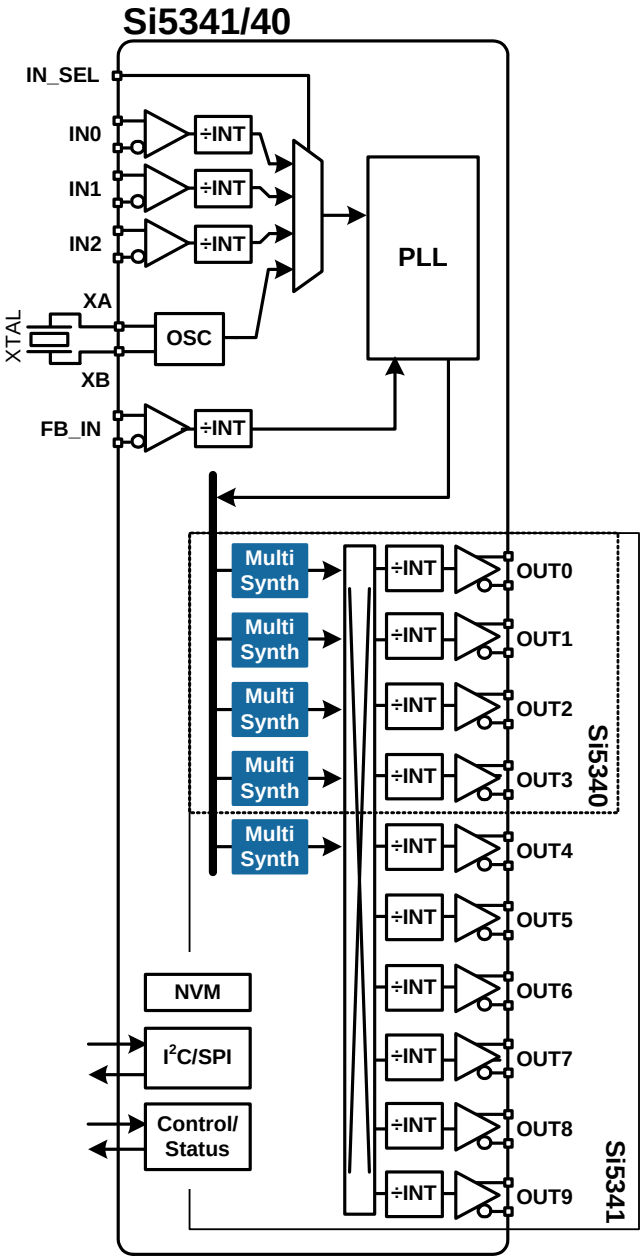
This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

Functional Block Diagram



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1. Typical Application Schematic

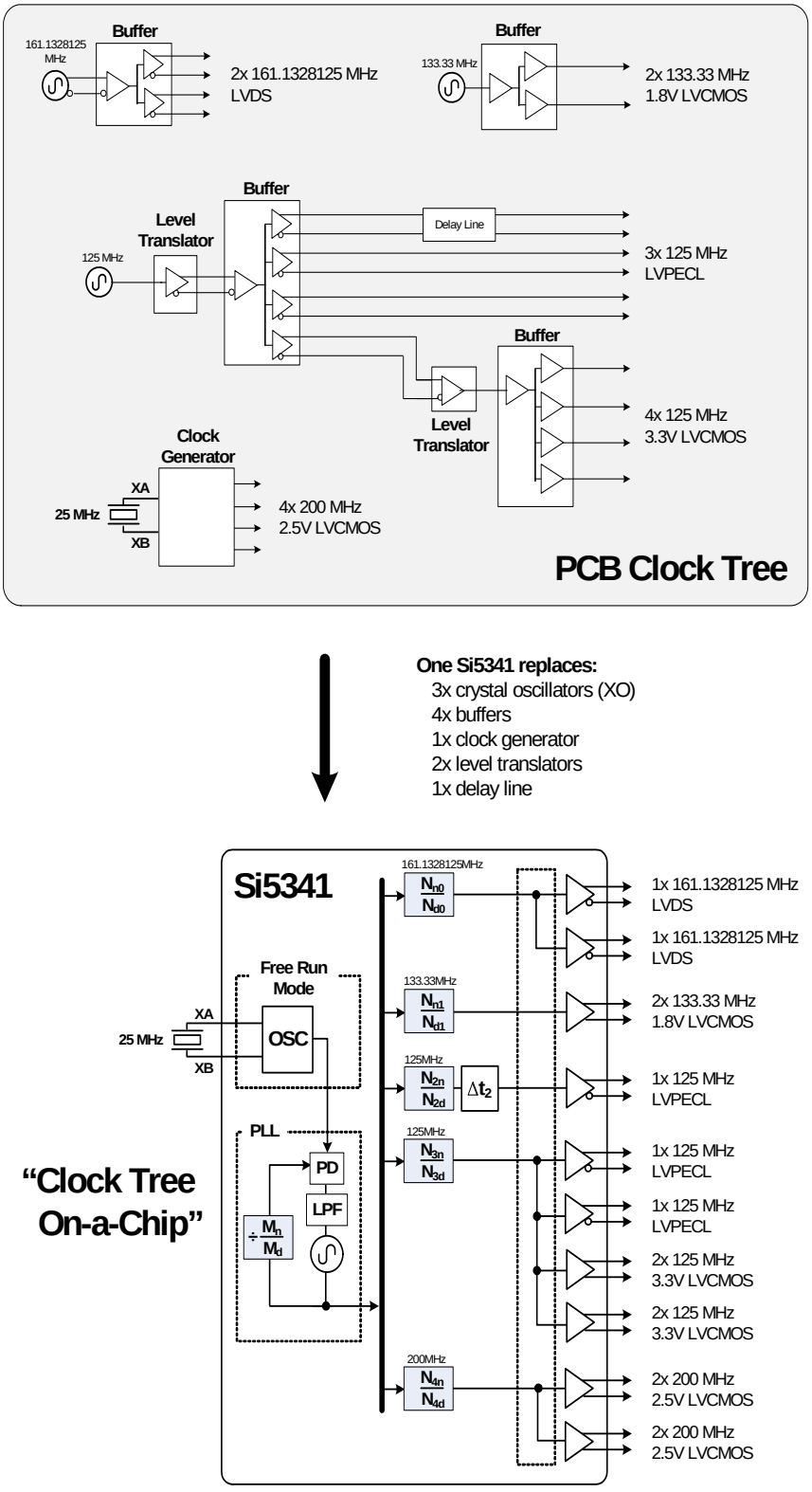


Figure 1. Using The Si5341 to Replace a Discrete Clock Tree

2. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V
***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.					

Table 2. DC Characteristics

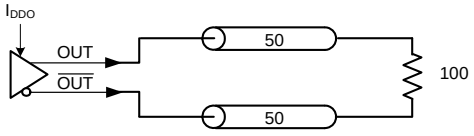
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core Supply Current	I_{DD}	Si5341 or Si5340	Notes [1,2]	—	98	140	mA
	I_{DDA}			—	115	125	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[3] @ 156.25 MHz		—	23	25	mA
		LVDS Output[3] @ 156.25 MHz		—	16	18	mA
		3.3V LVCMOS[4] output @ 156.25 MHz		—	19	26	mA
		2.5 V LVCMOS[4] output @ 156.25 MHz		—	15	19	mA
		1.8 V LVCMOS[4] output @ 156.25 MHz		—	11	13	mA
Total Power Dissipation	P_d	Si5341	Notes [1,5]	—	836	945	mW
		Si5340	Notes [2,5]	—	645	—	mW

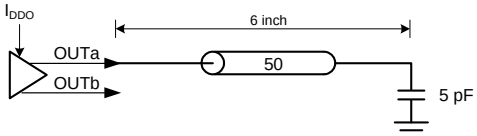
Notes:

1. Si5341 test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5340 test configuration: 4 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 6 inch 50 Ω PCB trace with 5 pF load.

Differential Output Test Configuration



LVCMOS Output Test Configuration



5. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 3. Input Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential or Single-Ended - AC Coupled (IN0/$\overline{IN0}$, IN1/$\overline{IN1}$, IN2/$\overline{IN2}$, FB_IN/$\overline{FB\_IN}$)						
Input Frequency Range	f_{IN_DIFF}		10	—	750	MHz
Voltage Swing	V_{IN}	f_{in} < 400 MHz	100	—	1000	mVpp_se
		600 MHz < f_{in} < 800 MHz	225	—	1000	mVpp_se
		f_{in} > 800 MHz	375	—	1000	mVpp_se
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
LVCMOS - DC Coupled (IN0, IN1, IN2)						
Input Frequency	f_{IN_CMOS}		10	—	250	MHz
Input Voltage	V_{IL}		-0.1	—	0.33	V
	V_{IH}		0.80	—	—	V
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC	Clock Input	40	—	60	%
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (Applied to XA/XB)						
REFCLK Frequency	f_{IN_REF}	Frequency range for best output jitter performance	48	—	54	MHz
			10	—	120	MHz
Input Voltage Swing	V_{IN}		350	—	1600	mVpp_se
Slew rate[1, 2]	SR	Imposed for best jitter performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Notes:

1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) * V_{IN\_Vpp\_se}) / SR$.
3. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.

Table 4. Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5341 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{\text{RST}}$, $\overline{\text{OE}}$, $\overline{\text{SYNC}}$, A1, SCLK, A0/$\overline{\text{CS}}$, FINC, FDEC)						
Input Voltage	V_{IL}		-0.1	—	$0.3xV_{DDIO}$*	V
	V_{IH}		$0.7xV_{DDIO}$[1]	—	3.6	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RST	50	—	—	ns
Si5340 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{\text{RST}}$, $\overline{\text{OE}}$, A1, SDA, SDI, SCLK, A0/$\overline{\text{CS}}$)						
Input Voltage	V_{IL}		–0.1	—	$0.3xV_{DDIO}$*	V
	V_{IH}		$0.7xV_{DDIO}$*	—	3.6	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RST	50	—	—	ns

***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.

Table 5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Frequency	f_{OUT}		0.0001	—	800	MHz
Duty Cycle	DC	f < 400 MHz	48	—	52	%
		400 MHz < f < 800 MHz	45	—	55	%
Output-Output Skew	T_{SK}	Differential Output	—	—	100	ps
OUT-$\overline{\text{OUT}}$ Skew	T_{SK_OUT}	Measured from the positive to negative output pins	—	—	100	ps

Notes:

1. Normal swing mode, high swing mode, Vswing and Cmode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently.
2. Not all combinations of voltage swing and common mode voltages settings are possible.
3. Common mode voltage min/max variation = ±4% from typical value
4. Driver output impedance depends on selected output mode (Normal, High).
5. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.

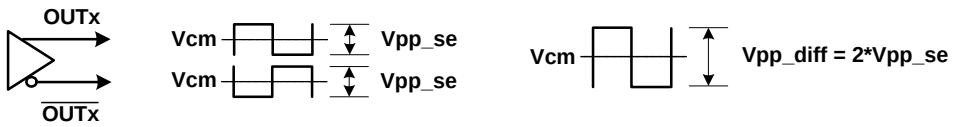


Table 5. Differential Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Voltage Swing[1]	Normal Swing Mode						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	370	470	570	mVpp_se
			LVPECL	650	820	1050	
	High Swing Mode						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	310	420	530	mVpp_se
		V_{DDO} = 3.3 V or 2.5 V	LVPECL	590	830	1060	
Common Mode Voltage[1, 2, 3]	Normal Swing or High Swing Modes						
	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.12	1.23	1.34	V
			LVPECL	1.90	2.0	2.13	
		V_{DDO} = 2.5 V	LVPECL LVDS	1.17	1.23	1.3	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Swing Mode		—	170	220	ps
		High Swing Mode		—	250	320	
Differential Output Impedance[4]	Z_O	Normal Swing Mode		—	100	—	Ω
		High Swing Mode		—	Hi-Z	—	Ω

Notes:

1. Normal swing mode, high swing mode, Vswing and Cmode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently.
2. Not all combinations of voltage swing and common mode voltages settings are possible.
3. Common mode voltage min/max variation = ±4% from typical value
4. Driver output impedance depends on selected output mode (Normal, High).
5. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.

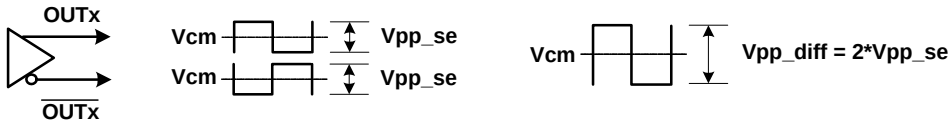


Table 5. Differential Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Supply Noise Rejection[5]	PSRR	Normal Swing Mode				
		10 kHz sinusoidal noise	—	–93	—	dBc
		100 kHz sinusoidal noise	—	–93	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–79	—	
		High Swing Mode				
		10 kHz sinusoidal noise	—	–98	—	dBc
		100 kHz sinusoidal noise	—	–95	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–76	—	
Output-output Crosstalk	XTALK	Measured spur from adjacent output	—	–73	—	dBc

Notes:
1. Normal swing mode, high swing mode, Vswing and Cmode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently.
2. Not all combinations of voltage swing and common mode voltages settings are possible.
3. Common mode voltage min/max variation = ±4% from typical value
4. Driver output impedance depends on selected output mode (Normal, High).
5. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.

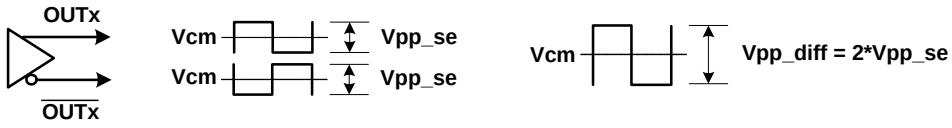


Table 6. Output Status Pin Specifications
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5341 Status Output Pins ($\overline{\text{LOL}}$, $\overline{\text{INTR}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[1] x 0.15	V
Si5340 Status Output Pins ($\overline{\text{INTR}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[1] x 0.15	V
Si5340 Status Output Pins ($\overline{\text{LOL}}$, $\overline{\text{LOS\_XAXB}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V
***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.						

Table 7. LVCMOS Clock Output Specifications

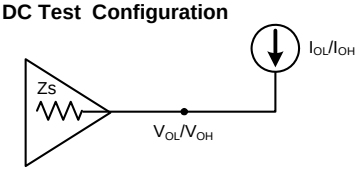
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency				0.0001	—	250	MHz
Duty Cycle	DC	f < 400 MHz		47	—	53	%
		400 MHz < f < 800 MHz		45	—	55	
Output-to-Output Skew	T_{SK}			—	—	100	ps
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		CMOS1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		CMOS2	I_{OH} = –12 mA		—	—	
		CMOS3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		CMOS1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		CMOS2	I_{OH} = –8 mA		—	—	
		CMOS3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		CMOS1	I_{OH} = –3 mA	V_{DDO} x 0.85	—	—	V
		CMOS2	I_{OH} = –4 mA		—	—	
		CMOS3	I_{OH} = –5 mA		—	—	

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are CMOS1, CMOS2, CMOS3.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ohm PCB trace. A 5 pF capacitive load is assumed.

DC Test Configuration



AC Test Configuration

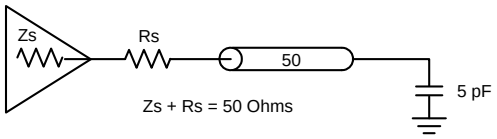
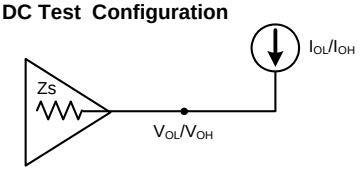


Table 7. LVCMOS Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		CMOS1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		CMOS2	I_{OL} = 12 mA	—	—		
		CMOS3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		CMOS1	I_{OH} = -6 mA	—	—	V_{DDO} x 0.15	V
		CMOS2	I_{OL} = 8 mA	—	—		
		CMOS3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		CMOS1	I_{OH} = –3 mA	—	—	V_{DDO} x 0.15	V
		CMOS2	I_{OH} = –4 mA	—	—		
		CMOS3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3V		—	360	—	ps
		VDDO = 2.5 V		—	420	—	ps
		VDDO = 1.8 V		—	280	—	ps

Notes:
1. Driver strength is a register programmable setting and stored in NVM. Options are CMOS1, CMOS2, CMOS3.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ohm PCB trace. A 5 pF capacitive load is assumed.

DC Test Configuration



AC Test Configuration

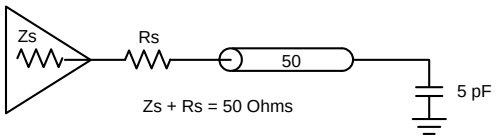


Table 8. Performance Characteristics
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PLL Loop Bandwidth	f_{BW}		—	1.0	—	MHz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	—	ms
POR[1] to Serial Interface Ready	t_{RDY}		—	—	10	ms
PLL Lock Time	t_{ACQ}		—	—	120	ms
Output delay adjustment	t_{DELAY}	f_{VCO} = 14 GHz Delay is controlled by the Multi-Synth	—	0.28	—	ps
	t_{RANGE}		—	±9.14	—	ns
Jitter Generation Locked to External Clock[1]	J_{RMS}	Integer Mode[2] 12 kHz to 20 MHz	—	0.115	0.200	ps RMS
		Fractional/DCO Mode[3] 12 kHz to 20 MHz	—	0.170	0.400	ps RMS
	J_{PER}	Derived from integrated phase noise	—	0.140	—	ps pk-pk
	J_{CC}		—	0.250	—	ps pk
	J_{PER}	N = 10,000 cycles Integer or Fractional Mode[2,3]. Measured in the time domain. Performance is limited by the noise floor of the equipment.	—	7.3	—	ps pk-pk
	J_{CC}		—	8.1	—	ps pk
Jitter Generation Locked to External XTAL	XTAL Frequency = 48 MHz to 54 MHz					
	J_{RMS}	Integer Mode[2] 12 kHz to 20 MHz	—	0.100	0.160	ps RMS
		Fractional/DCO Mode[3] 12 kHz to 20 MHz	—	0.140	0.350	ps RMS
	J_{PER}	Derived from integrated phase noise	—	0.150	—	ps pk-pk
	J_{CC}		—	0.270	—	ps pk
	J_{PER}	N = 10, 000 cycles Integer or Fractional Mode[2,3] . Measured in the time domain. Performance is limited by the noise floor of the equipment.	—	7.3	—	ps pk-pk
	J_{CC}		—	7.8	—	ps pk

Notes:
1. Jitter generation test conditions in synchronous mode: f_{IN} = 100 MHz, f_{OUT} = 156.25 MHz LVPECL. Does not include jitter from PLL input reference.
2. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value.
3. Fractional and DCO modes assumes that the output dividers (Nn/Nd) are configured with a fractional value.

Table 9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Units
			Standard Mode 100 kbps		Fast Mode 400 kbps		
SCL Clock Frequency	f_{SCL}		0	100	0	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		5.0	—	—	—	µs
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

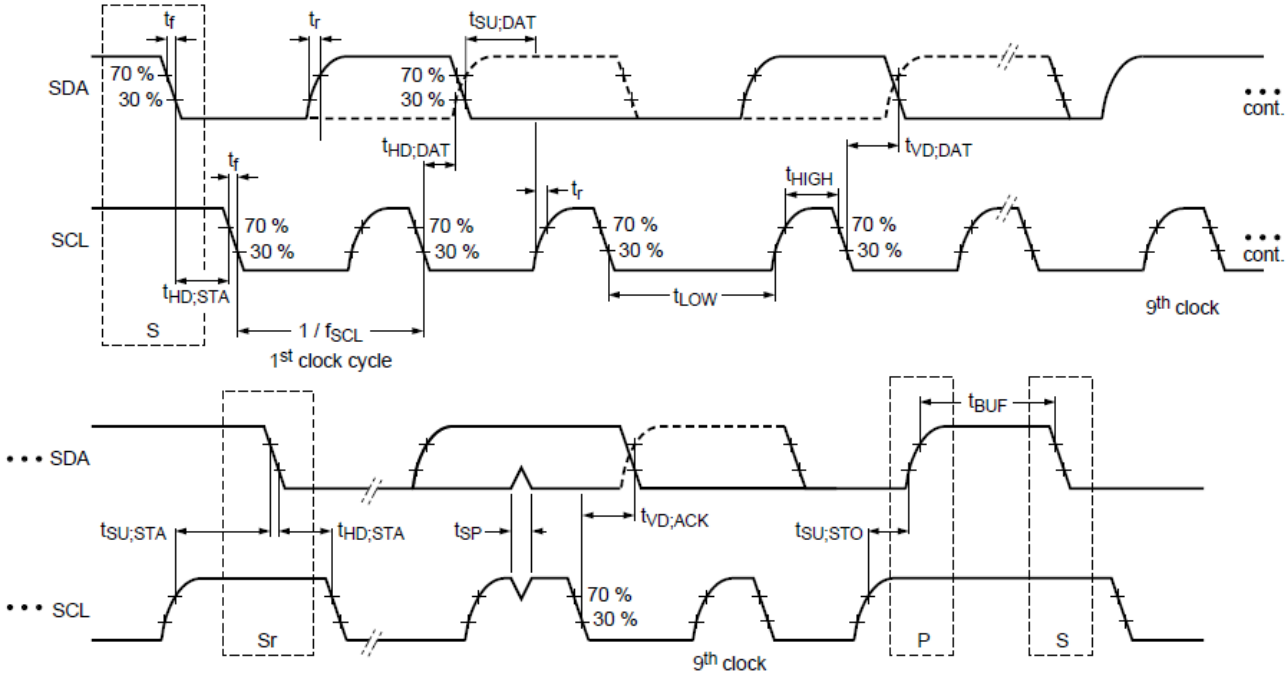


Figure 2. I²C Serial Port Timing Standard and Fast Modes

Table 10. SPI Timing Specifications
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Rise & Fall Time	Tr/Tf	—	—	10	ns
SCLK High & Low Time	T_{HL}				
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	12.5	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	12.5	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-State	T_{D3}	—	—	12.5	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	25	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Rise	T_{H1}	25	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	12.5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	12.5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	50	—	—	ns

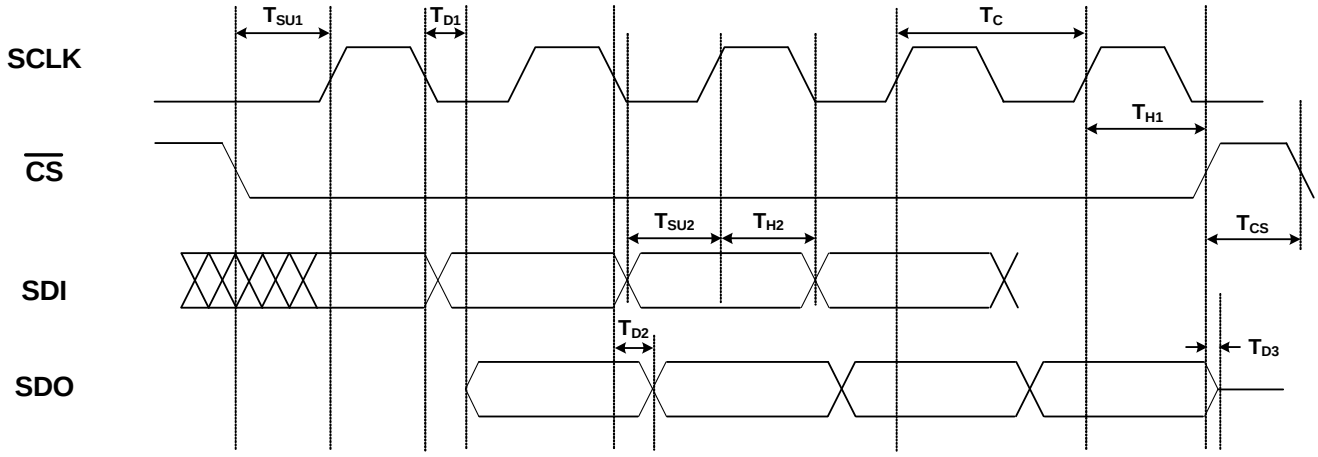


Figure 3. SPI Serial Interface Timing

Table 11. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency Range	$f_{XTAL\_48\text{-}54}$	Frequency range for best jitter performance	48	—	54	MHz
Load Capacitance	$C_{L\_48\text{-}54}$		—	8	—	pF
Shunt Capacitance	$C_{O\_48\text{-}54}$		—	—	2	pF
Crystal Drive Level	$d_{L\_48\text{-}54}$		—	—	200	µW
Equivalent Series Resistance	$r_{ESR\_48\text{-}54}$	Refer to the Si5341/40 Family Reference Manual to determine ESR.				
Crystal Frequency Range	f_{XTAL_25}		—	25	—	MHz
Load Capacitance	C_{L_25}		—	8	—	pF
Shunt Capacitance	C_{O_25}		—	—	3	pF
Crystal Drive Level	d_{L_25}		—	—	200	µW
Equivalent Series Resistance	r_{ESR_25}	Refer to the Si5341/40 Family Reference Manual to determine ESR				

Notes:
1. The Si5341/40 is designed to work with crystals that meet the specifications in Table 11.
2. Refer to the Si5341/40 Family Reference Manual for recommended 48 to 54 MHz crystals. Crystal frequencies from 24.97 to 54.06 MHz are supported, but jitter performance is best from 48 to 54 MHz.

Table 12. Thermal Characteristics

Parameter	Symbol	Test Condition*	Value	Units
Si5341 - 64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	
Si5340–44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	

***Note:** Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GND pad: 36, Number of Cu Layers: 4

Table 13. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0-IN2, FB_IN	-0.85 to 3.8	V
	V_{I2}	IN_SEL[1:0], $\overline{RST}$, $\overline{OE}$, $\overline{SYNC}$, I2C_SEL, SDI, SCLK, A0/$\overline{CS}$ A1, SDA/SDIO FINC/FDEC	-0.5 to 3.8	V
	V_{I3}	XA/XB	-0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Junction Temperature	T_{JCT}		-55 to 150	°C
Soldering Temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[5]	T_P		20-40	sec

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. Moisture sensitivity level is MSL2.
5. The device is compliant with JEDEC J-STD-020.

3. Detailed Block Diagrams

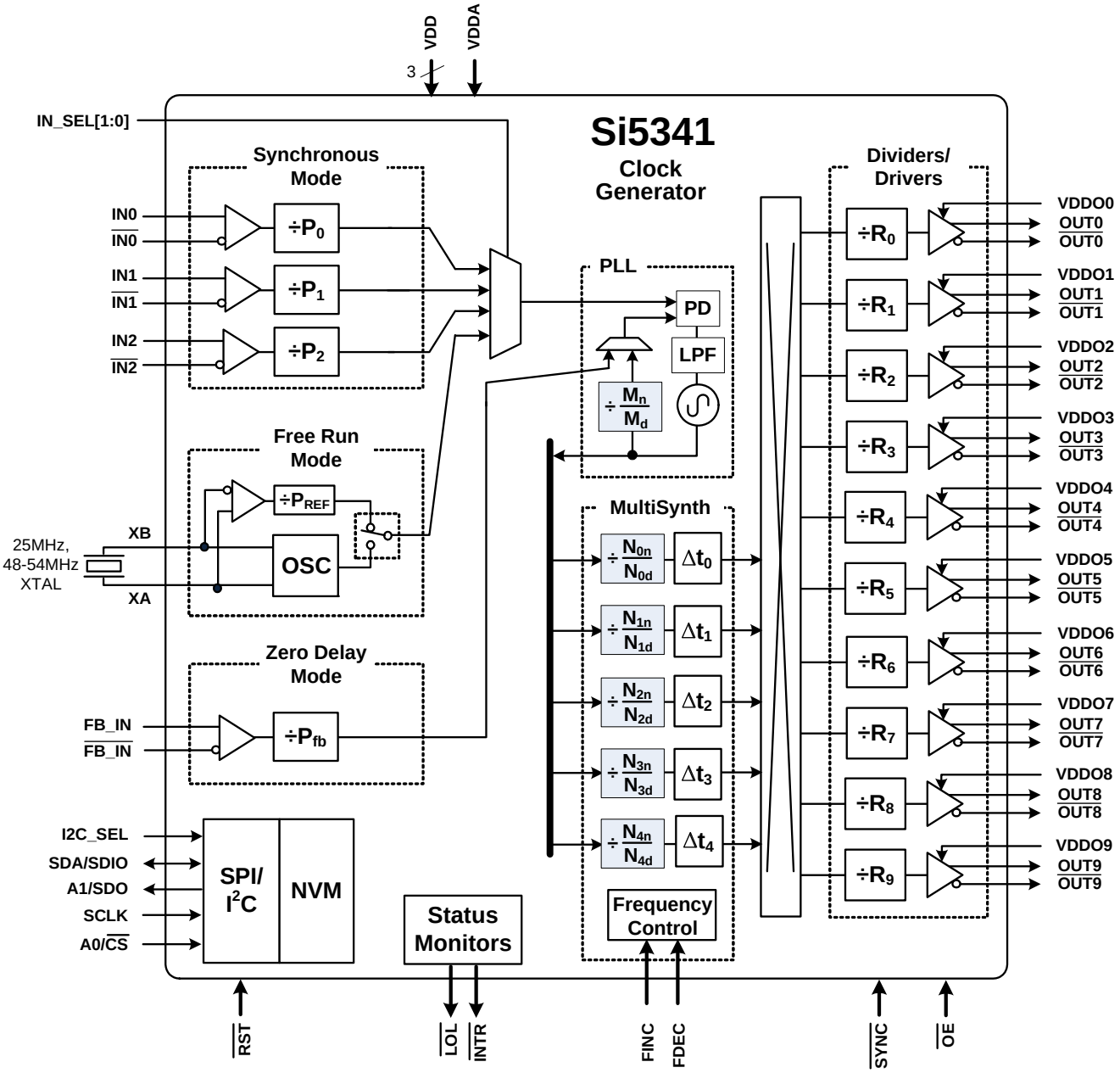


Figure 4. Si5341 Block Diagram

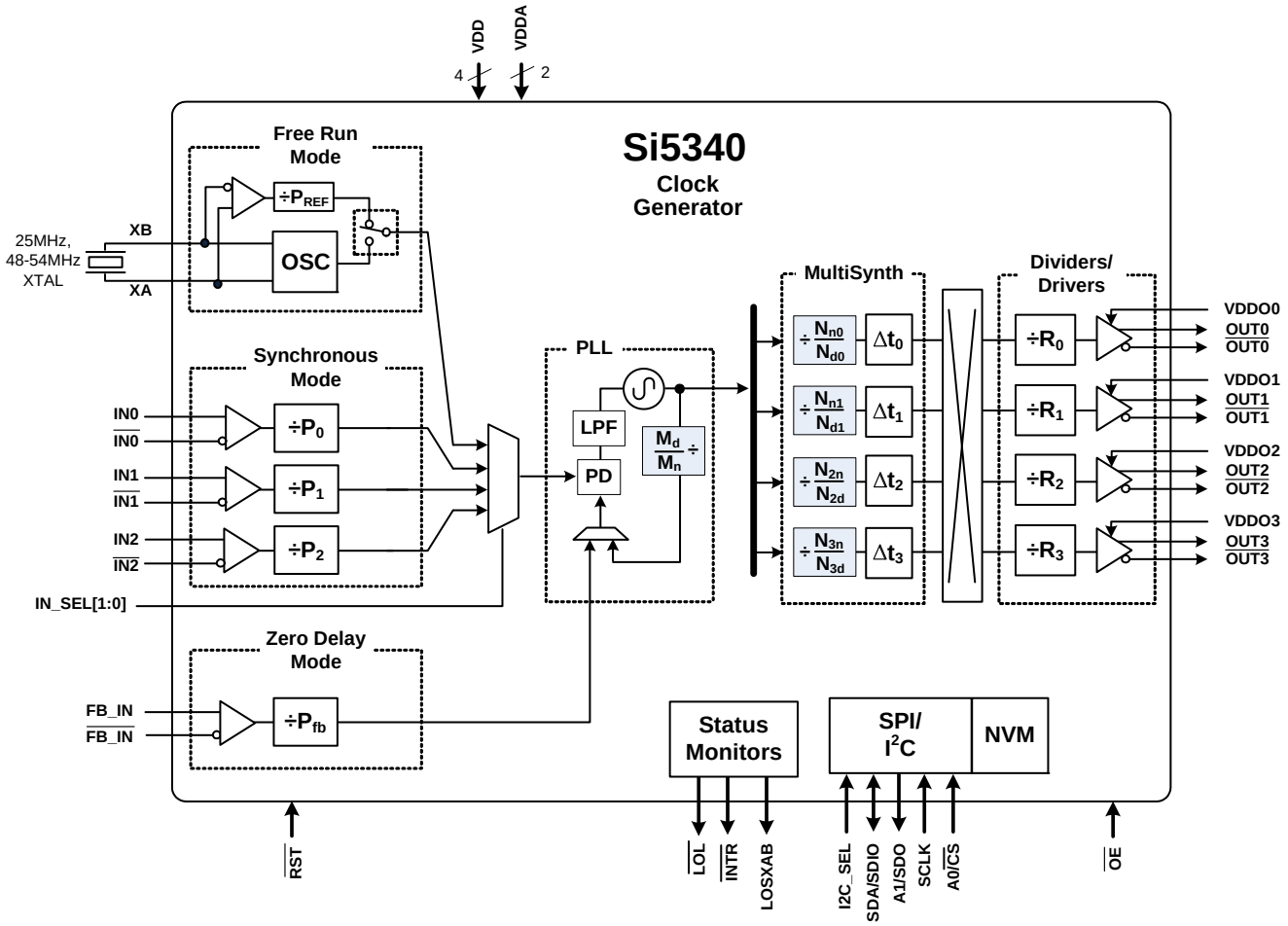


Figure 5. Si5340 Detailed Block Diagram

4. Functional Description

The Si5341/40 combines a wide band PLL with next generation MultiSynth technology to offer the industry's most versatile and high performance clock generator. The PLL locks to either an external crystal (XA/XB) for generating free-running clocks or to an external clock (IN0 - IN2) for generating synchronous clocks. In free-run mode the oscillator frequency is multiplied by the PLL and fractionally divided by the MultiSynth stage to any frequency in the range of 100 Hz to 800 MHz per output. In synchronous mode, any clock frequency at the input pins in the range of 10 MHz to 750 MHz can be multiplied to generate any output frequency from 100 Hz to 800 MHz on each output.

The high-resolution fractional MultiSynth™ dividers enables true any-frequency input to any-frequency on any of the outputs. The output drivers offer flexible output formats which are independently configurable on each of the outputs. This clock generator is fully configurable via its serial interface (I^2C/SPI) and includes in-circuit programmable non-volatile memory.

4.1. Modes of Operation

The Si5341/40 supports both free-run and synchronous modes of operation. Mode selection is manually selected through input pins (IN_SEL0/1) or through the serial interface by writing to the input select register (IN_SEL, 0x21[2:1]). Pin selection is set by default. A state diagram showing the modes of operation is shown in Figure 6.

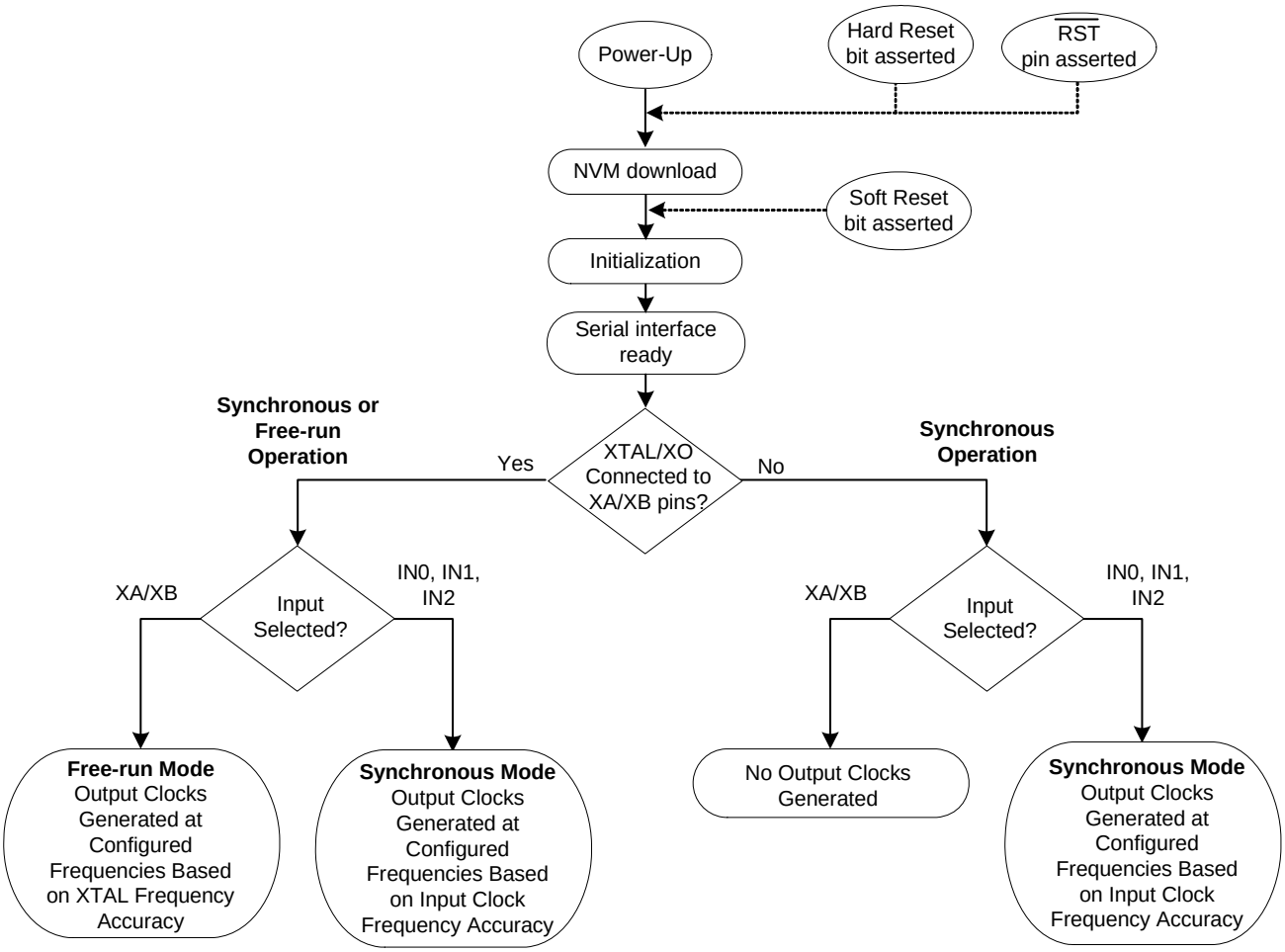


Figure 6. Si5341 Initialization and Modes of Operation

4.1.1. Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is done. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the $\overline{\text{RST}}$ pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

4.1.2. Freerun Mode

The Si5341/40 will enter the free-run mode if the a crystal input (XA/XB) is selected as its input source. Output frequencies will be generated with a frequency accuracy determined by the external crystal connected to the XA/XB pins. Any change or drift of the crystal frequency will be tracked by the output clocks. If the XA/XB input is not selected as the device input, or if a XTAL is not connected to the XA/XB pins, the Si5341/40 will not enter the free-run mode and no output clocks will be generated.

4.1.3. Synchronous Mode

If one of the input pins (IN0-IN2) is selected, the Si5341/40 will operate in synchronize mode if there is a valid clock at the selected input. Once lock is achieved, the output clocks will be phase locked to the input clock. If the selected clock fails the output clocks will stop until an alternate input clock is manually selected.

4.2. Frequency Configuration

The phase-locked loop is fully contained and does not require external loop filter components to operate. Its function is to phase lock to the selected input and provide a common synchronous reference to the MultiSynth high-performance fractional dividers.

A crosspoint mux connects any of the MultiSynth divided frequencies to any of the outputs drivers. Additional output integer dividers provides further frequency division if required. The frequency configuration of the device is programmed by setting the input dividers (P), the PLL feedback fractional divider (Mn/Md), the MultiSynth fractional dividers (Nn/Nd), and the output integer dividers (R). Silicon Labs' ClockbuilderPro™ configuration utility determines the optimum divider values for any desired input and output frequency plan.

4.3. Inputs

The Si5341/40 requires either an external crystal at its XA/XB pins for free-run operation or an external input clock (IN0-IN2) for synchronous operation. An external crystal is not required in synchronous mode.

4.3.1. External Reference Input (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce a low jitter reference for the PLL when operating in the free-run mode. A crystal frequency of 25 MHz can be used although crystals in the frequency range of 48 MHz to 54 MHz are recommended for best jitter performance. Frequency offsets due to C_L mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±1000 ppm. The Si5341/40 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Refer to Table 11 for crystal specifications.

The Si5341/40 can also accommodate an external reference clock (REFCLK) instead of a crystal. This allows the use of crystal oscillator (XO) instead of a XTAL. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal load capacitors (C_L) are disabled in the REFCLK mode. Refer to Table 3 for REFCLK requirements. Both a single-ended or a differential REFCLK can be connected to the XA/XB pins as shown in Figure 7. A P_{REF} divider is available to accommodate external clock frequencies higher than 54 MHz. Frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.

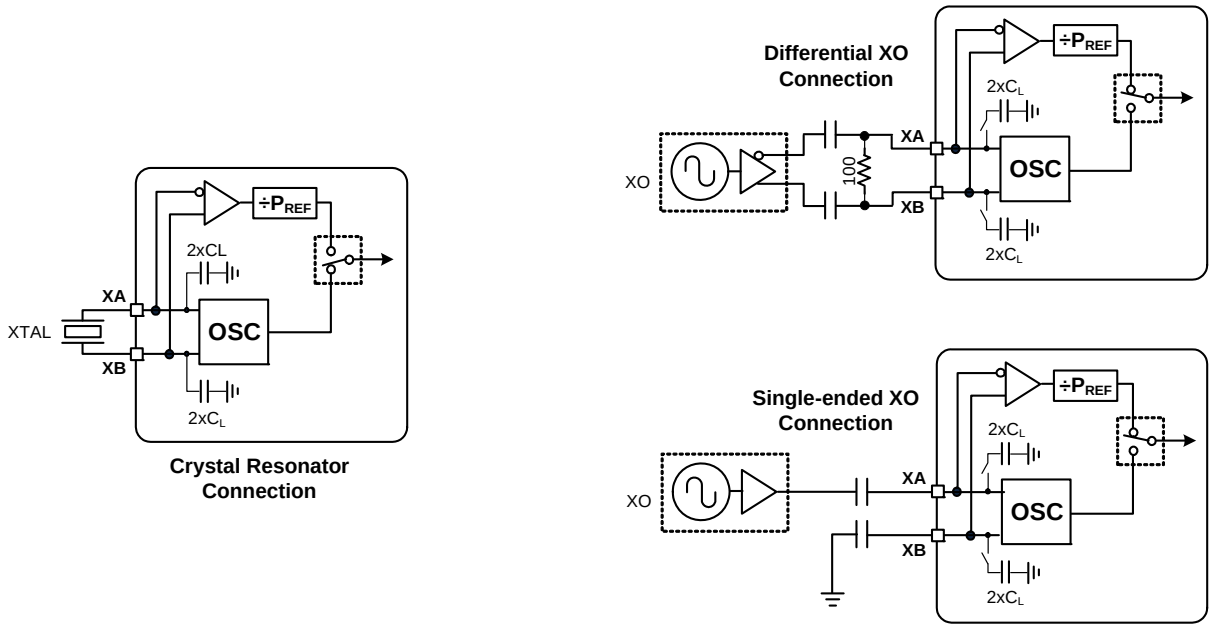


Figure 7. Crystal Resonator and External Reference Clock Connection Options

4.3.2. Input Clocks (IN0, IN1, IN2)

Three input clocks are available to synchronize the PLL when operating in synchronous mode. Each of the inputs can be configured as differential, single-ended, or LVCMOS. The recommended input termination schemes are shown in Figure 8. Differential signals must be AC coupled, while single-ended LVCMOS signals can be AC or DC coupled. Unused inputs can be disabled by register configuration.

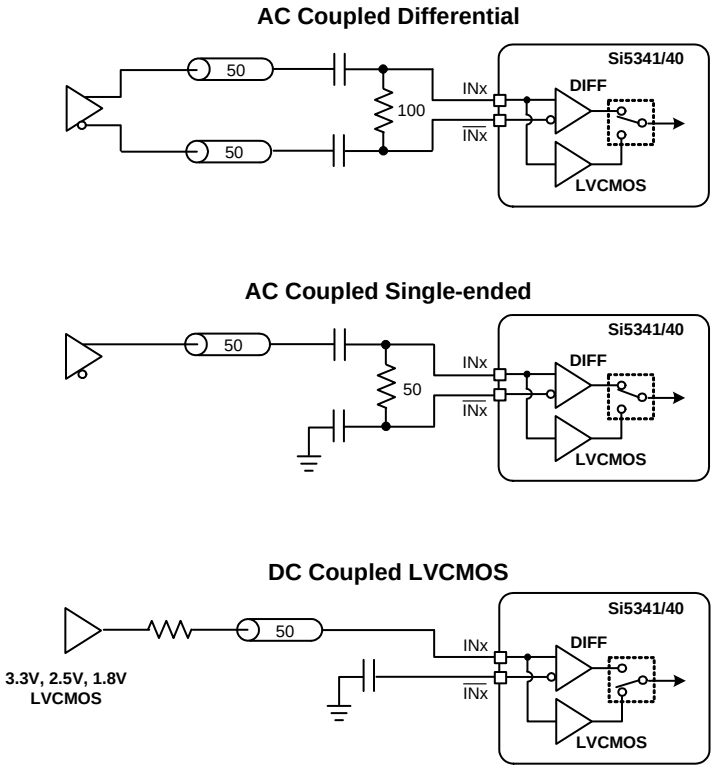


Figure 8. Termination of Differential and LVCMOS Input Signals

4.3.3. Input Selection (IN0, IN1, IN2, XA/XB)

The active clock input is selected using the IN_SEL[1:0] pins or by register control. A register bit determines input selection as pin or register selectable. The IN_SEL pins are selected by default. They are internally pulled high so that the free-run mode is automatically selected when left unconnected. If there is no clock signal on the selected input, the device will not generate output clocks.

Table 14. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	Comment
0	0	IN0	Synchronous mode
0	1	IN1	
1	0	IN2	
1	1	XA/XB	Free-run mode (default)

4.4. Fault Monitoring

The Si5341/40 provides fault indicators which monitor loss of signal (LOS) of the inputs (IN0, IN1, IN2, XA/XB, FB_IN) and loss of lock (LOL) for the PLL. This is shown in Figure 9.

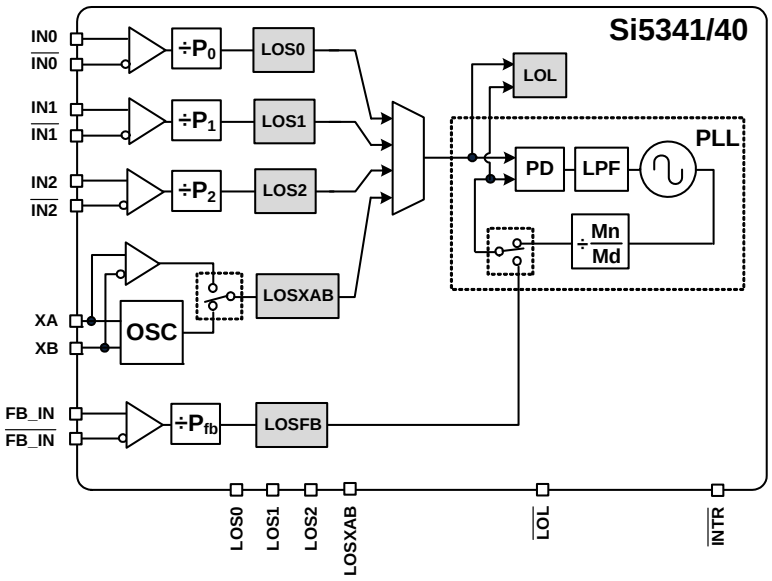


Figure 9. LOS and LOL Fault Monitors

4.4.1. Status Indicators

The state of the status monitors are accessible by reading registers through the serial interface or with dedicated pin ($\overline{\text{LOL}}$). Each of the status indicator register bits has a corresponding sticky bit in a separate register location. Once a status bit is asserted its corresponding sticky bit will remain asserted until cleared. Writing a logic zero to a sticky register bit clears its state.

4.4.2. Interrupt pin ($\overline{\text{INTR}}$)

An interrupt pin ($\overline{\text{INTR}}$) indicates a change in state with any of the status registers. All status registers are maskable to prevent assertion of the interrupt pin. The state of the $\overline{\text{INTR}}$ pin is reset by clearing the status registers.

4.5. Outputs

The Si5341 supports 10 differential output drivers which can be independently configured as differential or LVCMOS. The Si5340 supports 4 output drivers independently configurable as differential or LVCMOS.

4.5.1. Output Signal Format

The differential output swing and common mode voltage are both fully programmable and compatible with a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

4.5.2. Differential Output Terminations

The differential output drivers support both AC coupled and DC coupled terminations as shown in Figure 10.

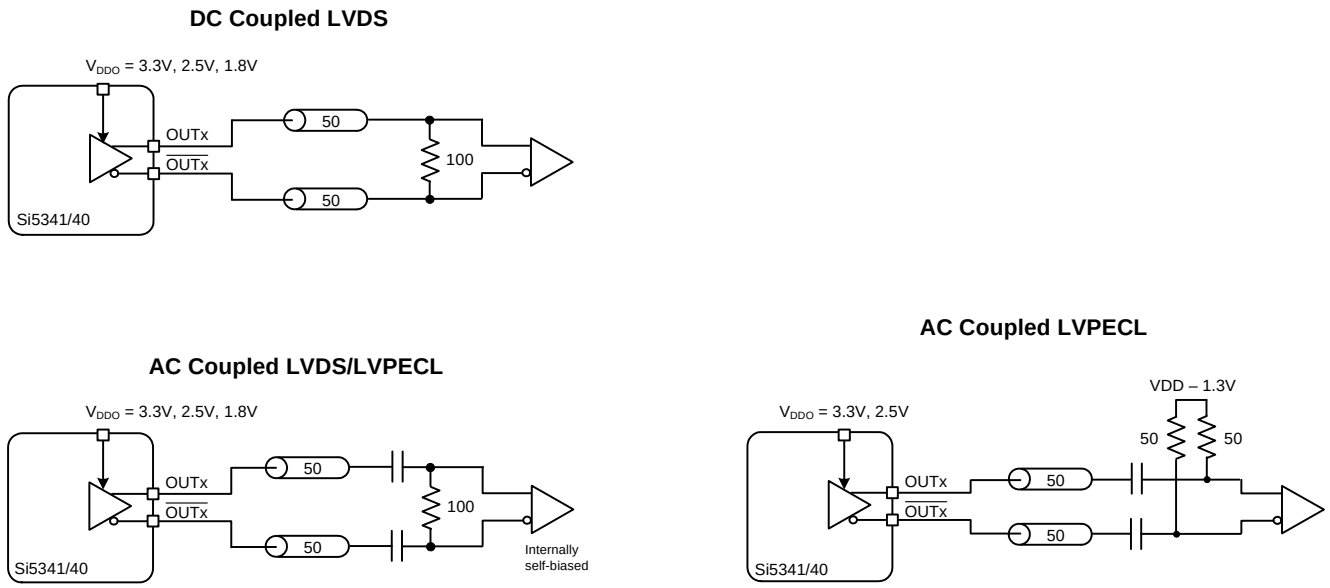


Figure 10. Supported Differential Output Terminations

4.5.3. Differential Output Swing Modes

There are two selectable differential output swing modes: Normal and High. Each output can support a unique mode.

- **Differential Normal Swing Mode:** When an output driver is configured in normal swing mode, its output swing is selectable as one of 7 settings ranging from 200 mVpp_se to 800 mVpp_se in increments of 100 mV. The output impedance in the Normal Swing Mode is 100Ω differential. Any of the terminations shown in Figure 10 are supported in this mode.
- **Differential High Swing Mode:** When an output driver is configured in high swing mode, its output swing is configurable as one of 7 settings ranging from 400 mVpp_se to 1600 mVpp_se in increments of 200 mV. The output driver is in high impedance mode and supports standard 50Ω. PCB traces. Any of the terminations shown in Figure 10 are supported in this mode.

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

4.5.4. Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential Normal and High Swing modes is programmable in 100 mV increments from 0.7 V to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when DC coupling the output drivers.

4.5.5. LVCMOS Output Terminations

LVCMOS outputs are dc-coupled as shown in Figure 11.

DC Coupled LVCMOS

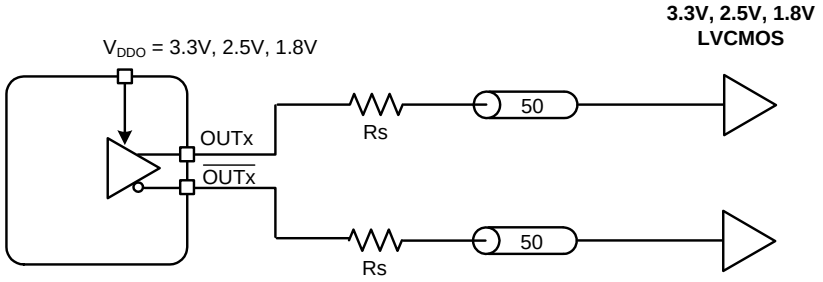


Figure 11. LVCMOS Output Terminations

4.5.6. LVCMOS Output Impedance And Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor (Rs) is recommended to help match the selected output impedance to the trace impedance (i.e. Rs = Trace Impedance - Zs). There are three programmable output impedance selections (CMOS1, CMOS2, CMOS3) for each VDDO options as shown in Table 15.

Table 15. Typical Output Impedance (Z_S)

	CMOS_DRIVE_Selection		
VDDO	**CMOS1**	**CMOS2**	**CMOS3**
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

4.5.7. LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

4.5.8. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and $\overline{\text{OUTx}}$). By default the clock on the $\overline{\text{OUTx}}$ pin is generated with complimentary polarity with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

4.5.9. Output Enable/Disable

The $\overline{\text{OE}}$ pin provides a convenient method of disabling or enabling the output drivers. When the $\overline{\text{OE}}$ pin is held high all outputs will be disabled. When held low, the outputs will be enabled. Outputs in the enabled state can be individually disabled through register control.

4.5.10. Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable low, disable high, disable high-impedance, or stop-mid (differential outputs).

4.5.11. Synchronous/Asynchronous Output Disable Feature

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode the output clock will disable immediately without waiting for the period to complete.

4.5.12. Output Skew Control ($\Delta t_0 - \Delta t_4$)

The Si5341/40 uses independent MultiSynth dividers (N_0 - N_4) to generate up to 5 unique frequencies to its 10 outputs through a crosspoint switch. By default all clocks are phase aligned. A delay path (Δt_0 - Δt_4) associated with each of these dividers is available for applications that need a specific output skew configuration. This is useful for PCB trace length mismatch compensation. The resolution of the phase adjustment is approximately 0.28 ps per step definable in a range of ±9.14 ns. Phase adjustments are register configurable. An example of generating two frequencies with unique configurable path delays is shown in Figure 12.

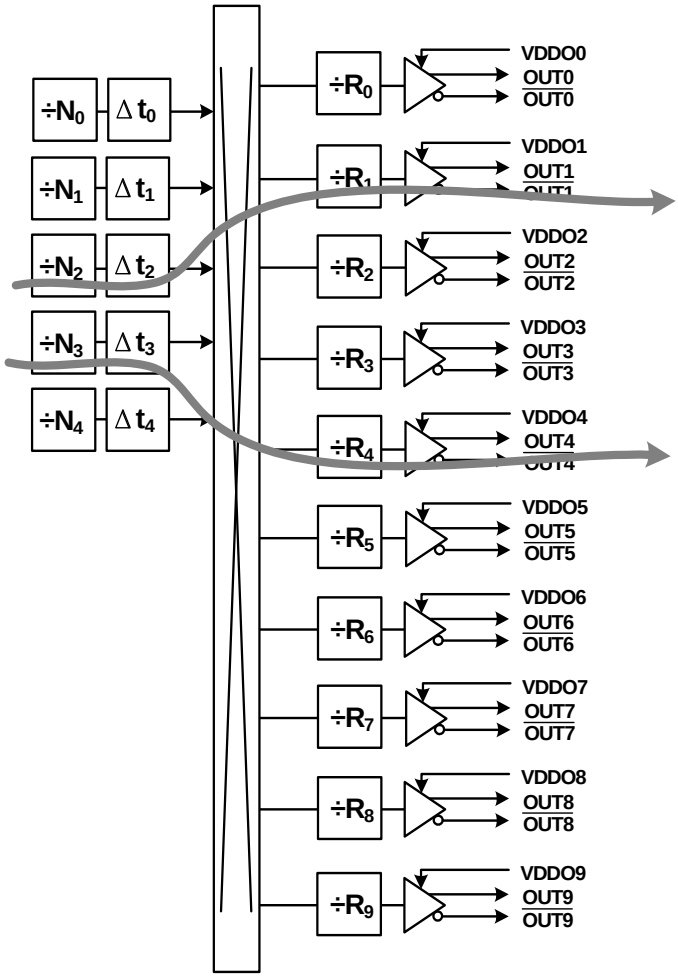


Figure 12. Example of Independently Configurable Path Delays

All phase delay values are restored to their default values after power-up, hard reset, or a reset using the $\overline{\text{RST}}$ pin. Phase delay default values can be written to NVM allowing a custom phase offset configuration at power-up or after power-on reset, or after a hardware reset using the $\overline{\text{RST}}$ pin.

4.5.13. Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in Figure 13. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9 (OUT3 for the Si5340) and FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and AC coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance.

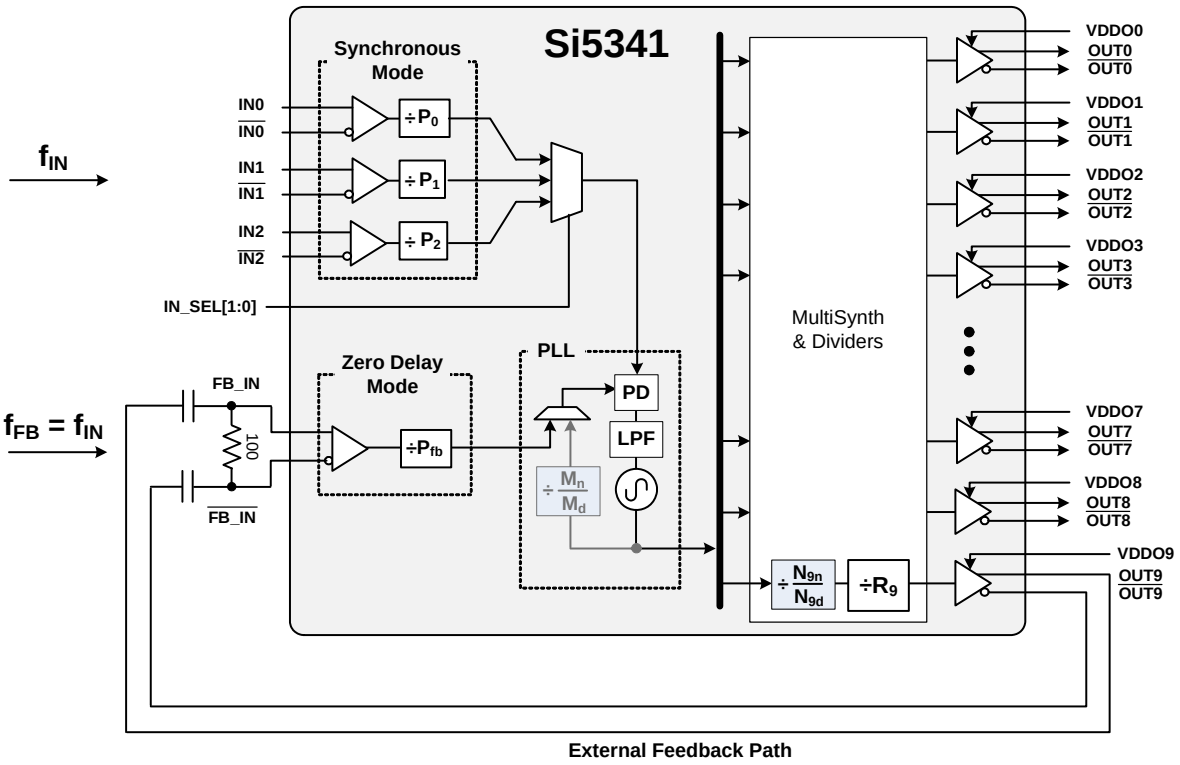


Figure 13. Si5341 Zero Delay Mode Setup

4.5.14. Sync Pin (Synchronizing R Dividers)

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the $\overline{\text{RST}}$ pin or asserting the hard reset bit will have the same result. The $\overline{\text{SYNC}}$ pin provides another method of re-aligning the R dividers without resetting the device. This pin is positive edge triggered. Asserting the sync register bit provides the same function. R dividers can also be reset individually using the R divider reset bits.

4.5.15. Output Crosspoint

The output crosspoint allows any of the N dividers to connect to any of the clock outputs.

4.5.16. Frequency Increment/Decrement

Each of the MultiSynth fractional dividers can be independently stepped up or down in predefined steps with a resolution as low as 0.001 ppb. Setting of the step size and control of the frequency increment or decrement is accomplished through the serial interface. The frequency steps can be controlled through register writes or with the FINC and FDEC pins. The frequency increment and decrement feature is useful in applications requiring a variable clock frequency (e.g., CPU speed control, FIFO overflow management, DCO or NCO, etc.) or in applications where frequency margining (e.g. fout ±5%) is necessary for design verification and manufacturing test. Defining FINC/FDEC step size can be easily determined using ClockBuilder Pro™.

4.6. Power Management

Several unused functions can be powered down to minimize power consumption. Consult the Si5341/40 Family Reference Manual and ClockBuilder Pro configuration utility for details.

4.7. In-Circuit Programming

The Si5341/40 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5341/40 Family Reference Manual for a detailed procedure for writing registers to NVM.

4.8. Serial Interface

Configuration and operation of the Si5341/40 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3V and 1.8V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Si5341/40 Family Reference Manual for details.

4.9. Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship to you within two weeks.

5. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible register such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in “5.2. High-Level Register Map” . Refer to the Si5341/40 Family Reference Manual for a complete list of registers descriptions and settings.

5.1. Addressing Scheme

The device registers are accessible using a 16-bit address which consists of an 8-bit page address + 8-bit register address. By default the page address is set to 0x00. Changing to another page is accomplished by writing to the ‘Set Page Address’ byte located at address 0x01 of each page.

5.2. High-Level Register Map

Table 16. High-Level Register Map

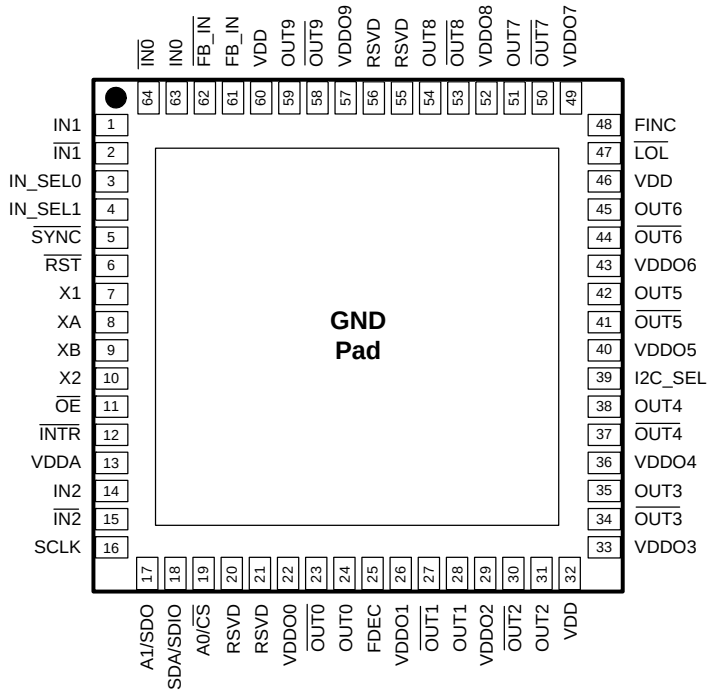
16-Bit Address		Content
8-bit Page Address	**8-bit Register Address Range**	
00	00	Revision IDs
	01	Set Page Address
	02–0A	Device IDs
	0B–15	Alarm Status
	17–1B	INTR Masks
	1C	Reset controls
	2C–E1	Alarm Configuration
	E2–E4	NVM Controls
	FE	Device Ready Status
01	01	Set Page Address
	08–3A	Output Driver Controls
	41–42	Output Driver Disable Masks
	FE	Device Ready Status

Table 16. High-Level Register Map (Continued)

16-Bit Address		Content
8-bit Page Address	**8-bit Register Address Range**	
02	01	Set Page Address
	02–05	XTAL Frequency Adjust
	08–2F	Input Divider (P) Settings
	30	Input Divider (P) Update Bits
	35–3D	PLL Feedback Divider (M) Settings
	3E	PLL Feedback Divider (M) Update Bit
	47–6A	Output Divider (R) Settings
	6B–72	User Scratch Pad Memory
	FE	Device Ready Status
03	01	Set Page Address
	02–37	MultiSynth Divider (N0–N4) Settings
	0C	MultiSynth Divider (N0) Update Bit
	17	MultiSynth Divider (N1) Update Bit
	22	MultiSynth Divider (N2) Update Bit
	2D	MultiSynth Divider (N3) Update Bit
	38	MultiSynth Divider (N4) Update Bit
	39–58	FINC/FDEC Settings N0–N4
	59–62	Output Delay (Δt) Settings
	63–94	Frequency Readback N0–N4
	FE	Device Ready Status
04–08	00–FF	Reserved
09	01	Set Page Address
	49	Input Settings
	1C	Zero Delay Mode Settings
A0–FF	00–FF	Reserved

6. Pin Descriptions

Si5341 64QFN
Top View



Si5340 44QFN
Top View

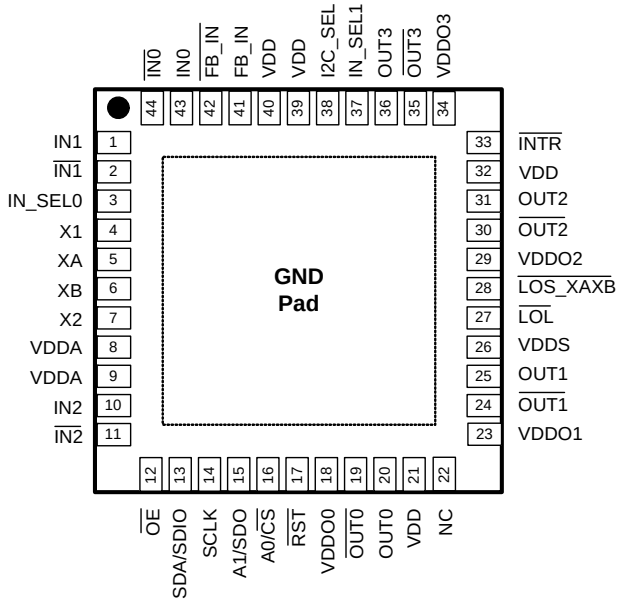


Table 17. Si5341/40 Pin Descriptions

Pin Name	Pin Number		Pin Type[1]	Function
Inputs				
XA	8	5	I	**Crystal Input** These pins are used for an optional XTAL input when operating the device in asynchronous mode (i.e. free-run mode). Alternatively, an external reference clock (REFCLK) can be applied to these pins. See "4.3.1. External Reference Input (XA/XB)" on page 22. An external XTAL or REFCLK is not needed when operating in synchronous mode when the device is locked to an external input clock through the clock input pins (IN0 to IN2). These pins can be left unconnected when not in use.
XB	9	6	I	
X1	7	4	I	**XTAL Shield** Connect these pins directly to the XTAL ground pins. X1, X2, and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5341/40 Family Reference Manual for layout guidelines. These pins should be left disconnected when connecting XA/XB pins to an external reference clock (REFCLK).
X2	10	7	I	

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5341/40 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
IN0	63	43	I	**Clock Inputs** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to "4.3.2. Input Clocks (IN0, IN1, IN2)" on page 23 for input termination options. These pins are high-impedance and must be terminated externally. Unused inputs can be disabled by register configuration and the pins left unconnected.
$\overline{\text{IN0}}$	64	44	I	
IN1	1	1	I	
$\overline{\text{IN1}}$	2	2	I	
IN2	14	10	I	
$\overline{\text{IN2}}$	15	11	I	
FB_IN	61	41	I	**External Feedback Input** These pins are used as the external feedback input (FB_IN/ $\overline{\text{FB\_IN}}$) for the optional zero delay mode. See "4.5.13. Zero Delay Mode" on page 28 for details on the optional zero delay mode.
$\overline{\text{FB\_IN}}$	62	42	I	

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5341/40 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
Outputs				
OUT0	24	20	O	**Output Clocks** These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in "4.5.2. Differential Output Terminations" on page 25 and "4.5.5. LVCMOS Output Terminations" on page 26. Unused outputs should be left unconnected.
$\overline{\text{OUT0}}$	23	19	O	
OUT1	28	25	O	
$\overline{\text{OUT1}}$	27	24	O	
OUT2	31	31	O	
$\overline{\text{OUT2}}$	30	30	O	
OUT3	35	36	O	
$\overline{\text{OUT3}}$	34	35	O	
OUT4	38	—	O	
$\overline{\text{OUT4}}$	37	—	O	
OUT5	42	—	O	
$\overline{\text{OUT5}}$	41	—	O	
OUT6	45	—	O	
$\overline{\text{OUT6}}$	44	—	O	
OUT7	51	—	O	
$\overline{\text{OUT7}}$	50	—	O	
OUT8	54	—	O	
$\overline{\text{OUT8}}$	53	—	O	
OUT9	59	—	O	
$\overline{\text{OUT9}}$	58	—	O	

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5341/40 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
Serial Interface				
I2C_SEL	39	38	I	**I2C Select** This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high. See Note 2.
SDA/SDIO	18	13	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when is SPI mode. See Note 2.
A1/SDO	17	15	I/O	**Address Select 1/Serial Data Output** In I^2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode this is the serial data output (SDO) pin. See Note 2.
SCLK	16	14	I	**Serial Clock Input** This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. See Note 2.
A0/$\overline{CS}$	19	16	I	**Address Select 0/Chip Select** This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up. See Note 2.

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5341/40 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
Control/Status				
$\overline{\text{INTR}}$	12	33	O	**Interrupt** This pin is asserted low when a change in device status has occurred. This pin must be pulled-up using an external resistor of at least 1 kΩ. It should be left unconnected when not in use. See Note 2.
$\overline{\text{RST}}$	6	17	I	**Device Reset** Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up. See Note 2.
$\overline{\text{OE}}$	11	12	I	**Output Enable** This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. See Note 2.
$\overline{\text{LOL}}$	47	—	O	**Loss Of Lock** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use. See Note 2.
	—	27	O	**Loss Of Lock** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use. See Note 3.
$\overline{\text{LOS\_XAXB}}$	—	28	O	**Loss Of Signal** This output pin indicates a loss of signal at the XA/XB pins. See note 2.
$\overline{\text{SYNC}}$	5	—	I	**Output Clock Synchronization** An active low signal on this pin resets the output dividers for the purpose of re-aligning the output clocks. This pin is internally pulled-up and can be left unconnected when not in use. See note 2.
FDEC	25	—	I	**Frequency Decrement Pin** This pin is used to step-down the output frequency of a selected output. The affected output driver and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use. See note 2.

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5341/40 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
FINC	48	—	I	**Frequency Increment Pin** This pin is used to step-up the output frequency of a selected output. The affected output and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use. See note 2.
IN_SEL0	3	3	I	**Input Reference Select** The IN_SEL[1:0] pins are used in the manual pin controlled mode to select the active clock input as shown in Table 14. See note 2.
IN_SEL1	4	37	I	
RSVD	20	22	—	**Reserved** These pins are connected to the die. Leave disconnected.
	21	—	—	
	55	—	—	
	56	—	—	
NC	—	22	—	**No Connect** These pins are not connected to the die. Leave disconnected.

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5341/40 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
Power				
VDD	32	21	P	**Core Supply Voltage** The device core operates from a 1.8V supply. See the Si5341/40 Family Reference Manual for power supply filtering recommendations.
	46	32		
	60	39		
	—	40		
VDDA	13	8	P	Core Supply Voltage 3.3V This core supply pin requires a 3.3V power source. See the Si5341/40 Family Reference Manual for power supply filtering recommendations.
	—	9	P	
VDDS	—	26	P	Status Output Voltage The voltage on this pin determines the V_{OL}/V_{OH} on $\overline{LOL}$ and LOS_XAXB status output pins. See the Si5341/40 Family Reference Manual for power supply filtering recommendations.
VDDO0	22	18	P	**Output Clock Supply Voltage 0–9** Supply voltage (3.3 V, 2.5 V. 1.8 V) for OUTn, $\overline{OUTn}$ outputs. See the Si5341/40 Family Reference Manual for power supply filtering recommendations. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	26	23	P	
VDDO2	29	29	P	
VDDO3	33	34	P	
VDDO4	36	—	P	
VDDO5	40	—	P	
VDDO6	43	—	P	
VDDO7	49	—	P	
VDDO8	52	—	P	
VDDO9	57	—	P	
GND PAD			P	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

7. Ordering Guide

Ordering Part Number (OPN)	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes (Typical Jitter)	Package	Temperature Range
Si5341					
Si5341A-A-GM[1,2]	3/10	0.0001 to 800 MHz	Integer (100 fs) fractional (150 fs)	64-Lead 9x9 QFN	-40 to 85 °C
Si5341B-A-GM[1,2]		0.0001 to 350 MHz			
Si5341C-A-GM[1,2]		0.0001 to 800 MHz	Integer Only (100 fs)		
Si5341D-A-GM[1,2]		0.0001 to 350 MHz			
Si5340					
Si5340A-A-GM[1,2]	3/4	0.0001 to 800 MHz	Integer (100 fs) fractional (150 fs)	44-Lead 7x7 QFN	-40 to 85 °C
Si5340B-A-GM[1,2]		0.0001 to 350 MHz			
Si5340C-A-GM[1,2]		0.0001 to 800 MHz	Integer Only (100 fs)		
Si5340D-A-GM[1,2]		0.0001 to 350 MHz			
Si5341/40-EVB					
Si5341-EVB	—	—	—	Evaluation Board	—
Si5340-EVB					

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by Silicon Labs and the ClockBuilder Pro software utility.
3. Custom part number format is: e.g., Si5341A-Axxxxx-GM, where “xxxxx” is a unique numerical sequence representing the preprogrammed configuration.

8. Package Outlines

8.1. Si5341 9x9 mm 64-QFN Package Diagram

Figure 14 illustrates the package details for the Si5341. Table 18 lists the values for the dimensions shown in the illustration.

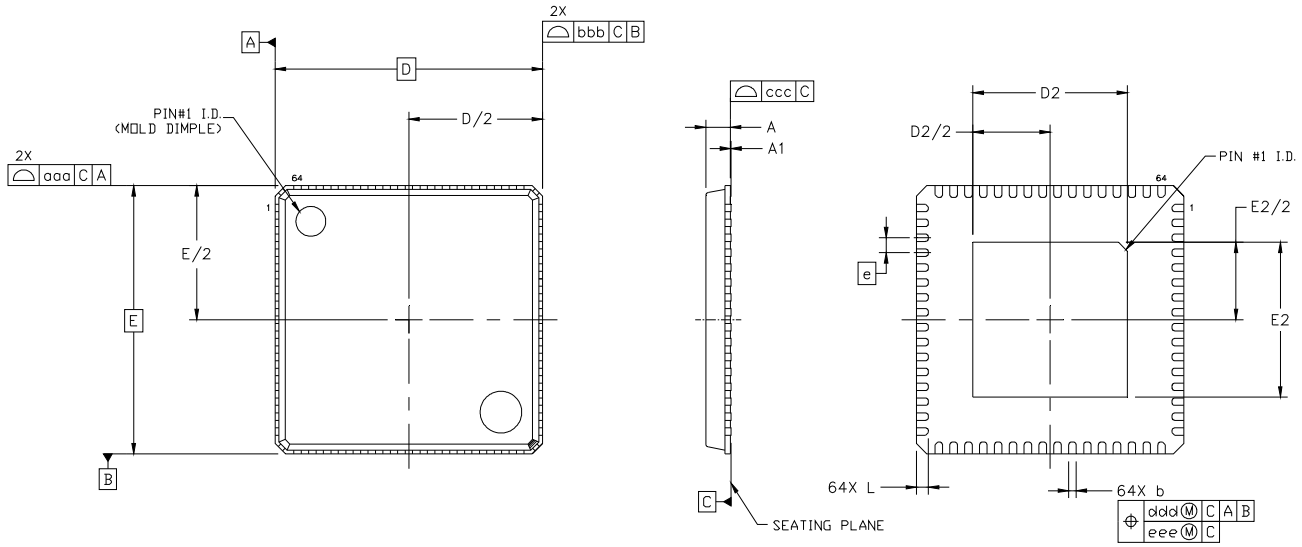


Figure 14. 64-Pin Quad Flat No-Lead (QFN)

Table 18. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2. Si5340 7x7 mm 44-QFN Package Diagram

Figure 15 illustrates the package details for the Si5340. Table 19 lists the values for the dimensions shown in the illustration.

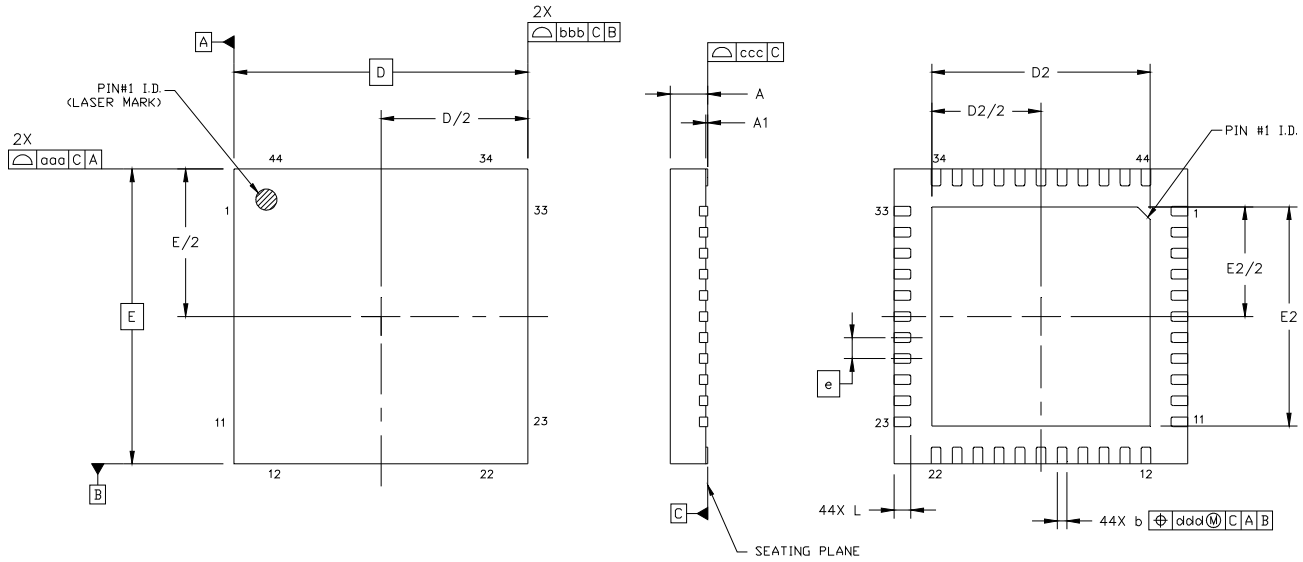


Figure 15. 44-Pin Quad Flat No-Lead (QFN)

Table 19. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

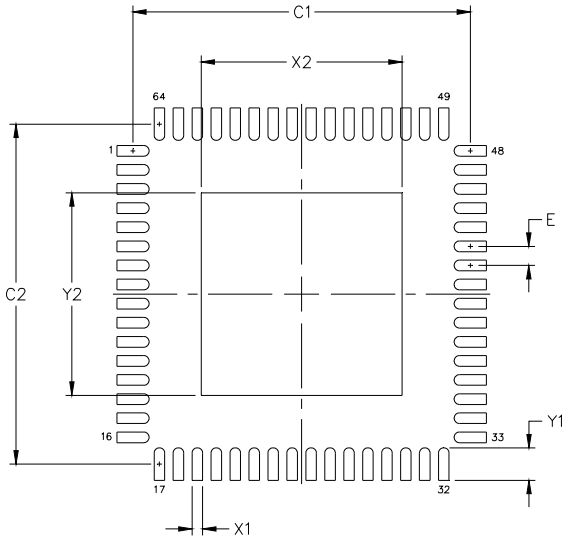
Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. PCB Land Pattern

Figure 16 illustrates the PCB land pattern details for the devices. Table 20 lists the values for the dimensions shown in the illustration.

Si5341



Si5340

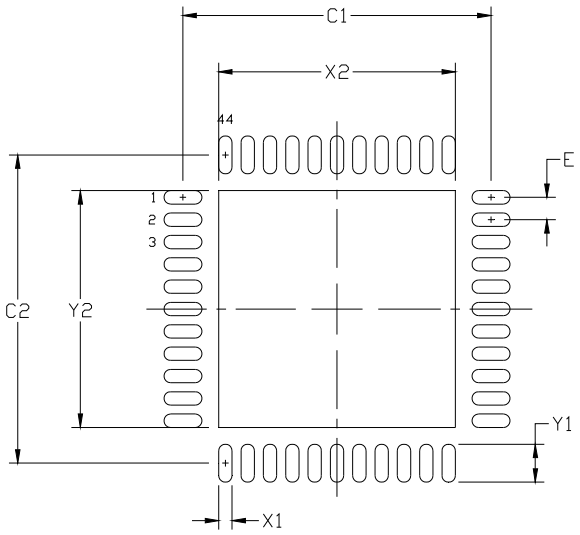


Figure 16. PCB Land Pattern

Table 20. PCB Land Pattern Dimensions

Dimension	Si5347 (Max)	Si5346 (Max)
C1	8.90	6.90
C2	8.90	6.90
E	0.50	0.50
X1	0.30	0.30
Y1	0.85	0.85
X2	5.30	5.30
Y2	5.30	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

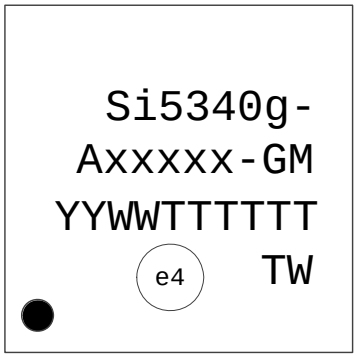
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Top Marking

64-QFN



44-QFN

Line	Characters	Description
1	Si5341g- Si5340g-	Base part number and Device Grade for Low Jitter, Any-Frequency, 10-output Clock Generator. Si5341: 10-output, 64-QFN Si5340: 4-output, 44-QFN g = Device Grade (A, B, C, D). See "7. Ordering Guide" on page 39 for more information. – = Dash character.
2	Axxxxx-GM	A = Product revision. (Refers to die revision A1). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) or 1.4 mm (44-QFN) diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

11. Device Errata

Please log in or register at www.silabs.com to access the device errata document.

APPENDIX—ADVANCE PRODUCT INFORMATION REVISION HISTORY

Table 21 lists the advance product information revision history.

Table 21. Advance Product Information Revision History

Revision	Change Description	Date
0.11	First draft	Aug 2012
0.12	■ Added clarification to section 1 on unused control inputs, unused clock inputs, and pull-up resistors for the I^2C interface.	Aug 2012
0.13	■ Updated block diagram ■ Other minor edits	Dec 2012
0.20	■ Updated pinouts, block diagrams, and electrical specifications ■ Programmable status pins (S0-S3) have been assigned to LOS status pins ■ Added register map information ■ Added package outline, land patterns, ordering guide, top markings ■ Reduced MultiSynth from 10 to 5 ■ Combined Si5341 and Si5340 data sheets ■ Added application diagram	Jun 2013
0.21	■ Minor updates from review cycle ■ Added new SPI streaming command ■ Added SPI timing diagrams ■ Added high level register map	July 2013
0.22	■ Minor edits	July 2013
0.23	■ Changed FINC/FDEC frequency step resolution from 0.05 ppb/step to 0.01 ppb/step. ■ Added REFCLK max input voltage swing specification of 1200 mVpp_se ■ Si5341 pin changes: • Renamed pin 13: VDD33 to VDDA • Renamed pins 32, 46, 60: VDD18 to VDD • Removed LOS0 function on pin 20. Renamed pin 20 to RSVD. • Removed LOS1 function on pin 21. Renamed pin 21 to RSVD. • Removed LOS2 function on pin 58. • Removed $\overline{\text{LOS}}$_XAXB on pin 59. • Moved $\overline{\text{OUT9}}$ from 55 to 58. Renamed pin 55 to RSVD • Moved $\overline{\text{OUT9}}$ from 56 to 59. Renamed pin 56 to RSVD ■ Si5340 pin changes: • Renamed pins 8, 9: VDD33 to VDDA • Renamed pins 21, 32, 39, 40: VDD18 to VDD • Renamed pin 26: VDD18 to VDDS ■ Other minor edits	Oct 2013
0.24	■ Updated Section 9 - Ordering Guide	Oct 2013
0.25	■ Minor edits	Oct 2013

Table 21. Advance Product Information Revision History (Continued)

Revision	Change Description	Date
0.26	■ Corrections to the Si5340 pin diagram of section 6 - Pin Descriptions: • Renamed pin 21 from VDD18 to VDD • Renamed pin 22 from RSVD to NC • Renamed pin 28 from LOS_XAXB to $\overline{\text{LOS\_XAXB}}$ • Renamed pin 41 from IN3/$\overline{\text{FB\_IN}}$ to $\overline{\text{FB\_IN}}$ • Renamed pin 42 from IN3/$\overline{\text{FB\_IN}}$ to $\overline{\text{FB\_IN}}$ ■ Corrections to the Si5340 pin list of section 6 - Pin Descriptions: • Renamed pin 22 from RSVD to NC • Renamed pin 28 from LOS_XAXB to $\overline{\text{LOS\_XAXB}}$ ■ Updated Section 9 - Ordering Guide	Nov 2013
0.30	■ Moved the register descriptions to the Si53451/40 Reference Manual. ■ Moved the majority of the contents of the Serial Interface section to the Si5341/40 Reference Manual. ■ Changed the output delay specification from “1 ps steps with a range of ±8.32 ns” to “0.28 ps steps with a range of ±9.14 ns”. Added this to the specification table. ■ Updated LVCMOS output impedance values in Table 15. ■ Added Control Input and Status Output table specifications. ■ Changed pin names XGND to X1 and X2. Functionality remains the same. ■ Added serial interface timing diagrams and specifications	Jun 2014

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