



# Si5341-D EVALUATION BOARD USER'S GUIDE

#### Description

The Si5341-D-EVB is used for evaluating the Si5341 Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier revision D. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5341-D-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

#### **EVB** Features

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL allows free-run mode of operation on the Si5341 or up to 3 input clocks for synchronous clocking.
- Feedback clock input for optional zero delay mode.
- ClockBuilder<sup>®</sup> Pro (CBPro) GUI programmable V<sub>DD</sub> supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI programmable V<sub>DDO</sub> supplies allow each of the 10 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI-controlled voltage, current, and power measurements of V<sub>DD</sub> and all V<sub>DDO</sub> supplies.
- Status LEDs for power supplies and control/status signals of Si5341.
- SMA connectors for input and output clocks.



Figure 1. Si5341-D Evaluation Board

## 1. Functional Block Diagram

Below is a functional block diagram of the Si5341-D-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See section "3. Quick Start" or section "8. Installing ClockBuilder Pro Desktop Software" for more information.

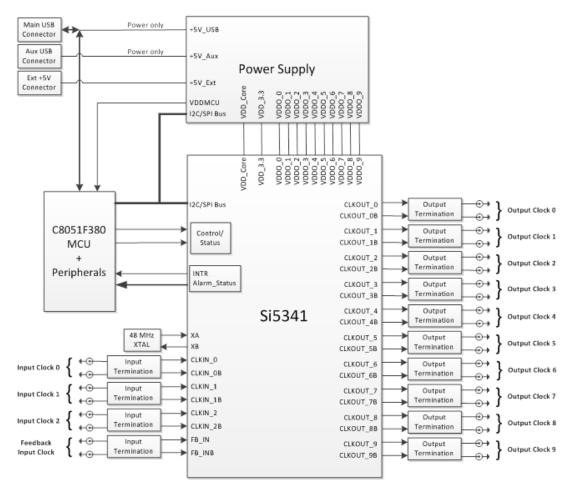


Figure 2. Si5341-D-EB Functional Block Diagram



## 2. Si5341-D-EVB Support Documentation and ClockBuilder Pro Software

All Si5341-D-EVB schematics, BOMs, User's Guides, and software can be found online at the following link: http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

## 3. Quick Start

- 1. Install ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.
- 2. Connect a USB cable from Si5341-D-EB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in Table 1.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5341-D-EB.
- 6. For the Si5341 data sheet, go to http://www.silabs.com/timing.



## 4. Jumper Defaults

Location	Туре	I = Installed 0 = Open		Location	Туре	l = Installed 0 = Open
JP1	2 pin	0		JP23	2 pin	0
JP2	2 pin	I		JP24	2 pin	0
JP3	2 pin	0		JP25	2 pin	0
JP4	2 pin	I		JP26	2 pin	0
JP5	2 pin	I		JP27	2 pin	0
JP6	2 pin	I		JP28	2 pin	0
JP7	2 pin	I		JP29	2 pin	0
JP8	2 pin	I		JP30	2 pin	0
JP9	2 pin	0		JP31	2 pin	0
JP10	2 pin	I		JP32	2 pin	0
JP13	2 pin	0		JP33	2 pin	0
JP14	2 pin	I		JP34	2 pin	0
JP15	3 pin	1 to 2		JP35	2 pin	0
JP16	3 pin	1 to 2		JP36	2 pin	0
JP17	2 pin	0		JP38	3 pin	All Open
JP18	2 pin	0		JP39	2 pin	0
JP19	2 pin	0		JP40	2 pin	0
JP20	2 pin	0		JP41	2 pin	0
JP21	2 pin	0		J36	5 x 2 Hdr	All 5 installed
JP22	2 pin	0				
*Note: Refer to	the Si5341	-D-EB schematics for	the	functionality ass	ociated with ea	ach jumper.

## Table 1. Si5341-D-EB Jumper Defaults



## 5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy

Table 2. Si5341-D-EB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5341 +3.3 V, and Si5341 V<sub>DD</sub> supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity.

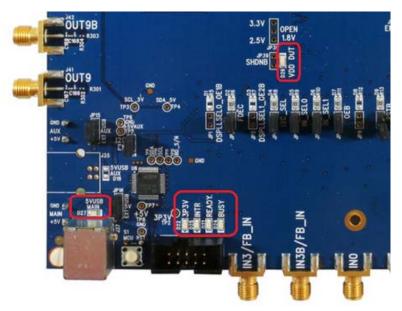


Figure 3. Status LEDs



## 6. Clock Input Circuits (INx/INxB and FB\_IN/FB\_INB)

The Si5341-D-EB has eight SMA connectors (IN0/IN0B–IN2/IN3B and FB\_IN/FB\_INB) for receiving external clock signals. All input clocks are terminated as shown in Figure 4 below. Note input clocks are ac-coupled and 50  $\Omega$  terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5341 data sheet.

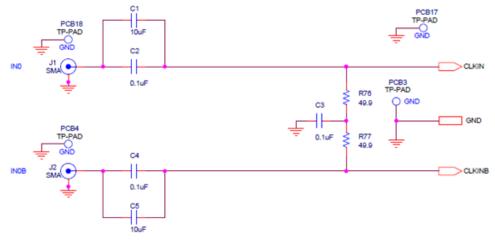


Figure 4. Input Clock Termination Circuit

## 7. Clock Output Circuits (OUTx/OUTxB)

Each of the twenty output drivers (10 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 5 below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5341-D-EVB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5341-D-EB and provide locations on the PCB for optional dc/ac terminations by the end user.

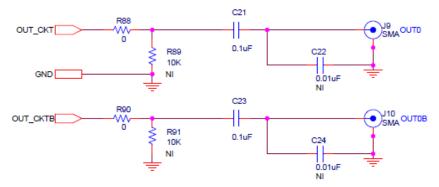


Figure 5. Output Clock Termination Circuit



## 8. Installing ClockBuilder Pro Desktop Software

To install the CBOPro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/CBPro and download ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above. Please follow the instructions as indicated.

## 9. Using the Si5341-D-EVB

## 9.1. Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the evaluation board with a USB cable as shown below.

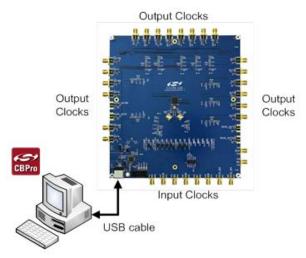


Figure 6. EVB Connection Diagram



## 9.2. Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is not needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5341-D-EB schematic for details.

The Si5341-EB comes preconfigured with jumpers installed at JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

Figure 7 shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

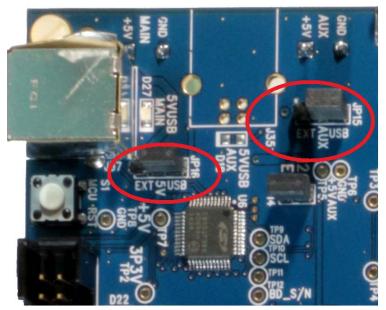


Figure 7. JP15-JP16 Standard Jumper Shunt Installation

Errata Note:Some early versions of the 64-pin Si534x-EBs may have the silkscreen text at JP15-JP16 reversed regarding EXT and USB, i.e., USB EXT instead of EXT USB. Regardless, the correct installation of the jumper shunts for default or standard operation is on the right hand side as read and viewed in Figure 7.

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, re-configure the EB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
  - Connect external +5 V power supply to terminal block J33 on the back side of the PCB.
  - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.



## 9.3. Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro. The ClockBuilder Pro installer will install **two** main applications:



#### Figure 8. Application #1: ClockBuilder Pro Wizard

#### Use the CBPro Wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

	-00-15-77-8F-BD - ClockB	uilder Pro	. I manual	Annale Spensor	madent maning	1 1000	
File Help							
Info DUT SPI I	2C DUT Register Editor	Regulators All	Voltages GPIO	Status Reg	isters		Control Registers
VDD	1.80V 🔽 On	Voltage	Current	Power	Read		Soft Reset and Calibration SOFT_RST
VDDA	On	v	A	W	Read		Hard Reset, Sync, & Power Down
VDDO0 VDDO1	2.50V On On On	V V	A A	w w	Read		HARD_RST
VDDO2	2.50V 🔽 On	v	A	W	Read		SYNC PDN: 0
VDDO3 VDDO4	2.50V <b>On</b> 2.50V <b>On</b>	V	A A	w w	Read Read		Frequency Adjust
VDDO5 VDDO6	2.50V <b>On</b> 2.50V <b>On</b>	v	A A	W	Read		FINC
VDD08	2.50V On On	V	A	W	Read		
VDDO8 VDDO9	2.50V  On	V	A A	w	Read		
All Output		Total	A	W	Read All		
Supplies –	Power On Power C	Com	pare Design Estir	mates to Mea	asurements		

Figure 9. Application #2: EVB GUI

#### Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5341)
- Control the EVB's regulators
- Monitor voltage, current, power on the EVB



### 9.4. Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5341-D-EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

#### 9.5. Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.



#### Figure 10. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.



#### Figure 11. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.

CIOCK	Builder Pro v0.104
0	Write Design to EVB? The EVB may be out-of-sync with your design. Would you like to write your design to the EVB?
	Ves No

#### Figure 12. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5341 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.



CB Si5341 Design Write	
Writing Si5341 Design to EVB Address 0x0119	

Figure 13. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.

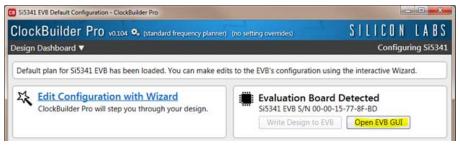


Figure 14. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown below.

le Help						
nfo DUT SPI I2	C DUT Register E	ditor Regulators	All Voltages	GPIO	Status Registers	;
		Voltage	Curre	nt	Power	
VDD	1.80V 🔽 🖸	n 1.306 V	488	mA	637 mW	Read
VDDA	0	n 3.294 V	/ 112	mA	369 mW	Read
VDD00	2.50V	n 2.514 V	/ 14	mA	35 mW	Read
VDDO1	2.50V 🔽 🖸	n 2.500 V	/ 17	mA	43 mW	Read
VDDO2	2.50V	n 2.507 V	/ 14	mA	35 mW	Read
VDDO3	2.50V	n 2.496 V	/ 14	mA	35 mW	Read
VDDO4	2.50V	n 2.499 V	/ 15	mA	37 mW	Read
VDDO5	2.50V	n 2.501 V	/ 16	mA	40 mW	Read
VDDO6	2.50V	n 2.504 V	/ 14	mA	35 mW	Read
VDD07	2.50V	n 2.485 V	/ 14	mA	35 mW	Read
VDDO8	2.50V	n 2.500 V	/ 14	mA	35 mW	Read
VDDO9	2.50V	n 2.490 V	/ 16	mA	40 mW	Read
All Output	Select Voltage	Total	748	mA	1.376 W	Read A

Figure 15. EVB GUI Window



#### 9.5.1. Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting "Off" then "On" of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wiz-ard's main menu and select "Write Design to EVB":

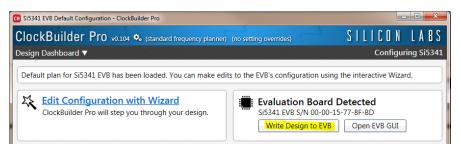


Figure 16. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

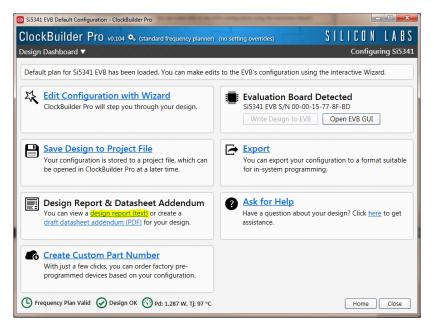


Figure 17. View Design Report



Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

Host Interface: I/O Power Supply: VDD (Core) SPI Mode: 4-Wire IZC Address Range: 116d to 119d / 0x74 to 0x77 (selected via A0/A1 pins) XA/XE: 48 MHz (XTAL - Crystal) Inputs: IND: 48 MHz Differential IN1: 48 MHz Differential IN2: 48 MHz Differential IN2: 48 MHz Differential	Design Repo	rt	
<pre>Si5341D 100 Hz to 350 MHz " * Based on your calculated frequency plan, a Si5341A grade device is required for your design. See the datasheet Ordering Guide for more information. Design ====== Host Interface: I/O Power Supply: VDD (Core) SPI Mode: 4-Wire I2C Address Range: 116d to 119d / 0x74 to 0x77 (selected via A0/A1 pins) XA/XB: 48 MHz (XTAL - Crystal) Inputs IND: 48 MHz Differential IN1: 48 MHz Differential IN2: 48 MHz Differential Outputs: OUT0: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT2: 162.5 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT3: 163.041015625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/</pre>	S15341B	100 Hz to 350 MHz "	
<pre>** Based on your calculated frequency plan, a Si5341A grade device is *required for your design. See the datasheet Ordering Guide for more information. Design ===== Host Interface: I/O Power Supply: VDD (Core) SFI Mode: 4-Wire I2C Address Range: 116d to 119d / 0x74 to 0x77 (selected via A0/A1 pins) XA/XE: 48 MHz (XTAL - Crystal) IND: 48 MHz Differential IND: 48 MHz Differential IND: 48 MHz Differential IND: 48 MHz Differential IND: 48 MHz OUTD: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 61.61.4025 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT3: 61.61.4025 MHz [ 168 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 55 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT5: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/28 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/32 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/32 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/32 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/32 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/32 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/32 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/32 MHz ] Enabled, LVDS 2.5 V OUT6: 174.703083700405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V OU</pre>			
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<pre>SPI Mode: 4-Wire I2C Address Range: 116d to 119d / 0x74 to 0x77 (selected via A0/A1 pins) XA/XB: 48 MHz (XTAL - Crystal) Inputs IN0: 48 MHz Differential IN1: 48 MHz Differential IN2: 48 MHz Differential IN2: 48 MHz Differential OUTD: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 162.5 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 15.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT5: 62.08 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT5: 62.08 MHz [ 162 + 2/25 MHz ]</pre>	Host Inte	rface:	
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<pre>Inputs: IN0: 48 MHz Differential IN1: 48 MHz Differential IN2: 48 MHz Differential Outputs: OUT0: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.040105625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 174.703083700405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V</pre>		(XTAL - Crystal)	
<pre>ING: 48 MHz Differential INI: 48 MHz Differential N2: 48 MHz Differential Outputs: OUTO: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUTI: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 160.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V</pre>		(mini orgovar)	
Differential IN1: 48 MHz Differential IN2: 48 MHz Differential OUT0: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.703083700405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT5: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 622 + 2/25 MHz ]			
<pre>IN1: 48 MHz Differential IN2: 48 MHz Differential Outputs: OUT0: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 160.94015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 167 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT5: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 155.52 MHz [ 152 + 2/25 MHz ]</pre>	INO:		
Differential IN2: 48 MHz Differential OUTD: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT5: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT3: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V			
<pre>IN2: 48 MHz Differential Outputs: OUT0: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 161.041015&amp;25 MHz [ 68 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 572.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT6: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT6: 22.08 MHz [ 622 + 2/25 MHz ]</pre>	IN1:		
Differential Outputs: OUTO: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 174.703083700405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT5: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V	TNO.		
Outputs: OUT0: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT0: 1625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 163.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 154.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]	INZ:		
OUT0: 161.1328125 MHz [ 161 + 17/128 MHz ] Enabled, LVDS 2.5 V OUT1: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V			
Enabled, LVDS 2.5 V OUT1: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT5: 160.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 072.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 022.08 MHz [ 622 + 2/25 MHz ]	Outputs:		
<pre>OUT1: 625 MHz Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT6: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 622 + 2/25 MHz ]</pre>	OUTO:		
Enabled, LVDS 2.5 V OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT6: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V			
<pre>OUT2: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 252.08 MHz [ 622 + 2/25 MHz ]</pre>	OUT1:		
Enabled, LVDS 2.5 V OUTS: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT6: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 155.52 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V	01170		
<pre>OUT3: 156.25 MHz [ 156 + 1/4 MHz ] Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT6: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]</pre>	0012:		
Enabled, LVDS 2.5 V OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT5: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 22.08 MHz [ 622 + 2/25 MHz ] Enabled, LVDS 2.5 V	OUT3.		
<pre>OUT4: 168.041015625 MHz [ 168 + 21/512 MHz ] Enabled, LVDS 2.5 V OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT6: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]</pre>	0010.		
OUT5: 672.1640625 MHz [ 672 + 21/128 MHz ] Enabled, LVDS 2.5 V OUT6: 174.703087004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]	OUT4:		
Enabled, LVDS 2.5 V OUT6: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]		Enabled, LVDS 2.5 V	
OUT6: 174.7030837004405286 MHz [ 174 + 798/1135 MHz ] Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]	OUT5:	672.1640625 MHz [ 672 + 21/128 MHz ]	
Enabled, LVDS 2.5 V OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]			
OUT7: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]	OUT6:		
Enabled, LVDS 2.5 V OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]	OUT -		
OUT8: 155.52 MHz [ 155 + 13/25 MHz ] Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]	0017:		
Enabled, LVDS 2.5 V OUT9: 622.08 MHz [ 622 + 2/25 MHz ]	OUT8 :		
OUT9: 622.08 MHz [ 622 + 2/25 MHz ]			
	OUT9:		
			Ŧ

Figure 18. Design Report Window

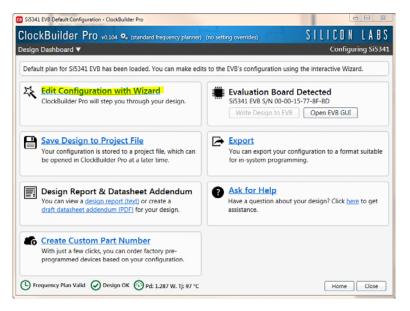
#### 9.5.2. Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.



9.6. Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on Edit Configuration with Wizard:



#### Figure 19. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

n 1 of 8 - Des	ian ID & Notes 🔻	Configuring Si5
esign ID		
he device has 8 r	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/rev	ision identifier.
esign ID:	5341EVB1 (optional; max 8 characters)	
	The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN_ID	07.
adding Mode:	NULL Padded If you do not enter the full 8 characters, the reamining bytes of DESIGN_IDx will be padde character).	ed with 0x00 bytes (aka NULL
	<ul> <li>Space Padded If you do not enter the full 8 characters, the reamining bytes of DESIGN_IDx will be padde character).</li> </ul>	ed with 0x20 bytes (space
lesian Notes		
esign Notes inter anything you	u want here. The text is stored in your project file and included in design reports (future feature).	
5	u want here. The text is stored in your project file and included in design reports (future feature).	
5	u want here. The text is stored in your project file and included in design reports (future feature).	

Figure 20. Design Wizard



Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

CB Si5341 Design Write	
Writing Si5341 Design to EVB Address 0x0119	

Figure 21. Writing Design Status

#### 9.7. Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

ClockBuilder Pro Wizard - Silicon Labs	
SILICON LABS We Make Timing Simp	0
Work With a Design	Quick Links
Create New Design	Jitter Attenuator Clock Products
🖶 Open Design Project File	Knowledge Base Custom Part Number Lookup ClockBuilder Go iOS App
ex <u>Open Sample Design</u>	
Evaluation Board Detected Si5341 EVB Open Default Plan Open EVB GUI	
Quick Tools	
Export Configuration	
	A Brit
O <sub>o</sub> Preferences	Version 0.104 Built on 7/17/2014

Figure 22. Open Design Project File



# Si5341-D-EVB

Locate your CBPro design file (\*.slabtimeproj or \*.sitproj file).design file in the Windows file browser.

Irganize • New folder				51 .		6
Favorites	Name	Date modified	Type	Size		
E Desktop	55341-EV8.slabtimeproj	6/30/2014 1:29 PM	Silcon Labs Timin		3 KB	
Downloads	S5345-EVB.slabtimeproj	6/30/2014 1:29 PM	Silicon Labs Timin		3.KB	
M Recent Places	SiS347.slabtimeproj	6/30/2014 1:29 PM	Silicon Labs Timin		3 KB	
🙀 Libraries						
Computer						
Kocal Disk (C:)						
😴 muanwar (\\silabs.c						
😪 muanwar (\\silabs.c						
CharacterizationVali						
Vetwork						

Figure 23. Browse to Project File

Select Yes when the WRITE DESIGN to EVB popup appears:



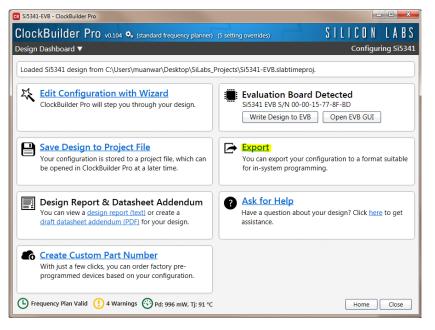
Figure 24. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.



#### 9.8. Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:



#### Figure 25. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

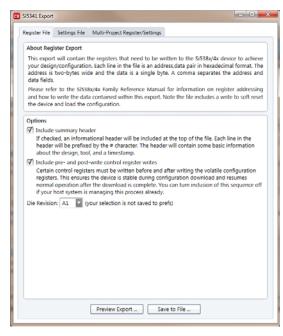


Figure 26. Export Settings



# 10. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

**Note:** Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5341 using Clock-Builder Pro on the Si5341-D-EB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5341 RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

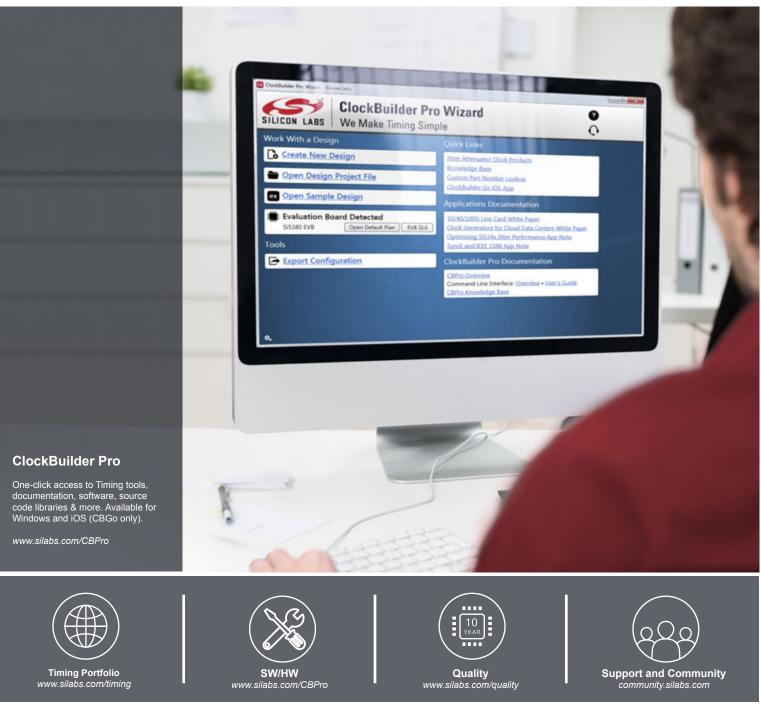
## 11. Si5341-D-EVB Schematic and Bill of Materials (BOM)

The Si5341-D-EVB Schematic and Bill of Materials (BOM) can be found online at

http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

Note: Please be aware that the Si5341-D-EB schematic is in **OrCad Capture** *hierarchical format* and not in a typical "flat" schematic format.





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