

UG149: Si5344H Evaluation Board User's Guide

The Si5344H-EVB is used for evaluating the Si5344H Any-Frequency, Any-Output, Jitter Attenuating Clock Multiplier. The Si5344H combines 4th generation DSPLL and Multisynth[™] technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance. The Si5344H-EVB has two independent input clocks and four independent output clocks. The Si5344H-EVB can be controlled and configured using the ClockBuilder[®] Pro (CBPro) software tool.



Si5344H Evaluation Board

EVB FEATURES:

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL or Reference SMA Inputs allow holdover mode of operation on the Si5344H.
- CBPro GUI-programmable VDD supply allows the device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI-programmable VDDO supplies allow each of the ten outputs to have its own supply voltage, selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies.
- Status LEDs for power supplies and control/status signals of Si5344H.
- SMA connectors for input clocks, output clocks, and optional external timing reference clock.

UG149: Si5344H Evaluation Board User's Guide • Overview

1. Overview

1.1 Functional Block Diagram

A functional block diagram of the Si5344H-EVB is shown below. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See Section 1.2 Si5344H EVB Support Documentation or Section 1.3 Quick Start for more information.

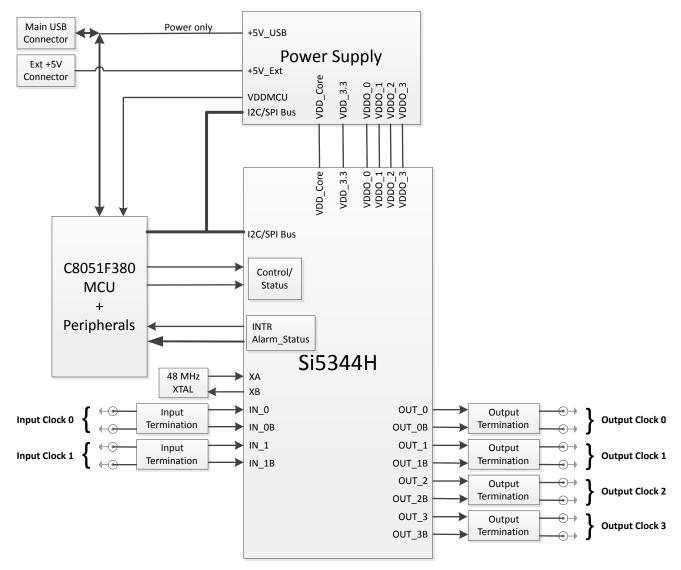


Figure 1.1. Si5344H-EVB Functional Block Diagram

1.2 Si5344H EVB Support Documentation

The Si5344H EVB Schematic and Bill of Materials (BOM) can be found online at: http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx. Contact Silicon labs for related user's guides, data sheets, and software.

Note: The Si5344H EVB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

UG149: Si5344H Evaluation Board User's Guide • Overview

1.3 Quick Start

- 1. Install ClockBuilder Pro desktop software: http://www.silabs.com/CBPro.
 - Installation instructions and the user's guide for ClockBuilder Pro can also be found at the download link shown above.
- 2. Connect a USB cable from the Si5344H-EVB to the PC where the software is installed.
- 3. Confirm jumpers are installed as shown in Table 1.1 Si5344H EVB Jumper Defaults on page 3.
- 4. Launch the ClockBuilder Pro software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5344H-EVB.
- 6. Contact Silicon Labs for the Si5344H data sheet.

1.4 Jumper Defaults

Location	Туре	I = Installed	Location	Туре	I = Installed
		0 = Open			0 = Open
JP1	2 pin	I	JP14	2 pin	0
JP2	2 pin	I	JP15	2 pin	0
JP3	2 pin	I	JP16	3 pin	all open
JP4	2 pin	I	JP17	3 pin	all open
JP5	3 pin	1 to 2	JP18	2 pin	0
JP6	2 pin	0	JP19	2 pin	0
JP7	2 pin	0	JP20	3 pin	all open
JP8	2 pin	0	JP21	3 pin	all open
JP9	2 pin	0	JP22	2 pin	0
JP10	2 pin	0	JP23	2 pin	0
JP11	2 pin	0	JP24	3 pin	all open
JP12	2 pin	0			
JP13	2 pin	0	JP17	5x2 Hdr	All 5 installed

Table 1.1. Si5344H EVB Jumper Defaults

Note:

1. Refer to the Si5344H EVB Schematics for the functionality associated with each jumper.

1.5 Status LEDs

Location	Silkscreen	Color	Status Function Indication
D5	INTRB	Blue	DUT Interrupt
D7	LOLB	Blue	DUT Loss of Lock
D8	LOSXAXBB	Blue	DUT Loss of Reference
D11	+5V MAIN	Green	Main USB +5 V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

Table 1.2. Si5344H EVB Status LEDs

D11 is illuminated when USB +5 V supply voltage is present. D12 and D13 are status LEDs showing on-board MCU activity.

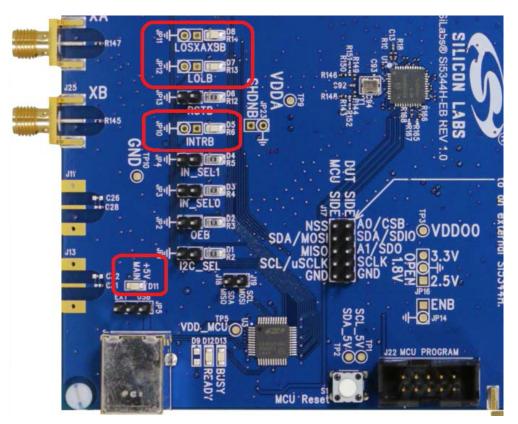


Figure 1.2. Status LEDs

1.6 External Reference Input (XA/XB)

An external reference (XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5344H-EVB can also accommodate an external reference clock instead of a crystal. To evaluate the device with a REFCLK, C93 and C94 must be populated and the XTAL removed (see the figure below). The REFCLK can then be applied to J25 and J26.

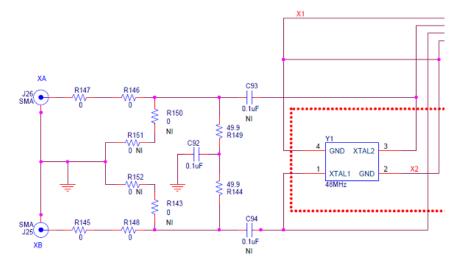


Figure 1.3. External Reference Input Circuit

1.7 Clock Input Circuits (INx/INxB and FB-IN/FB-INB)

The Si5344H-EVB has four SMA connectors (IN0/IN0B and IN1/IN1B) for receiving external clock signals. All input clocks are terminated, as shown in the figure below.

Input clocks are AC coupled and 50 W terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. See the Si5344H data sheet for details on how to configure inputs as single-ended.

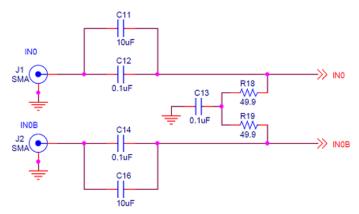


Figure 1.4. Input Clock Termination Circuit

1.8 Clock Output Circuits (OUTx/OUTxB)

Each of the eight outputs (four differential pairs) is AC coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal has no DC bias. If DC coupling is required, the AC coupling capacitors can be replaced with a resistor of appropriate value. The Si5344H-EVB provides pads for optional output termination resistors and/or low frequency capacitors.

Note: Components with schematic "NI" designation are not normally populated on the Si5344H-EVB and provide locations on the PCB for optional DC/AC terminations by the end user.

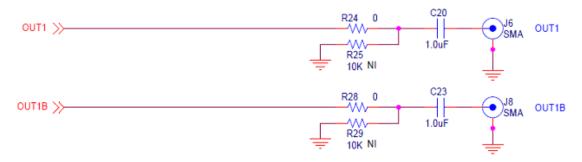


Figure 1.5. Output Clock Termination Circuit

2. Using Si5344H EVB

2.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect the software to the EVB with a USB cable, as shown in the figure below.

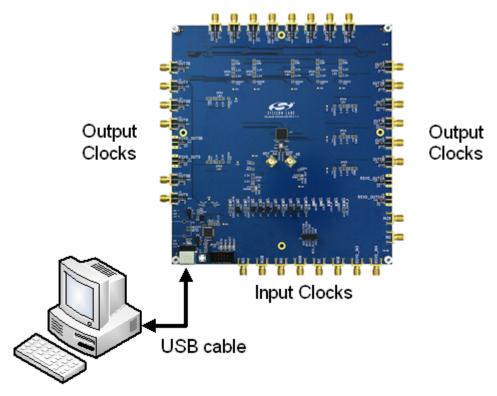


Figure 2.1. EVB Connection Diagram

2.2 Main Features of ClockBuilder Pro Applications

The ClockBuilder Pro installer installs two main applications: the ClockBuilder Pro Wizard and the EVB GUI.

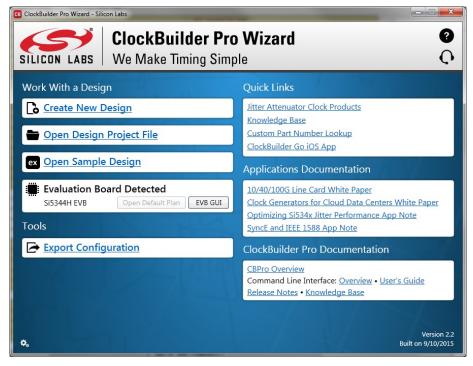


Figure 2.2. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to do the following:

- · Create a new design.
- · Review or edit an existing design.
- · Export: create in-system programming.

ile	Help							
Info	DUT SPI	I2C	DUT Register Editor	Regulators	All Voltages	GPIO	Status Register	s
				Voltage	Curre	nt	Power	
	VD	D 1.	80V 🔽 On	V		A	W	Read
	VDD	A	On	v		A	W	Read
	VDDC	00 1.	80V 🔽 🔽 O	₩ V		A	w	Read
	VDDC	01 1.	80V 🔽 🚺 O	₩ V		А	w	Read
	VDDC	02 1.	80V 🔽 🚺 O	₩ V		A	w	Read
	VDDC	3 1.	80V 🔽 🚺 O	₩ V		A	w	Read
	Output		elect Voltage	Total		A	w	Read All
	Supplies -		ower On Power C	off C	Compare Desig	gn Estin	nates to Measur	ements

Figure 2.3. Application #2: EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5344H).
- Control the EVB's regulators.
- Monitor voltage, current, power on the EVB.

2.3 Common ClockBuilder Pro Workflow Scenarios

There are three common workflow scenarios when using CBPro and the Si5344H EVB. These workflow scenarios are as follows:

Workflow Scenario #1:	Testing a Silicon Labs-created Default Configuration
Workflow Scenario #2:	Modifying the Default Silicon Labs-created Device Configuration
Workflow Scenario #3:	Testing a User-created Device Configuration

Each scenario is described in more detail in the following sections.

2.3.1 Workflow Scenario #1: Testing a Silicon Labs Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

1. Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.



Figure 2.4. ClockBuilder Pro Desktop Icon

When the EVB is detected, select the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

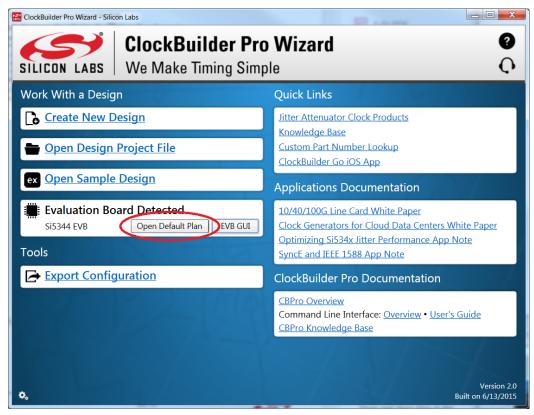


Figure 2.5. Open Default Plan

3. Once you open the default plan (based on your EVB model number), a popup window opens.

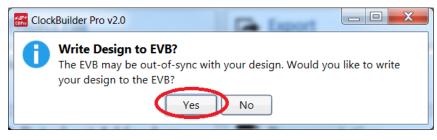


Figure 2.6. Write Design to EVB Dialog

4. Select "Yes" to write the default plan to the Si5344H device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.



Figure 2.7. Writing Design Status

5. After CBPro writes the default plan to the EVB, select "Open EVB GUI".

CB New Si5344H Design - ClockBuilder Pro	
ClockBuilder Pro v2.2 🍫 (standard frequency planner) (no	setting overrides) SILICON LABS
Design Dashboard 🔻	Configuring Si5344H
You have not finished your Si5344H design. You can save your de continue later. Or, click one of the links in the the "Edit Configura	
Edit Configuration with Wizard Design ID & Notes · Host Interface · XA/XB · Inputs · Input Select · Outputs · Output Skew · Output Drivers · DSPLL · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5344 EVB S/N 00-00-16-B1-A9-E4 Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation Technical documentation is currently restricted for this product. Please contact your <u>Silicon Labs sales</u> <u>representative</u> to request access to documentation.
With just a few clicks, you can order factory pre- programmed devices based on your configuration.	Ask for Help Have a question about your design? Click here to get assistance.
🕒 Frequency Plan Valid 📀 Design OK 😚 Pd: 663 mW, Tj: 85 °C	Home Close

Figure 2.8. Open EVB GUI

6. The EVB GUI opens. All power supplies are set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown in the figure below.

ile	Help			s				
Info	DUT SPI	I2C	DUT Register Editor	Regulators	All Voltages	GPIO	Status Register	s
				Voltage	Curre	nt	Power	
	VD	D 1.	80V 🔽 On	v		А	W	Read
	VDD	А	On	v		А	w	Read
	VDDO	0 1.	80V 📘 🔤	off V		А	W	Read
	VDDO	1 1.	80V 🔽 🚺	off V		А	w	Read
	VDDO	2 1.	80V 🔽 🚺	Off V		A	w	Read
	VDDO	3 1.	80V 📘 🔤	off V		A	w	Read
	Output		elect Voltage	Total		А	w	Read All

Figure 2.9. EVB GUI Window

Verify Free-run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the "Read All" button (bottom right-hand corner of Figure 2.9 EVB GUI Window on page 12) and then reviewing the voltage, current, and power readings for each VDDx supply.

Note: Shutting the VDD and VDDA power supplies "Off" and then "On" will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB".

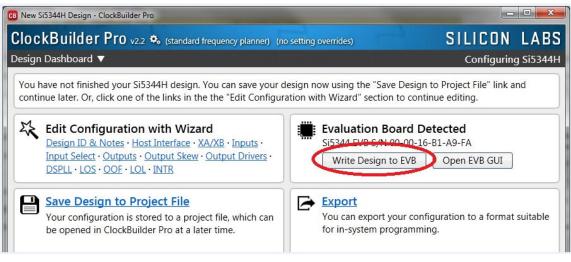


Figure 2.10. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running in free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on "View Design Report" as highlighted in the figure below.

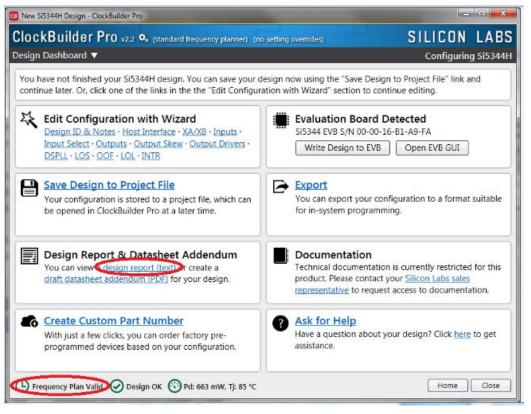


Figure 2.11. View Design Report

Your configuration's design report opens in a new window, as shown in the figure below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

<pre>48 MHz (XTAL - Crystal) Inputs: IN0: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused Utputs OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Plan Fprd = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fprd = 80 kHz Frao = 2.026 GHz [2 + 13/500 GHz] Fns1 = 312 MHz P dividers: F0 = 243 F1 = Unused F1 = Unuse F1 = Unused F1 = Unused F1 = Unused F1 = Unused F1 = Unused</pre>	Si5344H Frequency Plan	_ 0 _X
<pre>Timestamp: 2015-09-28 14:42:50 GMT-05:00 Design Rule Check Errors: - No errors Warnings Design Design Use 1-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) XX/XB: 48 MHz (XTAL - Crystal) Inputs: IN: Unused Vituats: Use 18 MHz [19 + 11/25 MHz] Enabled, LVDS 2.5 V OUT1: 15 MHz Enabled, LVDS 2.5 V OUT2: Unused Frequency Plan Ppfai = 48 MHz Frequency Plan Ppfai = 48 MHz Frequency Plan Ppfai = 48 MHz Proc = 14.182 GHz [14 + 91/500 GHz] Frequency Plan Ppfai = 48 MHz Proc = 14.182 GHz [14 + 91/500 GHz] Pinal = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 NCANB = 295.458333333333333 [295 + 11/24] N = 35455 N dividers: N0: N0: Value: 7 Skew: 0.000 s V V Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s V V V V V V V V V V V V V V V V V V V</pre>	equency Plan Result	
Design Rule Check Errors: - No errors Warnings: - No warnings Design Hoss Interface: I/O FOwer Supply: VDD (Core) SFI Mode: 4-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/Al pins) XA/XB: 48 MHz (XTAL - Crystal) Imputs: TMO: 19.44 MHz [19 + 11/25 MHz] Standard INI: Unused DUTO: 2.026 GHz [2 + 13/500 GHz] Enabled, LUDS 2.5 V OUT1: 156 MHz Enabled, LUDS 2.5 V OUT2: Unused OUT3: Unused Frequency Flan Frequency Flan Frequency Flan Frequency Flan Ppfd1 = 48 MHz Frequency Flan Ppfd1 = 48.2 GHz [14 + 91/500 GHz] Fprd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fpfd = 80 kHz P dividers: P0 = 243 P1 = Juneed Pxxxb = 1 WXMXB = 295.458333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s	Treated By: ClockBuilder Pro v2.2 [2015-09-10]	
<pre>Errors: - No errors Warnings: - No warnings Design Most Interface: I/O Fover Supply: VDD (Core) SFI Mode: 4-Mire IZC Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/Al pins) XA/XB: 48 MHz (XTAL - Crystal) Inputs) IN0: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused DUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Fian From = 14.132 GHz [14 + 91/500 GHz] Fprom = 14.132 GHz [14 + 91/500 GHz] Fprom = 14.132 GHz [14 + 91/500 GHz] Fprom = 14.132 GHz [14 + 91/500 GHz] Fprom = 14.132 GHz [14 + 91/500 GHz] Fprom = 14.132 GHz [2 + 13/500 GHz] Fprom = 14.132 GHz [2 + 13/500 GHz] Fprom = 14.132 GHz [2 + 13/500 GHz] MCAXB = 295.458333333333333 [295 + 11/24] MCAXB = 295.4583333333333333 [295 + 11/24] MCAXB = 295.45833333333333333 [45 + 71/156] Skew: 0.000 s Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s</pre>	imestamp: 2015-09-28 14:42:50 GMT-05:00	1
<pre>Errors: - No errors Warnings Design </pre>		
- No errors Warnings: - No warnings Design Host Interface: I/O Fover Supply: VDD (Core) SFI Mode: 4-Wire IZC Address Range: 104d to 107d / 0x68 to 0x6B (selected via AO/Al pins) XA/XB: 48 MHz (XTAL - Crystal) Inputs: INC: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused Unused Unused Unused Unused Project = 48 MHz Frequency Plan Fpfdi = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fpfdi = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pack = 1 NXXMB = 295.4583333333333 [295 + 11/24] NCXMB = 295.45833333333333 [295 + 11/24] NCXMB = 295.458333333333333 [45 + 71/156] Skew: 0.000 s		
<pre>Warnings - No warnings Design </pre>	irrors:	
- No warnings Design Host Interface: I/O Power Supply: VDD (Core) SFI Mode: 4-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) XA/XE: 48 MHz (XTAL - Crystal) INU: INU: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused UID: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused UID: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUTI: 156 MHz Enabled, LVDS 2.5 V OUTI: 156 MHz Enabled, LVDS 2.5 V OUTI: Unused Frequency Plan Fpfdi = 48 MHz Froco = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 KHz Fns0 = 2.026 GHz [2 + 13/500 GHz] Fns1 = 312 MHz P dividers: P0 = 243 P1 = Unused Fxakb = 1 NNARB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: NO: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] NI: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] NI: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] NI: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s	No errors	
<pre>Design Host Interface: I/O Power Supply: VDD (Core) SFI Mode: 4-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/Al pins) XA/XE: 48 MHz (XTAL - Crystal) Inputs IN0: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused Inputs OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Flan FFrid = 40 MHz Froco = 14.182 GHz [14 + 91/500 GHz] Frol = 40 KHz Ens0 = 2.026 GHz [2 + 13/500 GHz] Frs1 = 312 MHz P dividers: P0 = 243 P1 = Unused Fxaxb = 1 NXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1:</pre>	Varnings:	
Host Interface: I/O Power Supply: VDD (Core) SPI Mode: 4-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) XA/XB: 48 MHz (XTAL - Crystal) Inputs: IND: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused Upputs: OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Flan Ppfdi = 40 MHz Freo = 14.182 GHz [14 + 91/500 GHz] Frei = 40 MHz Proc = 14.182 GHz [14 + 91/500 GHz] Fnsl = 312 MHz P dividers: PO = 243 P1 = Unused Fxaxb = 1 XXAXB = 295.458333333333333 [295 + 11/24] M = 35455 N dividers: NO: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] NI: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s	No warnings	
<pre>Host Interface: I/O Power Supply: VDD (Core) SPI Mode: 4-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6E (selected via A0/Al pins) XA/XB: 48 MHz (XTAL - Crystal) Inputs) ref0: 19.44 MHz [19 + 11/25 MHz] Standard IN: Unused Urputs) OUTO: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT1: Unused OUT2: Unused Frequency Plan Frequency Plan TPFore = 14.182 GHz [14 + 91/500 GHz] Fns1 = 312 MHz P dividers: Po = 243 P1 = Unused Fxazb = 1 NXAXB = 295.458333333333333 [295 + 11/24] MXAXB = 295.4583333333333333 [295 + 11/24] MXAXB = 295.4583333333333333 [295 + 11/24] MXAXB = 295.45833333333333333 [295 + 11/24] MXAXB = 295.45833333333333333 [295 + 11/24] MXAXB = 295.45833333333333333 [295 + 11/24] MXAXB = 295.458333333333333333 [295 + 11/24] M = 35455 NO: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] Ni: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s</pre>		
<pre>I/O Power Supply: VDD (Core) SPI Mode: 4-Wire SPI Mode: 4-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) XX/XB: 48 MHz (XTAL - Crystal) Inputs IN1: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused Utputs OUT: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT2: Unused Prequency Plan Ppfdi = 48 MHz Frequency Plan Ppfdi = 48 MHz Frequency Plan Ppfdi = 48 MHz Proc = 14.182 GHz [14 + 91/500 GHz] Fns0 = 2.026 GHz [2 + 13/500 GHz] Fns1 = 312 MHz P dividers: P0 = 243 P1 = Unused Frank = 1 NXAXE = 295.45833333333333 [295 + 11/24] M = 35455 N' Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s OUT0 selector of the context of</pre>		
<pre>I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) XA/XB: 48 MHz (XTAL - Crystal) Inputs) IND: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused IN1: Unused Intputs) OUT: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused Frequency Plan Fpfdi = 48 MHz Frod = 80 KHz Fns0 = 2.026 GHz [2 + 13/500 GHz] Fns1 = 312 MHz P dividers: P0 = 243 P1 = Unused Faxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 NO: Value: 7 Skew: 0.000 s UT2 Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] Skew: 0.000 s UT2 Value: 45.4551282051 [45 + 71/156] </pre>	I/O Power Supply: VDD (Core)	
<pre>XA/XB: 48 MHz (XTAL - Crystal) inputs: TNO: 19.44 MHz [19 + 11/25 MHz] Standard INI: Unused UDTO: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Plan Ppfd = 48 MHz Froco = 14.182 GHz [14 + 91/500 GHz] Prfd = 80 kHz Fns0 = 2.026 GHz [2 + 13/500 GHz] Pms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 NXXXB = 295.458333333333333 [295 + 11/24] MXAXB = 295.458333333333333 [295 + 11/24] MXAXB = 295.4583333333333333 [295 + 11/24] MXXB = 295.45833333333333333 [295 + 11/24] Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s Value: 45.4551282051282051 [45 + 71/156] Value: 45.4551282051282051 [45 + 71/156] Value: 45.4551282051.</pre>		
<pre>48 MHz (XTAL - Crystal) Inputs: IN0: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused Utputs OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Plan Fprd = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fprd = 80 kHz Frao = 2.026 GHz [2 + 13/500 GHz] Fns1 = 312 MHz P dividers: F0 = 243 F1 = Unused F1 = Unuse F1 = Unused F1 = Unused F1 = Unused F1 = Unused F1 = Unused</pre>	I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pi	lns)
<pre>Inputs Inputs Inputs Standard IN1: Unused Utputs OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused Frequency Plan Ppfdi = 48 MHz Fvco = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 KHz Fns0 = 2.026 GHz [2 + 13/500 GHz] Fns1 = 312 MHz P dividers: P0 = 243 P1 = Unused Fxaxb = 1 MXAXB = 295.458333333333333 [295 + 11/24] M = 35455 N dividers: NO: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s</pre>	CA/XB:	
<pre>INU: 19.44 MHz [19 + 11/25 MHz] Standard INI: Unused Utput OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Plan Frod = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Fxaxb = 1 MXXXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>	48 MHz (XTAL - Crystal)	
<pre>INU: 19.44 MHz [19 + 11/25 MHz] Standard IN1: Unused UtputD OUTO: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Plan Frod = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fras0 = 2.026 GHz [2 + 13/500 GHz] Fmal = 312 MHz P dividers: PO = 243 P1 = Unused Fraxb = 1 MXXXB = 295.458333333333333 [295 + 11/24] M = 35455 N dividers: NO: Value: 7 Skew: 0.000 s UUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>	Inputs:	
<pre>Standard IN1: Unused Unput: OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Plan Froco = 14.182 GHz [14 + 91/500 GHz] Frod = 80 kHz Fns0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 7 Skew: 0.000 s</pre>		
Durputs Outo: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused Frequency Plan Fpfd1 = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fprd = 80 kHz Fns0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXXXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused Frequency Plan Fpfd1 = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s	IN1: Unused	
OUT0: 2.026 GHz [2 + 13/500 GHz] Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused Frequency Plan Fpfd1 = 48 MHz Froo = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
Enabled, LVDS 2.5 V OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused Prequency Plan Frequency Plan Frequency Plan From 2.026 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fns0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Praxb = 1 MXAXB = 295.4583333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
OUT1: 156 MHz Enabled, LVDS 2.5 V OUT2: Unused Frequency Plan Froc = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
Enabled, LVDS 2.5 V OUT2: Unused OUT3: Unused Frequency Plan Fpfd1 = 48 MHz Froco = 14.182 GHz [14 + 91/500 GHz] Frfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUTD: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
OUT2: Unused OUT3: Unused Frequency Plan Fpfdi = 48 MHz Fpro = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXXXB = 295.4583333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
OUT3: Unused Frequency Plan Fpfd1 = 48 MHz Froco = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
<pre>Fpfdi = 48 MHz Fproc = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Fxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>		
<pre>Fpfdi = 48 MHz Fproo = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>	requency Plan	
<pre>Fvco = 14.182 GHz [14 + 91/500 GHz] Fpfd = 80 kfz Fpms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.45833333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>		
<pre>Fpfd = 80 kHz Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Fxaxb = 1 MXAXB = 295.458333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>	Ppfdi = 48 MHz	
<pre>Fms0 = 2.026 GHz [2 + 13/500 GHz] Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.4583333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s V </pre>	'vco = 14.182 GHz [14 + 91/500 GHz]	
<pre>Fms1 = 312 MHz P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.4583333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s v </pre>	'pfd = 80 kHz	
<pre>P dividers: P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.4583333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s</pre>		
P0 = 243 P1 = Unused Pxaxb = 1 MXAXB = 295.458333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s	ms1 = 312 MHz	
<pre>P1 = Unused Pxaxb = 1 MXAXB = 295.4583333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s</pre>		
<pre>Pxaxb = 1 MXAXB = 295.45833333333333333333 [295 + 11/24] M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>		
MXAXB = 295.458333333333333333 [295 + 11/24] M = 35455 N dividers: NO: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
<pre>M = 35455 N dividers: N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s </pre>	Pxaxb = 1	
N dividers: N0: Value: 7 Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
N0: Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
Value: 7 Skew: 0.000 s OUT0: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
Skew: 0.000 s OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
OUTO: 2.026 GHz [2 + 13/500 GHz] N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
N1: Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
Value: 45.4551282051282051 [45 + 71/156] Skew: 0.000 s		
Skew: 0.000 s		
	Copy to Clipboard Ask for Help	Close

Figure 2.12. Design Report Window

Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

2.3.2 Workflow Scenario #2: Modifying the Default Silicon Labs Created Device Configuration

1. To modify the "default" configuration using the CBPro Wizard, select "Edit Configuration with Wizard".

CB New Si5344H Design - ClockBuilder Pro	
ClockBuilder Pro v2.2 🌣 (standard frequency planner) (no	setting overrides) SILICON LABS
Design Dashboard 🔻	Configuring Si5344H
You have not finished your Si5344H design. You can save your de continue later. Or, click one of the links in the the "Edit Configura	
Edit configuration with Wizard Design ID & Notes · Host Interface · XA/XB · Inputs · Input Select · Outputs · Output Skew · Output Drivers · BCPLI · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5344 EVB S/N 00-00-16-B1-A9-FA Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a design report (text) or create a draft datasheet addendum (PDF) for your design.	Documentation Technical documentation is currently restricted for this product. Please contact your <u>Silicon Labs sales</u> <u>representative</u> to request access to documentation.
Create Custom Part Number With just a few clicks, you can order factory pre- programmed devices based on your configuration.	Ask for Help Have a question about your design? Click here to get assistance.
🕒 Frequency Plan Valid 🧭 Design OK 😚 Pd: 708 mW, Tj: 85 °C	Home Close

Figure 2.13. Edit Configuration with Wizard

2. You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

Si5344 EVB Default Configuration - Clo	:kBuilder Pro		
ClockBuilder Pro v2.0	🍫 (standard frequency planner) (no	setting overrides)	SILICON LABS
Step 1 of 14 - Design ID & Note	es 🗸		Configuring Si5344
Design ID The device has 8 registers, DESIGN_ Design ID: 5344EVB2	D0 through DESIGN_ID7, that can be u	sed to store a design/configuration/	'revision identifier.
Padding Mode:	enter here is stored as ASCII bytes in re led ot enter the full 8 characters, the remai		
character). O Space Pad			
	ext is stored in your project file and incl ports, you can use newlines to start a r		part number datasheet addendums.
Frequency Plan Valid 🕢 Des	ign OK 🛞 Pd: 877 mW, Tj: 89 °C	Write to EVEO < Back	Next > Finish Cancel

Figure 2.14. Design Wizard

Note: You can click on the icon on the lower left hand of the menu to confirm that your frequency plan is valid. After making your desired changes, you can click on "Write to EVB" to update the DUT to reconfigure your device in real-time. The Design Write status window opens each time you make a change.

Writing Si5344 Design to	D EVB	
Address 0x011E		

Figure 2.15. Writing Design Status

2.3.3 Workflow Scenario #3: Testing a User Created Device Configuration

1. To test a previously-created user configuration, open the CBPro Wizard by clicking the icon on your desktop and then selecting "Open Design Project File".

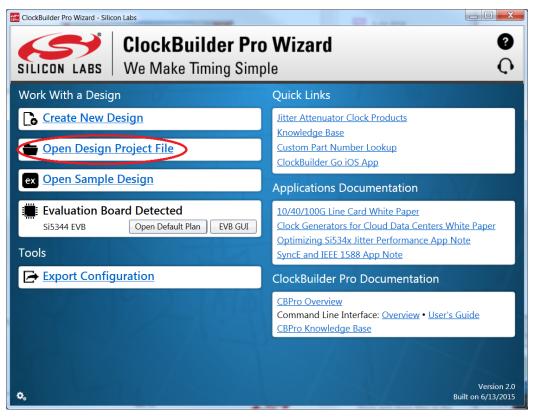


Figure 2.16. pen Design Project File

2. Locate your CBPro design file (*.slabtimeproj or *.sitproj file) design file in the Windows file browser.

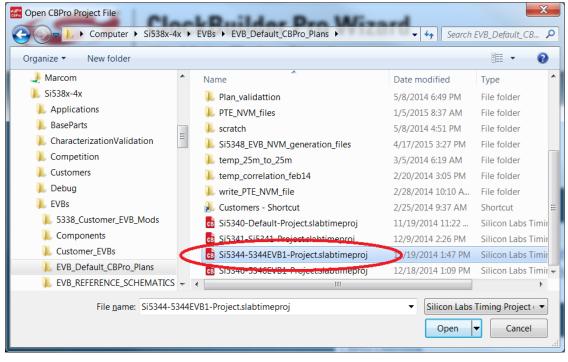


Figure 2.17. Browse to Project File

3. Select "Yes" when the WRITE DESIGN to EVB popup appears:

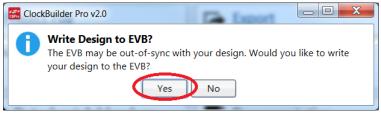


Figure 2.18. Write Design to EVB Dialog

4. The progress bar is launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

2.4 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export", as shown in the figure below.

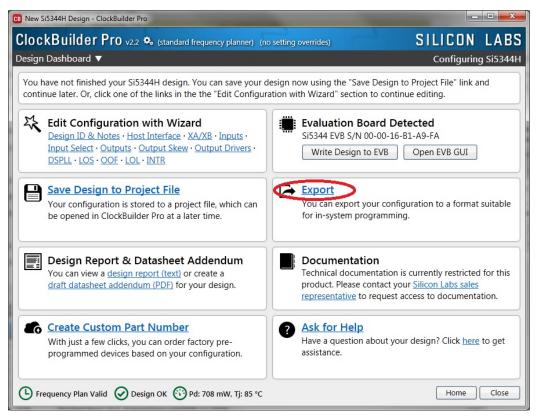


Figure 2.19. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

Si5344 Export	t		
Register File	Settings File	Multi-Project Register/Settings	
About Reg	jister Export		
your desig	n/configuration two-bytes with	the registers that need to be written to the Si n. Each line in the file is an address,data pair ir de and the data is a single byte. A comma s	h hexadecimal format. The
and how t		8x/4x Family Reference Manual for informatic a contained within this export. Note the file in configuration.	
Options			
If chec header	r will be prefixe	der ational header will be included at the top of th d by the # character. The header will contain s d, and a timestamp.	
Certair registe norma	n control regist rs. This ensure I operation afte	-write control register writes ers must be written before and after writing th s the device is stable during configuration dow er the download is complete. You can turn incl managing this process already.	nload and resumes
🗌 I am ta	rgeting pre-pr	oduction samples	

Figure 2.20. Export Settings

UG149: Si5344H Evaluation Board User's Guide • Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

3. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5344H using ClockBuilder Pro on the Si5344H EVB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5344H RAM space and can be done virtually unlimited number of times. Writing to OTP is limited, as described below.

Refer to the Si534x/8x Family Reference Manuals and device datasheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can only be programmed a maximum of two times. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

UG149: Si5344H Evaluation Board User's Guide • Serial Device Communications (Si5344H ↔ MCU)

4. Serial Device Communications (Si5344H ↔ MCU)

4.1 On-Board SPI Support

The MCU on-board the Si5344H-EVB communicates with the Si5344H device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5344H device is the SPI slave. The Si5344H device can also support a 2-wire I2C serial interface, although the Si5344H-EVB does NOT support the I2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I2C.

4.2 External I2C Support

I²C can be supported if driven from an external I²C controller. The serial interface signals between the MCU and Si5344H pass through shunts loaded on header J17. These jumper shunts must be installed in J17 for normal EVB operation using SPI with CBPro. If testing of I²C operation via external controller is desired, the shunts in J17 can be removed thereby isolating the on-board MCU from the Si5344H device. The shunt at JP1 (I2C_SEL) must also be removed to select I²C as Si5344H interface type. An external I2C controller connected to the Si5344H side of J17 can then communicate to the Si5344H device. (For more information on I²C signal protocol, please refer to the Si5344H data sheet.)

The figure below illustrates the J17 header schematic. J17 even numbered pins (2, 4, 6, etc.) connect to the Si5344H device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J17 and JP1, I2C operation should use J17 pin 4 (DUT_SDA_SDIO) as the I²C SDA and J17 pin 8 (DUT_SCLK) as the I²C SCLK. Please note the external I²C controller will need to supply its own I²C signal pull-up resistors.

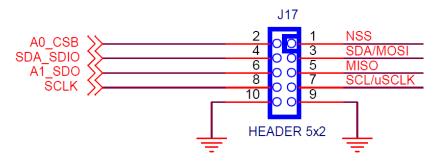


Figure 4.1. Serial Communications Header J17

SKYWORKS

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

www.skyworksinc.com/CBPro



C

Portfolio www.skyworksinc.com/ia/timing

www.skyworksinc.com/CBPro



Quality www.skyworksinc.com/quality



Support & Resources www.skyworksinc.com/support

Copyright © 2021 Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5[®], SkyOne[®], SkyBlue[™], Skyworks Green[™], Clockbuilder[®], DSPLL[®], ISOmodem[®], ProSLIC[®], and SiPHY[®] are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.



X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Clock & Timer Development Tools category:

Click to view products by Silicon Labs manufacturer:

Other Similar products are found below :

AD9517-0A/PCBZ AD9517-2A/PCBZ AD9522-4/PCBZ AD9520-5PCBZ AD9553/PCBZ ADCLK914PCBZ LMH2180SDEVAL DSC400-0333Q0032KE1-EVB TDGL013 MAX2880EVKIT# MAX2750EVKIT MAX2752EVKIT ADCLK946PCBZ ADCLK946/PCBZ MAX2622EVKIT EKIT01-HMC1032LP6G Si5332-8IX-EVB RV-2251-C3-EVALUATION-BOARD Si5332-12IX-EVB RV-3029-C2-EVALUATION-BOARD-OPTION-B Si5332-6IX-EVB SKY72310-11-EVB EV1HMC8364LP6G EV1HMC8362LP6G RV-8263-C7-EVALUATION-BOARD EVK9FGV1002 EVK9FGV1008 EV1HMC6832ALP5L EVAL01-HMC830LP6GE EVAL01-HMC911LC4B EVAL01-HMC988LP3E TS3002DB LMX2487E-EVM MIKROE-2481 2045 EKIT01-HMC835LP6G EKIT01-HMC834LP6GE TS3006DB DSC-TIMEFLASH2-KIT1 110227-HMC510LP5 110227-HMC513LP5 AD9515/PCBZ ADCLK948/PCBZ ADCLK954/PCBZ 112261-HMC739LP4 ADCLK925/PCBZ AD9522-0/PCBZ AD9520-4/PCBZ AC164147 DFR0469