Si5347/46

DUAL/QUAD DSPLL ANY-FREQUENCY, ANY-OUTPUT JITTER ATTENUATORS

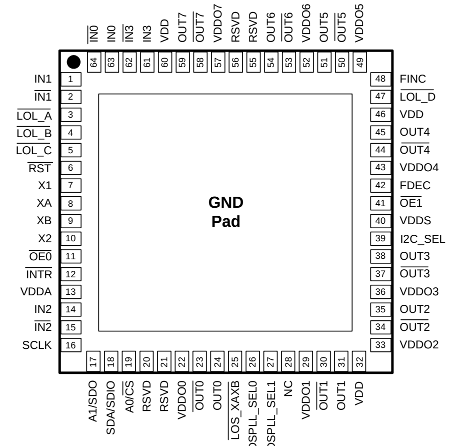
Features

- Four or two independent DSPLLs in a single monolithic IC
- Each DSPLL generates any output frequency from any input frequency
- Input frequency range:
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: up to 800 MHz
  - LVCMOS: up to 250 MHz
- Jitter performance: <100 fs typ (12 kHz–20 MHz)
- Flexible crosspoints route any input to any output clock
- Programmable jitter attenuation bandwidth per DSPLL: 0.1 Hz to 4 kHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, programmable signal swings
- Status monitoring (LOS, OOF, LOL)
- Hitless input clock switching: automatic or manual
- Locks to gapped clock inputs
- Automatic free-run and holdover modes
- Fastlock: <200 ms lock time
- Glitchless on-the-fly DSPLL frequency changes
- DCO mode: as low as 0.01 ppb steps per DSPLL
- Core voltage:
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output supply pins: 3.3V, 2.5V, or 1.8V
- Output-output skew:
- <100 ps per DSPLL
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder Pro software tool simplifies device configuration
- Si5347: Quad DSPLL, 4 input, 8 output, 64 QFN
- Si5346: Dual DSPLL, 4 input, 4 output, 44 QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

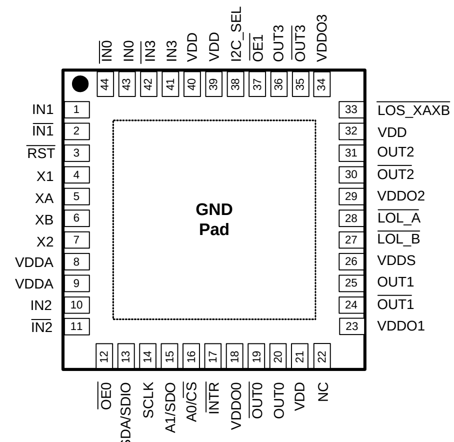
Ordering Information:
See section 7

Pin Assignments

Si5347 64QFN
Top View



Si5346 44QFN
Top View



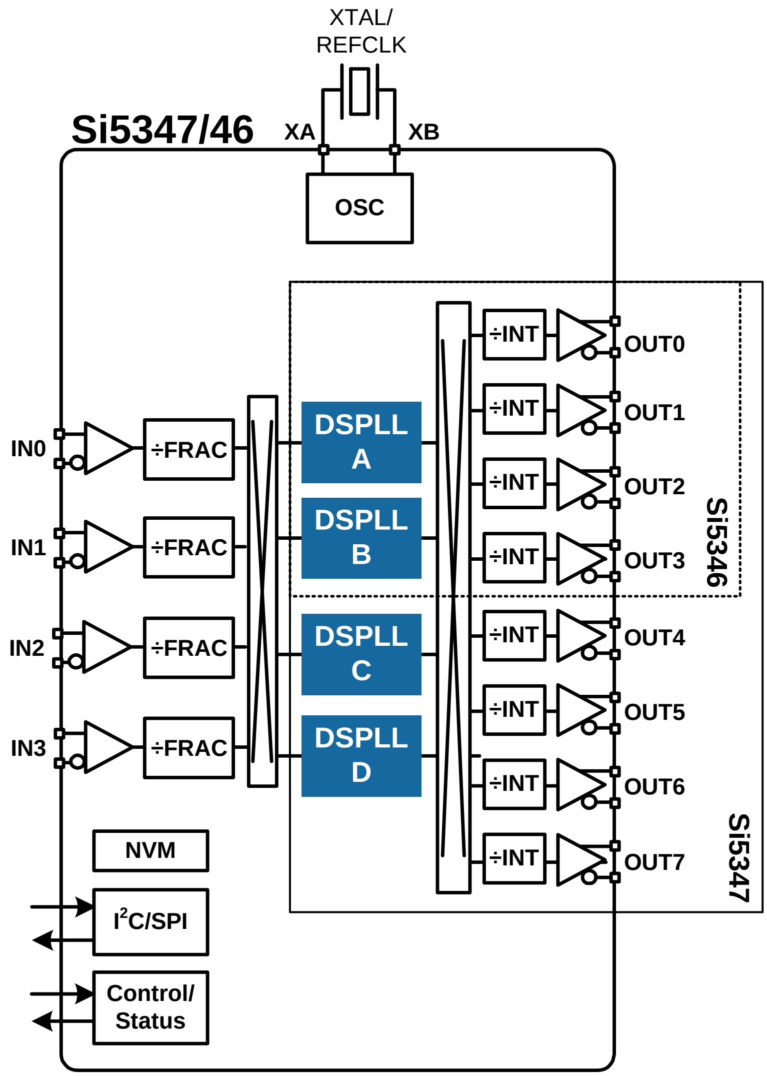
Applications

- OTN Muxponders and Transponders
- 10/40/100G network line cards
- GbE/10GbE/100GbE Synchronous Ethernet
- Carrier Ethernet switches
- Broadcast video

Description

The Si5347 is a high performance jitter attenuating clock multiplier which integrates four any-frequency DSPLLs for applications that require maximum integration and independent timing paths. The Si5346 is a dual DSPLL version in a smaller package. Each DSPLL has access to any of the four inputs and can provides low jitter clocks on any of the device outputs. Based on 4th generation DSPLL technology, these devices provide any-frequency conversion with typical jitter performance of 100 fs. Each DSPLL supports independent free-run, holdover modes of operation, and offers automatic and hitless input clock switching. The Si5347/46 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up with a known configuration. Programming the Si5347/46 is made easy with Silicon Labs' ClockBuilderPro software. Factory pre-programmed devices are also available.

Functional Block Diagram



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1. Typical Application Schematic

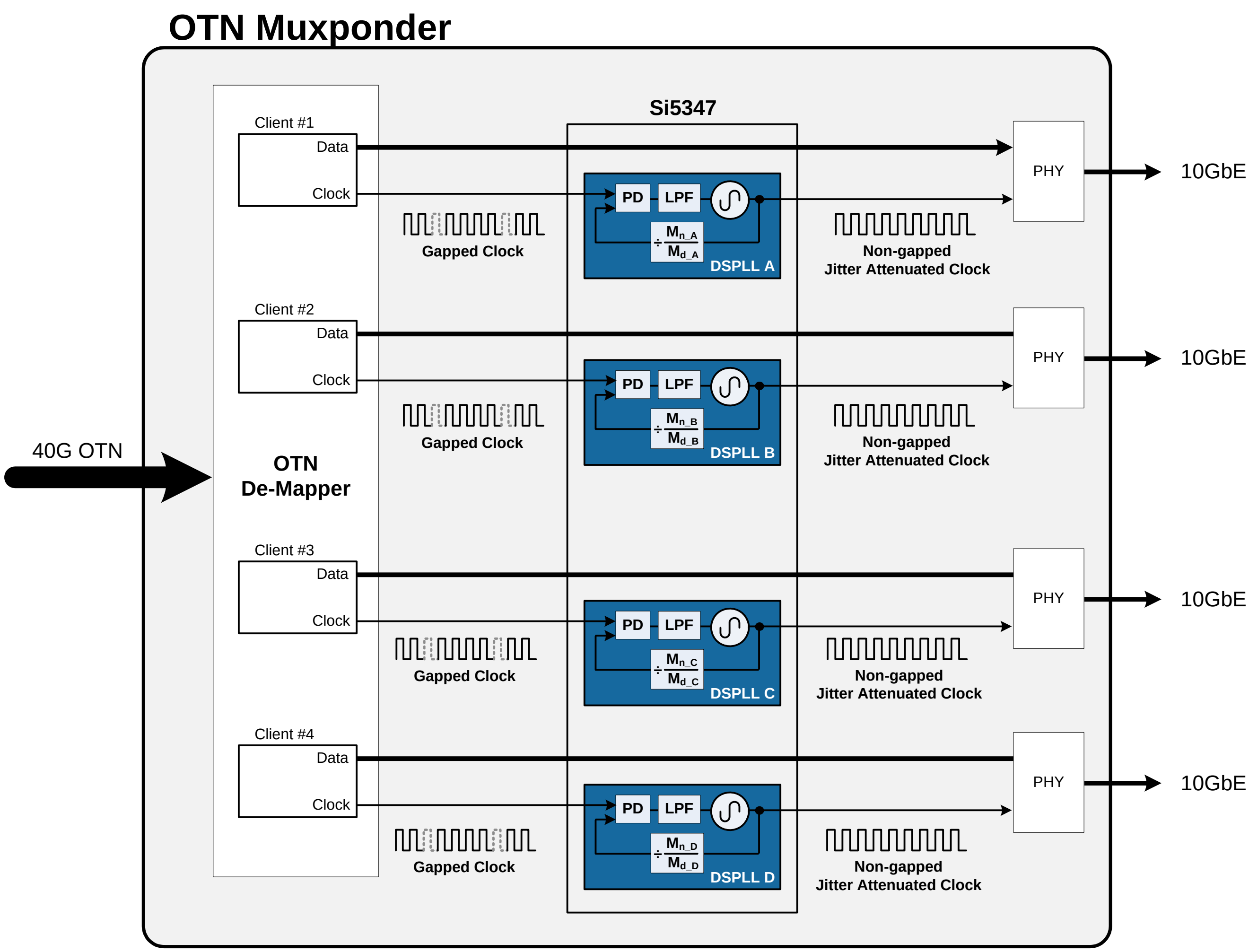


Figure 1. Using The Si5347 to Clean Gapped Clocks in an OTN Application

2. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

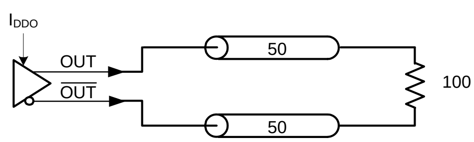
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core Supply Current	I_{DD}	Si5347	Notes [1], [2]	—	270	365	mA
		Si5346		—	—	173	mA
	I_{DDA}	Si5347		—	125	137	mA

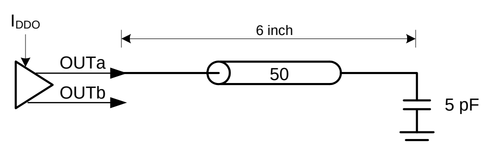
Note:

1. Si5347 test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5346 test configuration: 4 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 6 inch 50 Ω PCB trace with 5 pF load.

Differential Output Test Configuration



LVCMOS Output Test Configuration



5. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 2. DC Characteristics (Continued)

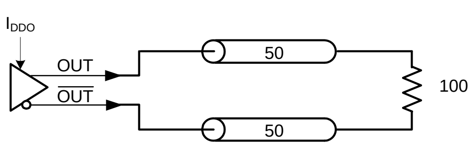
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[3] @ 156.25 MHz	—	23	25	mA
		LVDS Output[3] @ 156.25 MHz	—	16	18	mA
		3.3V LVCMOS[4] output @ 156.25 MHz	—	19	26	mA
		2.5V LVCMOS[4] output @ 156.25 MHz	—	15	19	mA
		1.8V LVCMOS[4] output @ 156.25 MHz	—	11	13	mA
Total Power Dissipation	P_d	Si5347 Note [1,5]	—	1180	1380	mW
		Si5346 Note [2,5]	—	883	—	mW

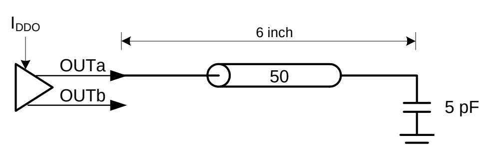
Note:

1. Si5347 test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5346 test configuration: 4 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 6 inch 50 Ω PCB trace with 5 pF load.

Differential Output Test Configuration



LVCMOS Output Test Configuration



5. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 3. Input Specifications
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential or Single-Ended - AC Coupled (IN0/$\overline{IN0}$, IN1/$\overline{IN1}$, IN2/$\overline{IN2}$, IN3/$\overline{IN3}$)						
Input Frequency Range	f_{IN_DIFF}		0.008	—	750	MHz
Voltage Swing	V_{IN}	f_{in}< 400 MHz	100	—	1000	mVpp_se
		600 MHz < f_{in}< 800 MHz	225	—	1000	mVpp_se
		f_{in} > 800 MHz	375	—	1000	mVpp_se
Slew Rate[1,2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
LVCMOS - DC Coupled (IN0, IN1, IN2, IN3)						
Input Frequency	f_{IN_CMOS}		0.008	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.18	V
	V_{IH}		0.7	—	—	V
Slew Rate[1,2]	SR		400	—	—	V/µs
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (Applied to XA/XB)						
REFCLK Frequency	f_{IN_REF}	Frequency range for best output jitter performance	48	—	54	MHz
Input Voltage Swing	V_{IN}		350	—	1600	mVpp_se
Slew rate[1,2]	SR	Imposed for best jitter performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Note:
1. Imposed for jitter performance
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20}$ = ((0.8 - 0.2) x $V_{IN\_Vpp\_se}$) / SR
3. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.
4. A programmable internal divider (P_{REF}) is available to help support REFCLK frequencies up to 200 MHz.

Table 4. Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5347 Control Input Pins (I2C_SEL, $\overline{\text{RST}}$, $\overline{\text{OE0}}$, A1, SCLK, A0/$\overline{\text{CS}}$, $\overline{\text{FINC}}$, A0/$\overline{\text{CS}}$, SDA, SDI, DSPLL_SEL0, DSPLL_SEL1)						
Input Voltage	V_{IL}		–0.1	—	0.3 x V_{DDIO}*	V
	V_{IH}		0.7 x V_{DDIO}*	—	3.6	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RST	50	—	—	ns
Si5347 Control Input Pins ($\overline{\text{FDEC}}$, $\overline{\text{OE1}}$)						
Input Voltage	V_{IL}		–0.1	—	0.3 x V_{DDS}	V
	V_{IH}		0.7 x V_{DDS}	—	3.6	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	FDEC	50	—	—	ns
Si5346 Control Input Pins (I2C_SEL, $\overline{\text{RST}}$, $\overline{\text{OE0}}$, $\overline{\text{OE1}}$, A1, SCLK, A0/$\overline{\text{CS}}$, SDA, SDI)						
Input Voltage	V_{IL}		–0.1	—	0.3 x V_{DDIO}*	V
	V_{IH}		0.7 x V_{DDIO}*	—	3.6	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RST	50	—	—	ns
***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.						

Table 5. Differential Clock Output Specifications
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	f_{OUT}			0.0001	—	800	MHz
Duty Cycle	DC	f < 400 MHz		48	—	52	%
		400 MHz < f < 800 MHz		45	—	55	%
Output-Output Skew	T_{SK}	Differential Output		—	—	100	ps
OUT-$\overline{OUT}$ Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	—	100	ps
Output Voltage Swing[1]	**Normal Swing Mode**						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	370	470	570	mVpp_se
			LVPECL	650	820	1050	
	Low Power Mode						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	310	420	530	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVPECL	590	830	1063	
Common Mode Voltage[1,2,3]	**Normal Swing or Low Power Modes**						
	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.12	1.23	1.34	V
			LVPECL	1.90	2.0	2.13	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.17	1.23	1.30	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Swing Mode		—	170	220	ps
		Low Power Mode		—	250	320	
Differential Output Impedance[4]	Z_O	Normal Swing Mode		—	100	—	Ω
		Low Power Mode		—	Hi-Z	—	Ω

Table 5. Differential Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Supply Noise Rejection[5]	PSRR	**Normal Swing Mode**				
		10 kHz sinusoidal noise	—	–93	—	dBc
		100 kHz sinusoidal noise	—	–93	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–79	—	
		Low Power Mode				
		10 kHz sinusoidal noise	—	–98	—	dBc
		100 kHz sinusoidal noise	—	–95	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–76	—	
Output-output Crosstalk	XTALK	Measured spur from adjacent output	—	–73	—	dB

Notes:

1. Normal swing mode, low power mode, Vswing and Cmode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently.
2. Not all combinations of voltage swing and common mode voltages settings are possible.
3. Common mode voltage min/max variation = ±4% from typical value.
4. Driver output impedance depends on selected output mode (Normal, High).
5. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.

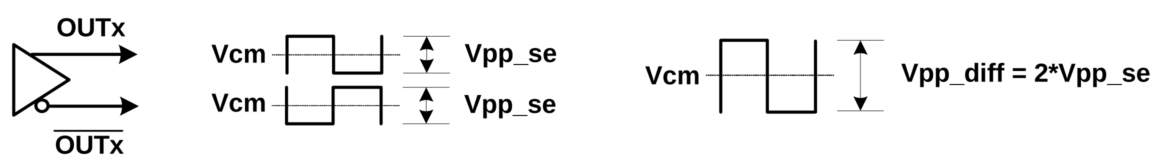


Table 6. Output Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5347 Status Output Pins ($\overline{LOL\_A}$, $\overline{LOL\_B}$, $\overline{LOL\_C}$, $\overline{LOL\_D}$, $\overline{INTR}$, $\overline{LOS\_XAXB}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}^1 x 0.15	V
Si5346 Status Output Pins ($\overline{LOL\_A}$, $\overline{LOL\_B}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V
Si5346 Status Output Pins ($\overline{INTR}$, $\overline{LOS\_XAXB}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}* x 0.15	V
***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.						

Table 7. LVCMOS Clock Output Specifications

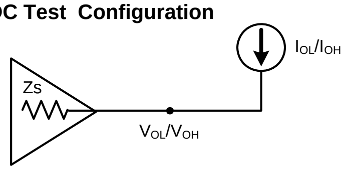
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	F_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	f < 400 MHz		48	—	52	%
		400 MHz < f < 800 MHz		45	—	55	%
Output-to-Output Skew	T_{SK}			—	—	100	ps
Output Voltage High[1,2,3]	V_{OH}	V_{DDO} = 3.3 V					
		CMOS1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		CMOS2	I_{OH} = –12 mA		—	—	
		CMOS3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		CMOS2	I_{OH} = –8 mA	V_{DDO} x 0.85	—	—	V
		CMOS3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		CMOS3	I_{OH} = –5 mA	V_{DDO} x 0.85	—	—	V
Output Voltage Low[1,2,3]	V_{OL}	V_{DDO} = 3.3 V					
		CMOS1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		CMOS2	I_{OL} = 12 mA	—	—		
		CMOS3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		CMOS2	I_{OL} = 8 mA	—	—	V_{DDO} x 0.15	V
		CMOS3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		CMOS3	I_{OL} = 5 mA	—	—	V_{DDO} x 0.15	V
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3 V		—	360	—	ps
		VDDO = 2.5 V		—	420	—	ps
		VDDO = 1.8 V		—	280	—	ps

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are CMOS1, CMOS2, CMOS3.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ohm PCB trace. A 5 pF capacitive load is assumed.

DC Test Configuration



AC Test Configuration

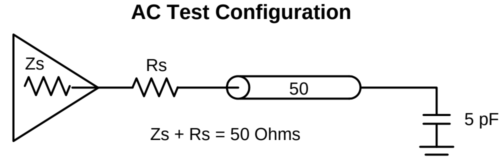


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Table 8. Performance Characteristics

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DD33} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	—	ms
PLL Lock Time	t_{ACQ}	With Fastlock enabled[1]	—	160	—	ms
POR to Serial Interface Ready	t_{RDY}		—	—	10	ms
PLL Loop Bandwidth	f_{BW}		0.1	—	4000	Hz
Jitter Peaking	J_{PK}		—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter modulation = 10 Hz	—	23	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}		—	—	1.5	ns
Pull-in Range	ω_P		—	500	—	ppm
Input-to-Output Delay	$t_{IODELAY}$	Input-to-output delay is consistent at every power-up	—	2	—	ns
RMS Phase Jitter[2]	J_{GEN}	12 kHz to 20 MHz	—	0.115	0.160	ps

Notes:

1. Fastlock bandwidth = 1 kHz. Measured from valid input to LOL deassertion.
2. Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz. Does not include jitter from input clock.

Table 9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Units
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		0	100	0	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		5.0	—	—	—	µs
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

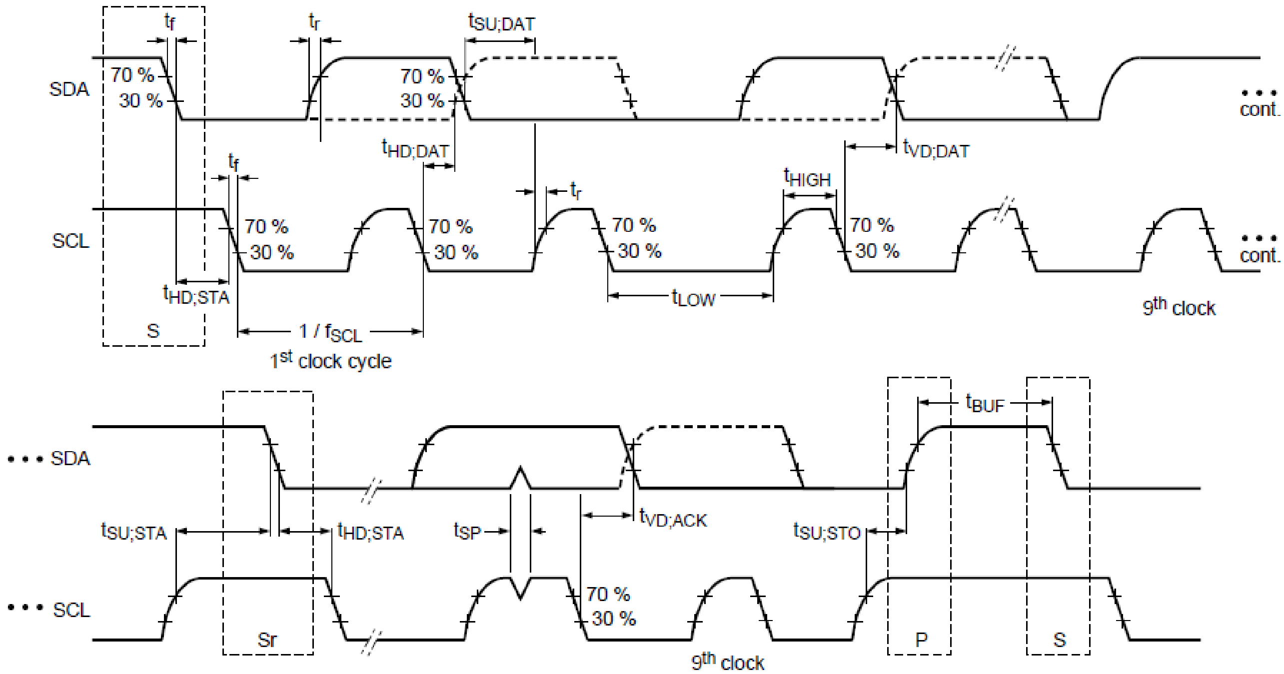


Figure 2. I^{2}C Serial Port Timing Standard and Fast Modes

Table 10. SPI Timing Specifications

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DD33} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Rise & Fall Time	Tr/Tf	—	—	10	ns
SCLK High & Low Time	T_{HL}				
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	12.5	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	12.5	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-State	T_{D3}	—	—	12.5	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	25	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Rise	T_{H1}	25	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	12.5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	12.5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	50	—	—	ns

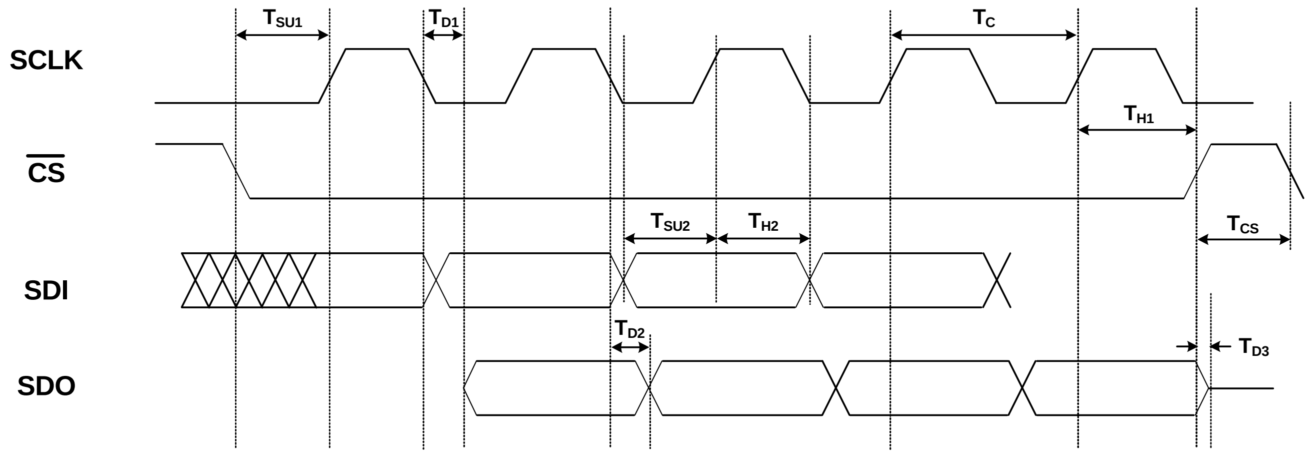


Figure 3. SPI Serial Interface Timing

Table 11. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency Range	f_{XTAL}	Frequency range for best jitter performance	48	—	54	MHz
Load Capacitance	C_L		—	8	—	pF
Shunt Capacitance	C_O		—	—	3	pF
Crystal Drive Level	d_L		—	—	200	µW
Equivalent Series Resistance	r_{ESR}	Refer to the Si5347/46 Family Reference Manual to determine ESR				

Notes:

1. The Si5347/46 is designed to work with crystals that meet the specifications in Table 11.
2. Refer to the Si5347/46 Family Reference Manual for recommended 48 to 54 MHz crystals. Crystal frequencies from 24.97 to 54.06 MHz are supported, but jitter performance is best from 48 to 54 MHz.

Table 12. Thermal Characteristics

Parameter	Symbol	Test Condition*	Value	Units
Si5347–64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	
Si5346–44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	

***Note:** Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 13. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0 - IN3	–0.85 to 3.8	V
	V_{I2}	$\overline{\text{RST}}$, $\overline{\text{OE0}}$, $\overline{\text{OE1}}$, I2C_SEL, FINC, FDEC, PLL_SEL[1:0] SDI, SCLK, A0/$\overline{\text{CS}}$	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Junction Temperature	T_{JCT}		–55 to 150	°C
Soldering Temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[5]	T_P		20–40	s

Note:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. Moisture sensitivity level is MSL2.
5. The device is compliant with JEDEC J-STD-020.

3. Detailed Block Diagram

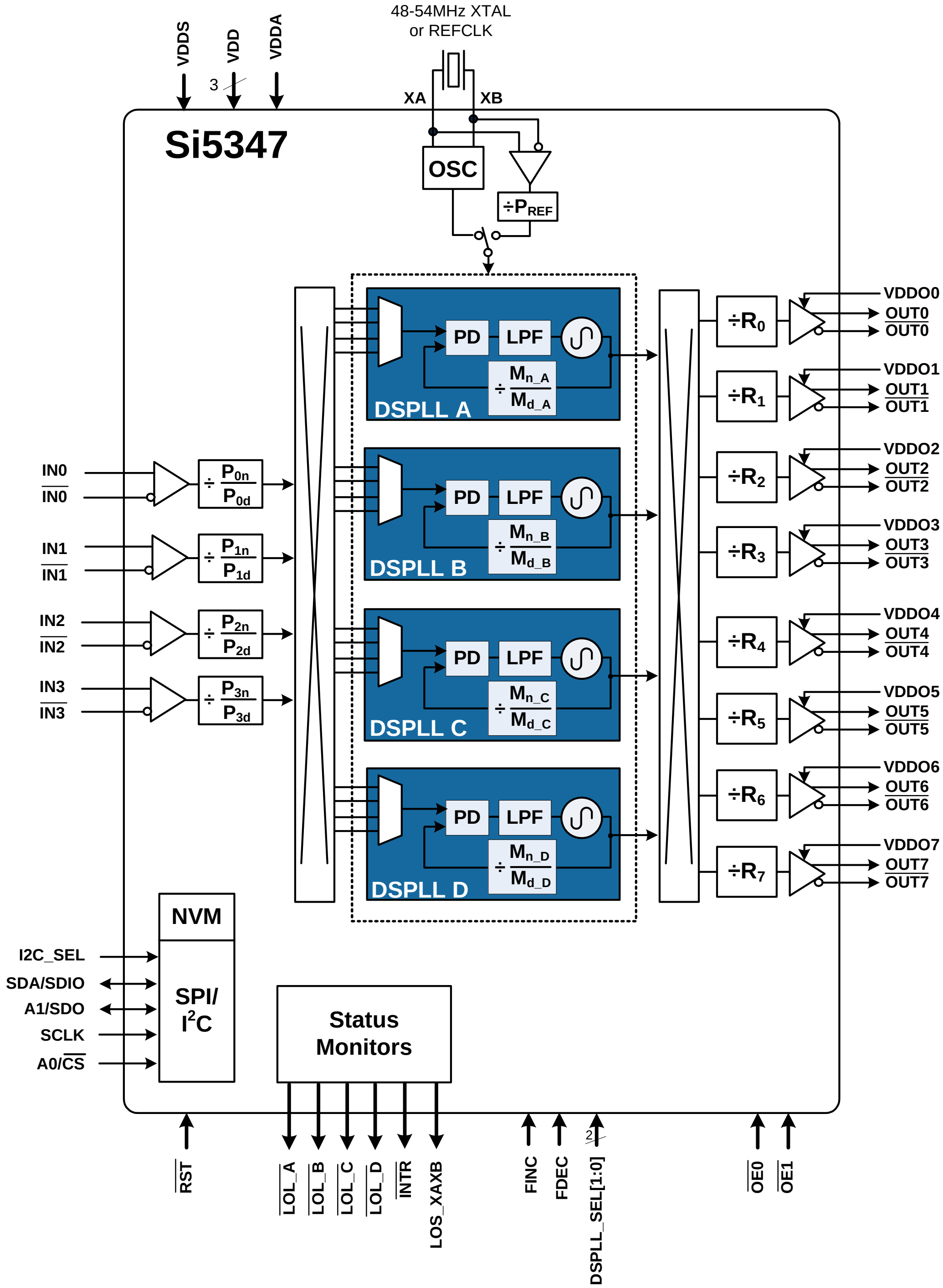


Figure 4. Si5347 Detailed Block Diagram

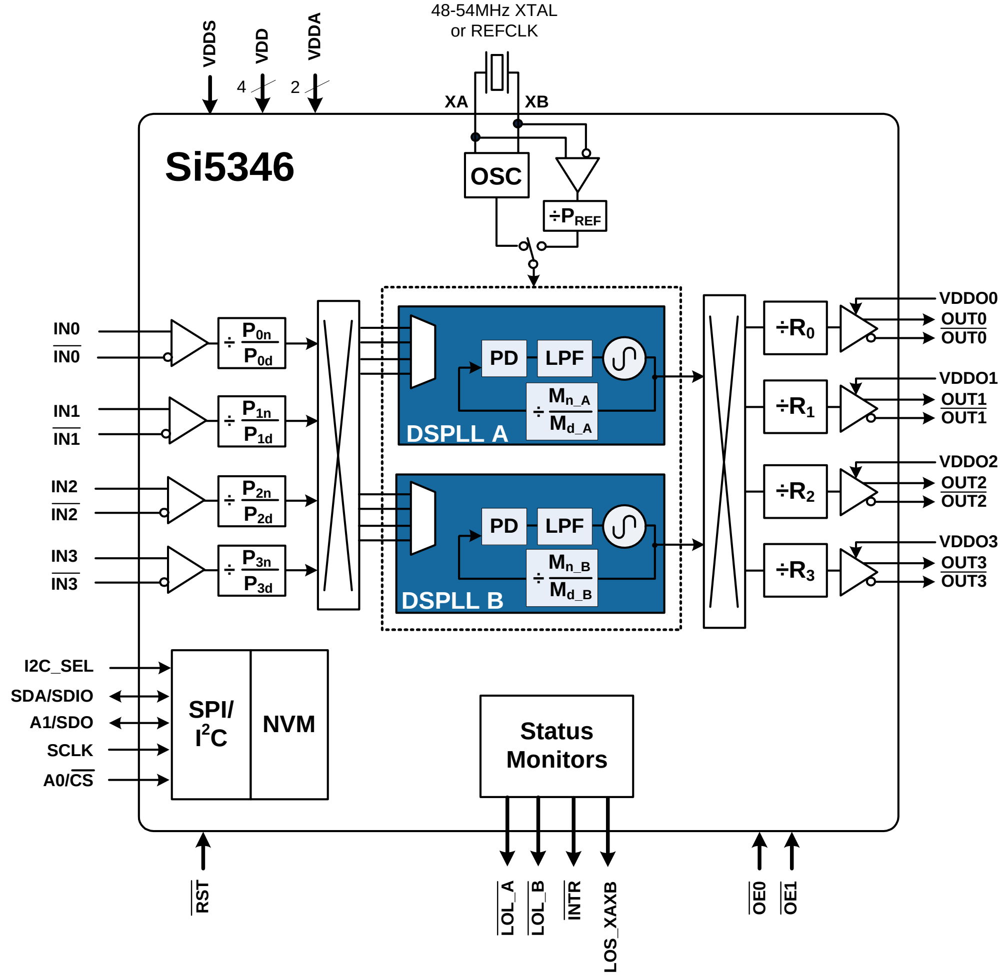


Figure 5. Si5346 Detailed Block Diagram

4. Functional Description

The Si5347 takes advantage of Silicon Labs' 4th generation DSPLL technology to offer the industry's most integrated and flexible jitter attenuating clock generator solution. Each of the DSPLLs operate independently from each other and are controlled through a common serial interface. Each DSPLL has access to any of the four inputs (IN0 to IN3) with manual or automatic input selection. Any of the output clocks (OUT0 to OUT7) can be configured to any of the DSPLLs using a flexible crosspoint connection. The Si5346 is a smaller form factor dual DSPLL version with four inputs and four outputs.

4.1. Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), and integer output division (R_n) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

4.2. DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection for each of the DSPLLs. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

4.2.1. Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in in the range of 100 Hz to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting as described in section "4.2. DSPLL Loop Bandwidth" . The fastlock feature can be enabled or disabled independently for each of the DSPLLs.

4.3. Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of three modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 6. The following sections describe each of these modes in greater detail.

4.3.1. Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the $\overline{RST}$ pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can affect all or each DSPLL individually.

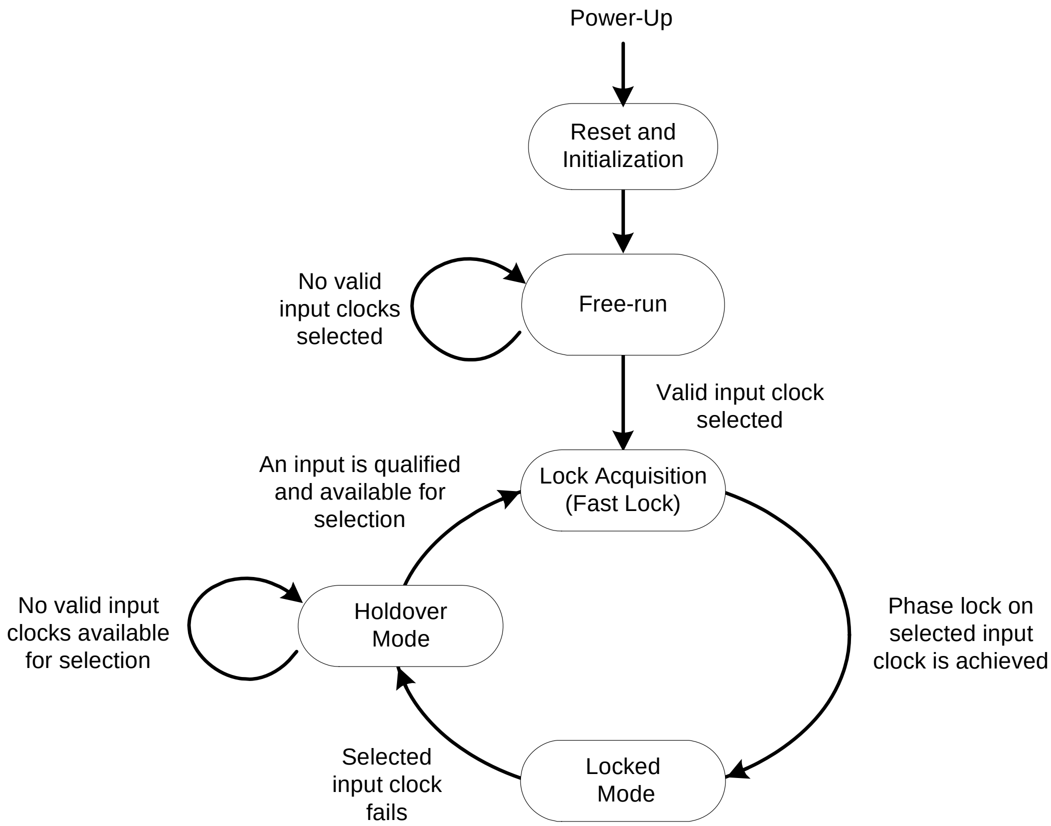


Figure 6. Modes of Operation

4.3.2. Freerun Mode

Once power is applied to the Si5347 and initialization is complete, all four DSPLLs will automatically enter freerun mode. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes.

4.3.3. Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process.

If the fast lock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.3.4. Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own $\overline{LOL}$ pin and status bit to indicate when lock is achieved. See "4.7.4. LOL Detection" on page 28 for more details on the operation of the loss of lock circuit.

4.3.5. Holdover Mode

Any of the DSPLLs will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in Figure 7. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

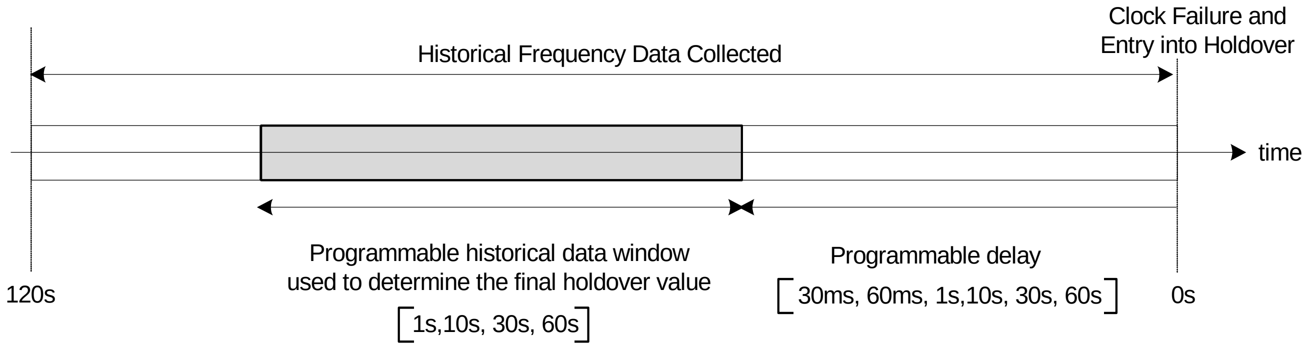


Figure 7. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, a DSPLL will automatically exit the holdover mode and reacquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless, and its rate is controlled by the DSPLL bandwidth, the Fastlock bandwidth, or an artificial linear ramp rate selectable from 0.75 ppm/s up to 40 ppm/s. These options are register programmable.

4.4. Digitally-Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in predefined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in either free-running or locked mode. Controlling The DCO Mode Using The Serial Interface

4.5. External Reference (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLLs and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in Figure 8. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to Table 11 for crystal specifications. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance. Frequency offsets due to C_L mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±200 ppm. The Si5347/46 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

The device can also accommodate an external reference clock (REFCLK) instead of a crystal. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (C_L) are disabled in this mode. Refer to Table 3 for REFCLK requirements when using this mode. The Si5347/46 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. A P_{REF} divider is available to accommodate external clock frequencies higher than 54 MHz. Although the REFCLK frequency range of 25 MHz to 200 MHz is supported, frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.

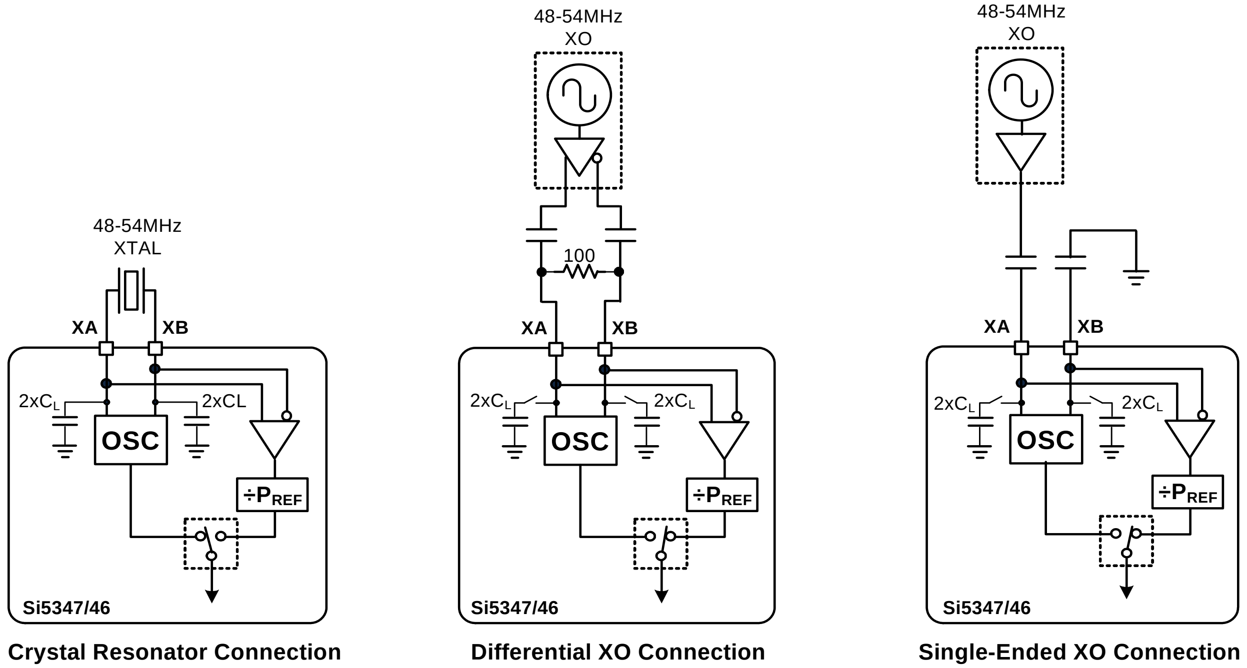


Figure 8. Crystal Resonator and External Reference Clock Connection Options

4.6. Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs as shown in Figure 9.

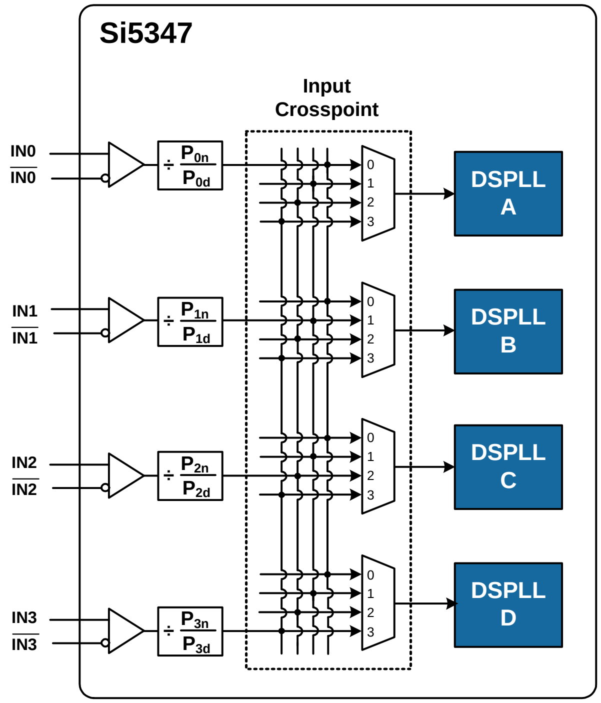


Figure 9. DSPLL Input Selection Crosspoint

4.6.1. Input Selection

Input selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine.

4.6.2. Manual Input Selection

In manual mode the input selection is made by writing to a register. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode.

4.6.3. Automatic Input Selection

When configured in this mode, the DSPLLs automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each DSPLL and supports revertive or non-revertive selection.

All inputs are continuously monitored for loss of signal (LOS) and/or invalid frequency range (OOF). Only inputs that do not assert both the LOS and OOF monitors can be selected for synchronization by the automatic state machine. The DSPLL(s) will enter the holdover mode if there are no valid inputs available.

4.6.4. Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in Figure 10. Differential signals must be ac coupled, while single-ended LVCMOS signals can be ac or dc coupled. Unused inputs can be disabled and left unconnected when not in use.

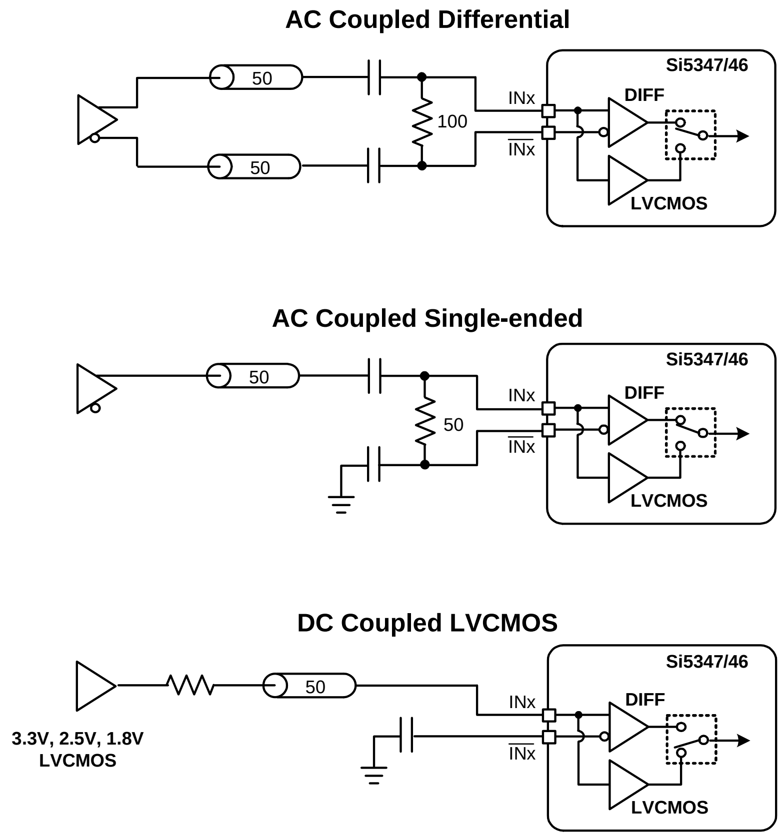


Figure 10. Termination of Differential and LVCMOS Input Signals

4.6.5. Hitless Input Switching

Hitless switching is a feature that prevents a phase transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at a fractional frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during a input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz. Hitless switching can be enabled on a per DSPLL basis.

4.6.6. Glitchless Input Switching

The DSPLLs have the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if it is enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition.

4.6.7. Synchronizing to Gapped Input Clocks

Each of the DSPLLs support locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in Figure 11.

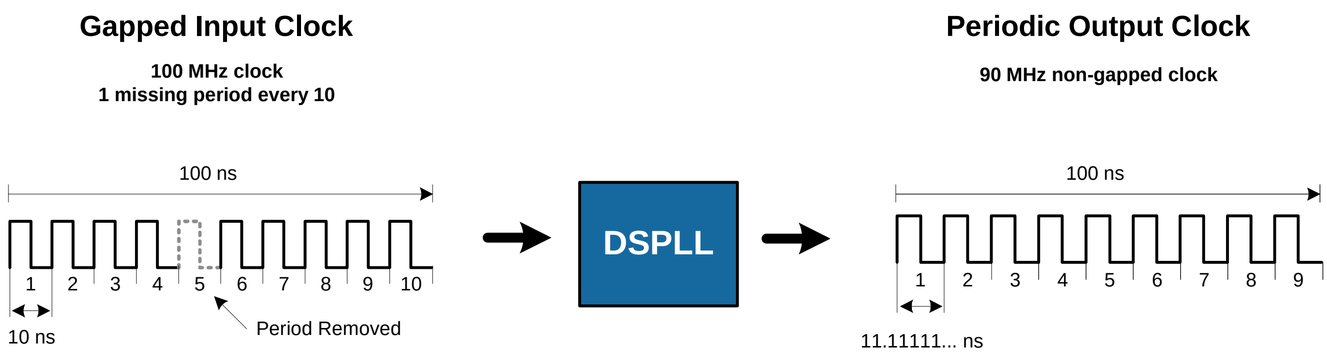


Figure 11. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every 8. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 8 when the switch occurs during a gap in either input clocks.

4.7. Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in Figure 12. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has a Loss Of Lock (LOL) indicator, which is asserted when synchronization is lost with their selected input clock.

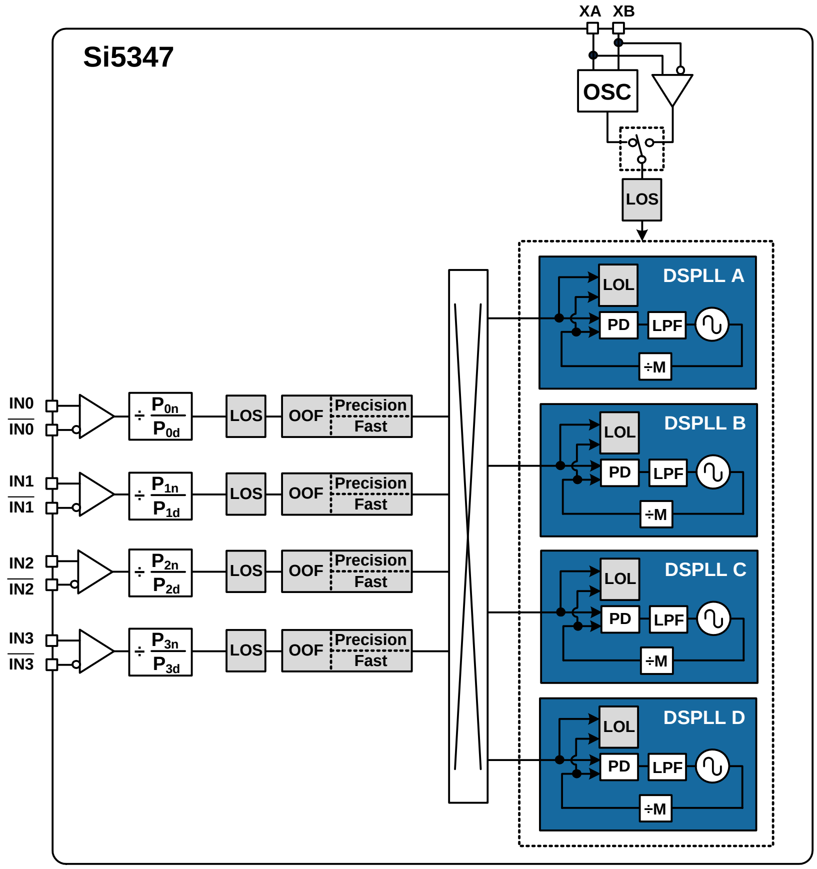


Figure 12. Si5347/46 Fault Monitors

4.7.1. Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

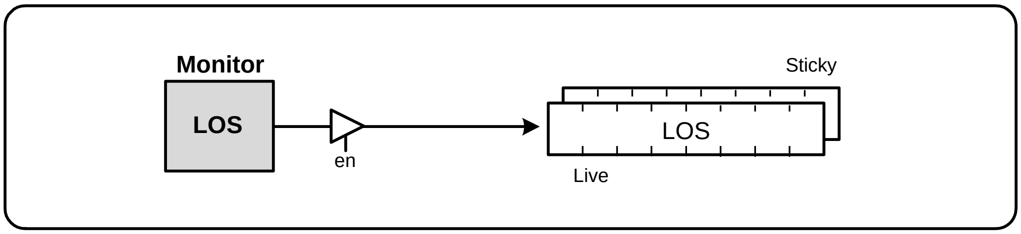


Figure 13. LOS Status Indicators

4.7.2. XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

4.7.3. OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference.

This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in Figure 14. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

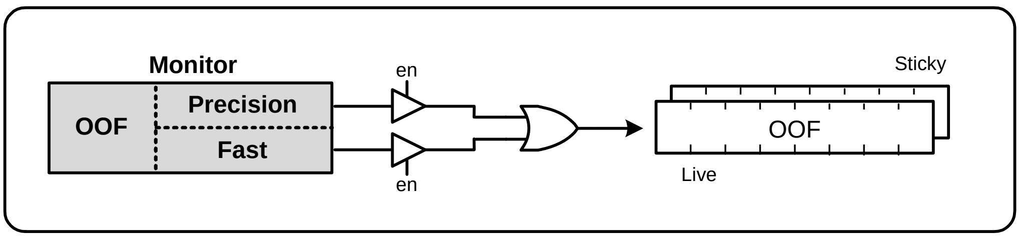


Figure 14. OOF Status Indicator

4.7.3.1. Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable from ±2 ppm to ±500 ppm in steps of 2 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in Figure 15. In this case the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 – IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register-configurable.

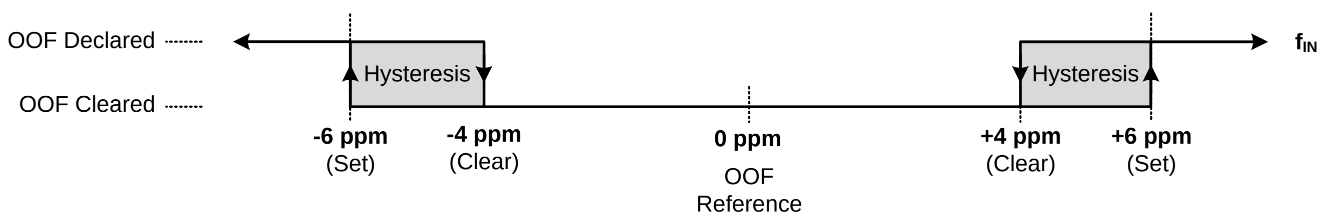


Figure 15. Example of Precise OOF Monitor Assertion and De-assertion Triggers

4.7.3.2. Fast OOF Monitor

Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

4.7.4. LOL Detection

There is a loss of lock (LOL) monitor for each of the DSPLLs. The LOL monitor asserts a LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs ($\overline{LOL\_A}$, $\overline{LOL\_B}$, $\overline{LOL\_C}$, $\overline{LOL\_D}$). The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in Figure 16. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

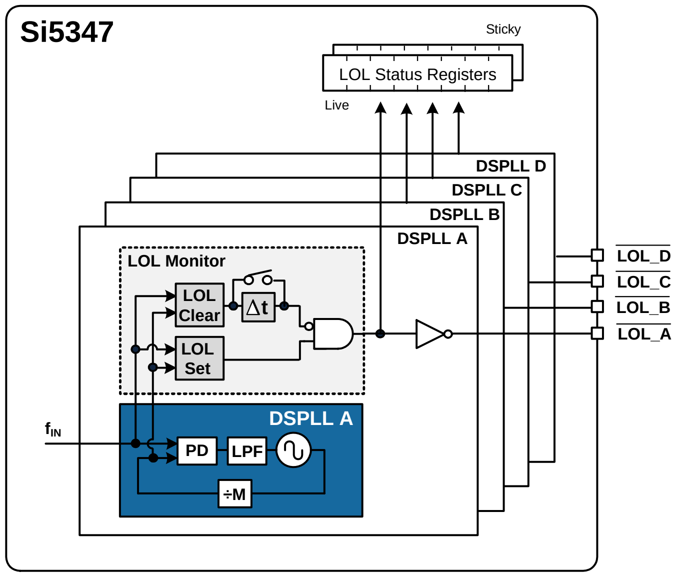


Figure 16. LOL Status Indicators

Each of the LOL frequency monitors has adjustable sensitivity which is register configurable from 0.2 ppm to 20000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 2 ppm frequency difference is shown in Figure 17.

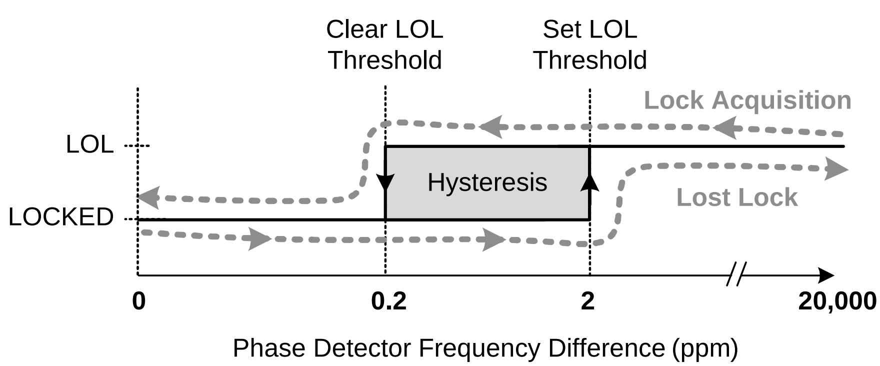


Figure 17. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

4.7.5. Interrupt Pin (INTR)

An interrupt pin (INTR) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the sticky status registers.

4.8. Outputs

The Si5347 supports eight differential output drivers and the Si5346 supports four. Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 16 single-ended outputs, or any combination of differential and single-ended outputs.

4.8.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs as shown in Figure 18. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

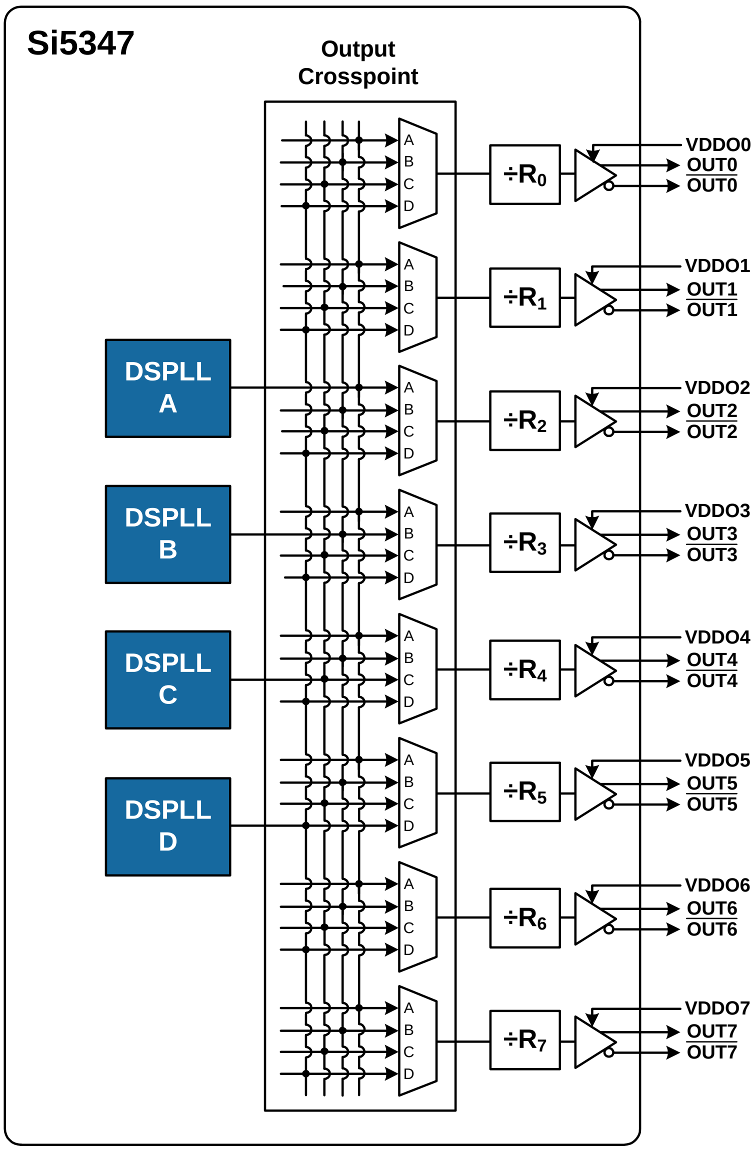


Figure 18. DSPLL to Output Driver Crosspoint

4.8.2. Differential Output Terminations

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

The differential output drivers support both ac coupled and dc coupled terminations as shown in Figure 19.

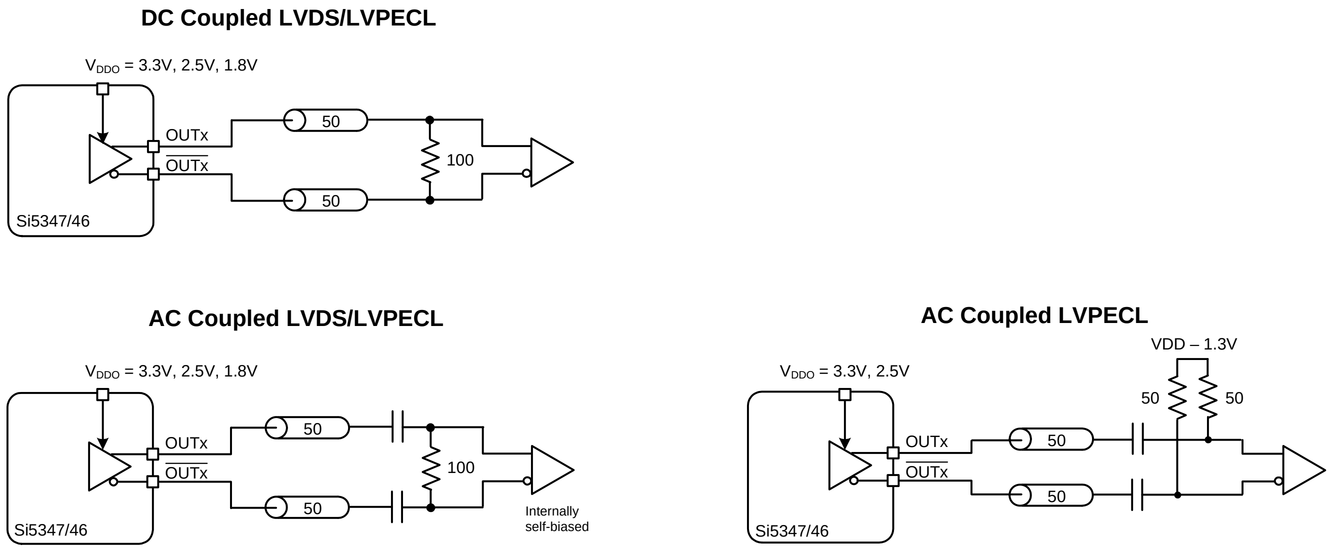


Figure 19. Supported Differential Output Terminations

4.8.3. LVCMOS Output Terminations

LVCMOS outputs are dc-coupled as shown in Figure 20.

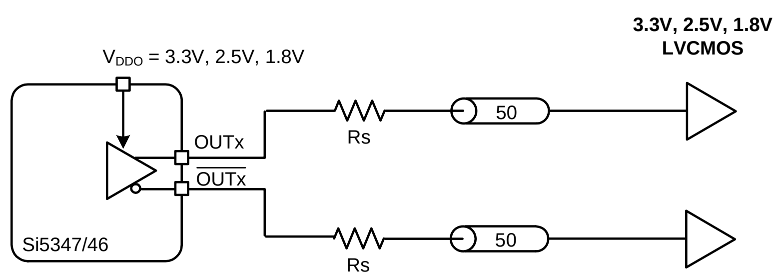


Figure 20. LVCMOS Output Terminations

4.8.4. Output Signal Format

The differential output swing and common mode voltage are both fully programmable and compatible with a wide variety of signal formats, including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 20 single-ended outputs or any combination of differential and single-ended outputs.

4.8.5. Differential Output Swing Modes

There are two selectable differential output swing modes: Normal and high swing. Each output can support a unique mode.

- **Differential Normal Swing Mode:** When an output driver is configured in normal swing mode, its output swing is selectable as one of 7 settings ranging from 200 mVpp_se to 800 mVpp_se in increments of 100 mV. The output impedance in the Normal Swing Mode is 100Ω differential. Any of the terminations shown in Figure 19 is supported in this mode.

- **Differential Low Power Mode:** When an output driver is configured in low power mode, its output swing is configurable as one of 7 settings ranging from 400 mVpp_se to 1600 mVpp_se in increments of 200 mV. The output driver is in high impedance mode and supports standard 50 Ω PCB traces. Any of the terminations shown in Figure 19 is supported in this mode.

4.8.6. Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential Normal and Low Power modes is programmable in 100 mV increments from 0.7 V to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when DC coupling the output drivers.

4.8.7. LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections (CMOS1, CMOS2, CMOS3) for each VDDO options as shown in Table 14.

Table 14. Typical Output Impedance (Z_S)

	CMOS_DRIVE_Selection		
VDDO	**CMOS1**	**CMOS2**	**CMOS3**
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

4.8.8. LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

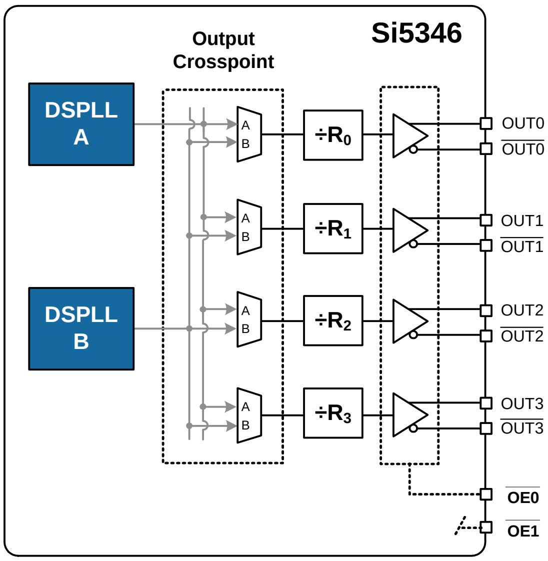
4.8.9. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and $\overline{\text{OUTx}}$). By default the clock on the $\overline{\text{OUTx}}$ pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

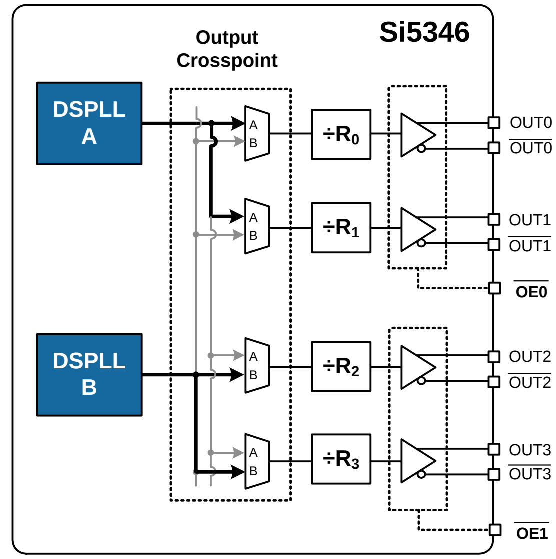
4.8.10. Output Enable/Disable

The Si5347/46 allows enabling/disabling outputs by pin or register control, or a combination of both. Two output enable pins are available ($\overline{\text{OE0}}$, $\overline{\text{OE1}}$). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default $\overline{\text{OE0}}$ controls all of the outputs while $\overline{\text{OE1}}$ remains unmapped and has no affect until configured. Figure 21 shows an example of a output enable mapping scheme that is register configurable and can be stored in NVM as the default at power-up.

Enabling and disabling outputs can also be controlled by register control. This allows disabling one or more output when the $\overline{\text{OE}}$ pin(s) has them enabled. By default the output enable register settings are configured to allow the $\overline{\text{OE}}$ pins to have full control.



In its default state the OE0 pin enables/disables all outputs. The OE1 pin is not mapped and has no effect on outputs.



An example of an configurable output enable scheme. In this case OE0 controls the outputs associated with DSPLL A, while OE1 controls the outputs of DSPLL B.

Figure 21. Example of Configuring Output Enable Pins

4.8.11. Output Disable During LOL

By default a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is out of lock (LOL). This option can be useful to force a downstream PLL into holdover.

4.8.12. Output Disable During XAXB_LOS

The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.

4.8.13. Output Driver State When Disabled

The disabled state of an output driver is register configurable as: disable low, disable high, or disable high-impedance.

4.8.14. Synchronous/Asynchronous Output Disable

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode the output clock will disable immediately without waiting for the period to complete.

4.8.15. Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RST pin or asserting the hard reset bit will have the same result.

4.9. Power Management

Unused inputs, output drivers, and DSPLLs can be powered down when unused. Consult the Si5347/46 Family Reference Manual and ClockBuilder Pro configuration utility for details.

4.10. In-Circuit Programming

The Si5347/46 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5347/46 Family Reference Manual for a detailed procedure for writing registers to NVM.

4.11. Serial Interface

Configuration and operation of the Si5347/46 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3V and 1.8V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Si5347/46 Family Reference Manual for details.

4.12. Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship to you within two weeks.

5. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible register such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in Table 15. Refer to the Si5347/46 Family Reference Manual for a complete list of register descriptions and settings.

5.1. Addressing Scheme

The device registers are accessible using a 16-bit address which consists of an 8-bit page address +8-bit register address. By default the page address is set to 0x00. Changing to another page is accomplished by writing to the “Set Page Address” byte located at address 0x01 of each page.

Table 15. High-Level Register Map

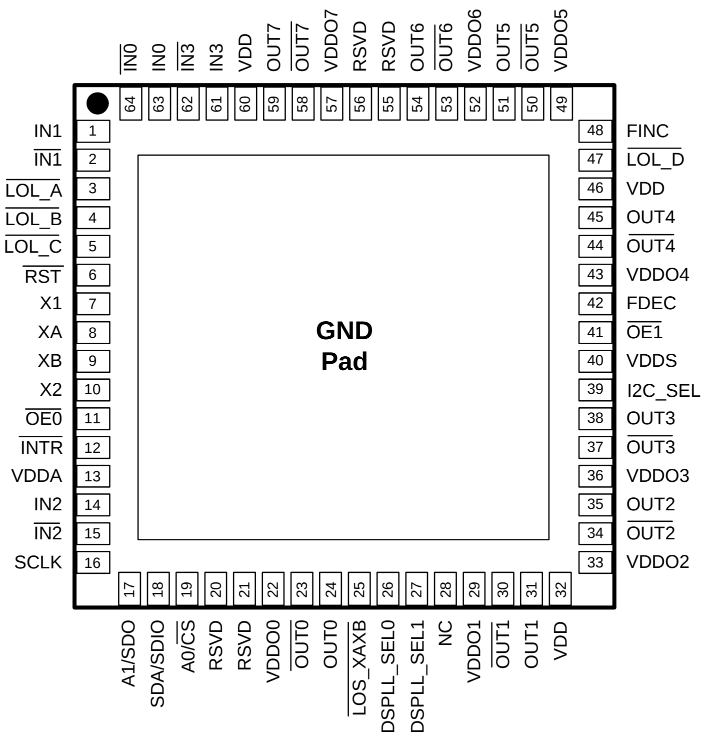
16-Bit Address		Content
8-bit Page Address	**8-bit Register Address Range**	
00	00	Revision IDs
	01	Set Page Address
	02 - 0A	Device IDs
	0B–15	Alarm Status
	17–1B	INTR Masks
	1C	Reset controls
	2C–E1	Alarm Configuration
	E2–E4	NVM Controls
	FE	Device Ready Status
01	01	Set Page Address
	08–3A	Output Driver Controls
	41–42	Output Driver Disable Masks
	FE	Device Ready Status
02	01	Set Page Address
	02–05	XTAL Frequency Adjust
	08–2F	Input Divider (P) Settings
	47–6A	Output Divider (R) Settings
	6B–72	User Scratch Pad Memory
	FE	Device Ready Status
03	01	Reserved

Table 15. High-Level Register Map (Continued)

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
04	01	Set Page Address
	08–0D	DSPLL_A Bandwidth Setting
	0E–13	DSPLL_A Fastlock Bandwidth Setting
	15–1F	DSPLL_A Feedback Divider Setting (MA)
	23–29	DSPLL_A FINC/FDEC Settings
	36, 38–39	DSPLL_A Input Switching Controls
	FE	Device Ready Status
05	01	Set Page Address
	08–0D	DSPLL_B Bandwidth Setting
	0E–13	DSPLL_B Fastlock Bandwidth Setting
	15–1F	DSPLL_B Feedback Divider Setting (MA)
	23–29	DSPLL_B FINC/FDEC Settings
	36, 38–39	DSPLL_B Input Switching Controls
	FE	Device Ready Status
06	01	Set Page Address
	08–0D	DSPLL_C Bandwidth Setting
	0E–13	DSPLL_C Fastlock Bandwidth Setting
	15–1F	DSPLL_C Feedback Divider Setting (MA)
	23–29	DSPLL_C FINC/FDEC Settings
	36, 38–39	DSPLL_C Input Switching Controls
	FE	Device Ready Status
07	01	Set Page Address
	09–0E	DSPLL_D Bandwidth Setting
	0F–14	DSPLL_D Fastlock Bandwidth Setting
	16- 20	DSPLL_D Feedback Divider Setting (MA)
	24–2A	DSPLL_D FINC/FDEC Settings
	37, 39–3A	DSPLL_D Input Switching Controls
	FE	Device Ready Status
09	01	Set Page Address
	49	Input Settings
0A–FF	00–FF	Reserved

6. Pin Descriptions

Si5347 64QFN
Top View



Si5346 44QFN
Top View

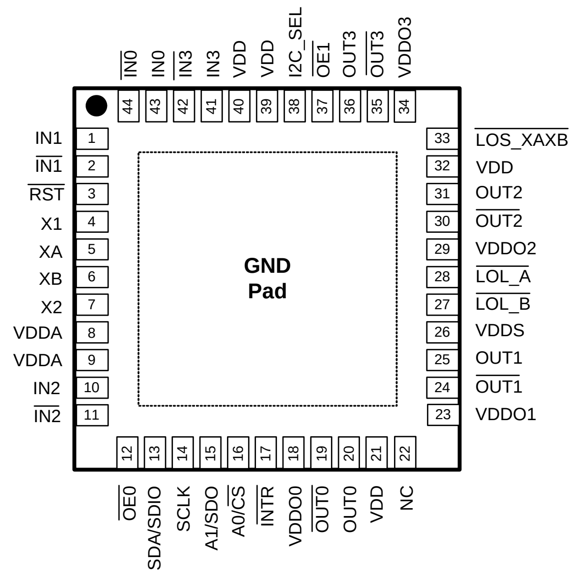


Table 16. Si5347/46 Pin Descriptions

Pin Name	Pin Number		Pin Type[1]	Function
	Si5347	Si5346		
Inputs				
XA	8	5	I	**Crystal Input**. Input pin for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REF-CLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.
XB	9	6	I	
X1	7	4	I	**XTAL Ground.** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5347/46 Family Reference Manual for layout guidelines. These pins should be left discon-nected when connecting XA/XB pins to an external reference clock (REFCLK).
X2	10	7	I	
IN0	63	43	I	**Clock Inputs**. These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to “4.6.4. Input Configuration and Terminations” for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded when accepting a single-ended clock.
$\overline{\text{IN0}}$	64	44	I	
IN1	1	1	I	
$\overline{\text{IN1}}$	2	2	I	
IN2	14	10	I	
$\overline{\text{IN2}}$	15	11	I	
IN3	61	41	I	
$\overline{\text{IN3}}$	62	42	I	

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 16. Si5347/46 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
	Si5347	Si5346		
Outputs				
OUT0	24	20	O	**Output Clocks**. These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in “4.8.2. Differential Output Terminations” and “4.8.3. LVCMOS Output Terminations” Unused outputs should be left unconnected.
$\overline{\text{OUT0}}$	23	19	O	
OUT1	31	25	O	
$\overline{\text{OUT1}}$	30	24	O	
OUT2	35	31	O	
$\overline{\text{OUT2}}$	34	30	O	
OUT3	38	36	O	
$\overline{\text{OUT3}}$	37	35	O	
OUT4	45	—	O	
$\overline{\text{OUT4}}$	44	—	O	
OUT5	51	—	O	
$\overline{\text{OUT5}}$	50	—	O	
OUT6	54	—	O	
$\overline{\text{OUT6}}$	53	—	O	
OUT7	59	—	O	
$\overline{\text{OUT7}}$	58	—	O	

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 16. Si5347/46 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
	Si5347	Si5346		
Serial Interface				
I2C_SEL	39	38	I	I2C Select. This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high. See note 2.
SDA/SDIO	18	13	I/O	Serial Data Interface. This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when is SPI mode. See Note [2].
A1/SDO	17	15	I/O	Address Select 1/Serial Data Output. In I^2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode this is the serial data output (SDO) pin. See Note [2].
SCLK	16	14	I	Serial Clock Input. This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. See Note [2].
A0/$\overline{CS}$	19	16	I	**Address Select 0/Chip Select.** This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up. See Note [2].

Notes:

1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 16. Si5347/46 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
	Si5347	Si5346		
Control/Status				
INTR	12	17	O	**Interrupt**. This pin is asserted low when a change in device status has occurred. This pin must be pulled-up using an external resistor of at least 1 kΩ. It should be left unconnected when not in use. See Note [2].
RST	6	3	I	**Device Reset.** Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up. See Note [2].
OE0	11	12	I	**Output Enable 0**. This pin is used to enable (when held low) and disable (when held high) the output clocks. By default this pin controls all outputs. It can also be configured to control a subset of outputs. See section 4.8.10 for details. This pin is internally pulled-down. See Note [2].
OE1	41	—		**Output Enable 1**. **(Si5347)** This is an additional output enable pin that can be configured to control a subset of outputs. By default it has no control on the outputs until configured. See section 4.8.10 for details. There is no internal pull-up/pull-down for this pin. See Note [3].
	—	37		**Output Enable 1**. **(Si5346)** This is an additional output enable pin that can be configured to control a subset of outputs. By default it has no control on the outputs until configured. See section 4.8.10 for details. This pin is internally pulled-down. See Note [2].
LOL_A	3	28	O	**Loss Of Lock_A/B/C/D**. These output pins indicate when DSPLL A, B, C, D is out-of-lock (low) or locked (high). They can be left unconnected when not in use. Si5347: See Note [2], Si5346: See Note [3].
LOL_B	4	27	O	
LOL_C	5	—	O	
LOL_D	47	—	O	
LOS_XAXB	25	33	O	**Status Pins.** This pin indicates a loss of signal alarm on the XA/XB pins. This either indicates a XTAL failure or a loss of external signal on the XA/XB pins. This pin can be left unconnected when unused. Si5347: See note 3, Si5346: See Note [2].
DSPLL_SEL0	26	—	I	**DSPLL Select Pins (Si5347 only).** These pins are used in conjunction with the FINC and FDEC pins. The DSPLL_SEL[1:0] pins determine which DSPLL is affected by a frequency change using the FINC and FDEC pins. See section 4.4 for details. These pins are internally pulled-down. See Note [2].
DSPLL_SEL1	27	—	I	

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 16. Si5347/46 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
	Si5347	Si5346		
FDEC	42	—	I	**Frequency Decrement Pin (Si5347 only)**. This pin is used to step-down the output frequency of a selected DSPLL. The frequency change step size is register configurable. The DSPLL that is affected by the frequency change is determined by the DSPLL_-SEL[1:0] pins. See Note 2.
FINC	48	—	I	**Frequency Increment Pin (Si5347 only)**. This pin is used to step-up the output frequency of a selected DSPLL. The frequency change step size is register configurable. The DSPLL that is affected by the frequency change is determined by the DSPLL_-SEL[1:0] pins. See Note 2.
RSVD	20	—	—	**Reserved.** These pins are connected to the die. Leave disconnected.
	21	—	—	
	55	—	—	
	56	—	—	
NC	28	22	—	**No Connect.** These pins are not connected to the die. Leave disconnected.

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 16. Si5347/46 Pin Descriptions (Continued)

Pin Name	Pin Number		Pin Type[1]	Function
	Si5347	Si5346		
Power				
VDD	32	21	P	**Core Supply Voltage**. The device core operates from a 1.8 V supply.
	46	32		
	60	39		
	—	40		
VDDA	13	8	P	**Core Supply Voltage 3.3V.** This core supply pin requires a 3.3 V power source.
	—	9	P	
VDDS	40	26	P	**Status Output Voltage.** The voltage on this pin determines the V_{OL}/V_{OH} on some of the output status pins and V_{IL}/V_{IH} for some control input pins. Connect to 3.3 V or 1.8 V. A 0.1 uF bypass capacitor should be placed very close to this pin.
VDDO0	22	18	P	**Output Clock Supply Voltage 0–7**. Supply voltage (3.3 V, 2.5 V. 1.8 V) for OUTn, $\overline{\text{OUTn}}$ outputs. A 0.1 uF bypass capacitor should be placed very close to this pin. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	29	23	P	
VDDO2	33	29	P	
VDDO3	36	34	P	
VDDO4	43	—	P	
VDDO5	49	—	P	
VDDO6	52	—	P	
VDDO7	57	—	P	
GND PAD	—	—	P	**Ground Pad**. This pad provides connection to ground and must be connected for proper operation.

Notes:
1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

7. Ordering Guide

Ordering Part Number	Number Of DSPLLs	Output Clock Frequency Range	Package	RoHS-6, Pb-Free	Temperature Range
Si5347A-A-GM[1,2]	4	0.0001 to 800 MHz	64-Lead 9x9 QFN	Yes	–40 to 85 °C
Si5347B-A-GM[1,2]		0.0001 to 350 MHz			
Si5346A-A-GM[1,2]	2	0.0001 to 800 MHz	44-Lead 7x7 QFN		
Si5346B-A-GM[1,2]		0.0001 to 350 MHz			
Si5347-EVB	—	—	Evaluation Board	—	—
Si5346-EVB	—	—		—	—

Notes:

1. Add an R at the end of the device part number to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by Silicon Labs. Part number format is: Si5347A-Axxxxx-GM or Si5346A-Axxxxx-GM, where “xxxxx” is a unique numerical sequence representing the pre-programmed configuration.

8. Package Outlines

8.1. Si5347 9x9 mm 64-QFN Package Diagram

Figure 22 illustrates the package details for the Si5347. Table 17 lists the values for the dimensions shown in the illustration.

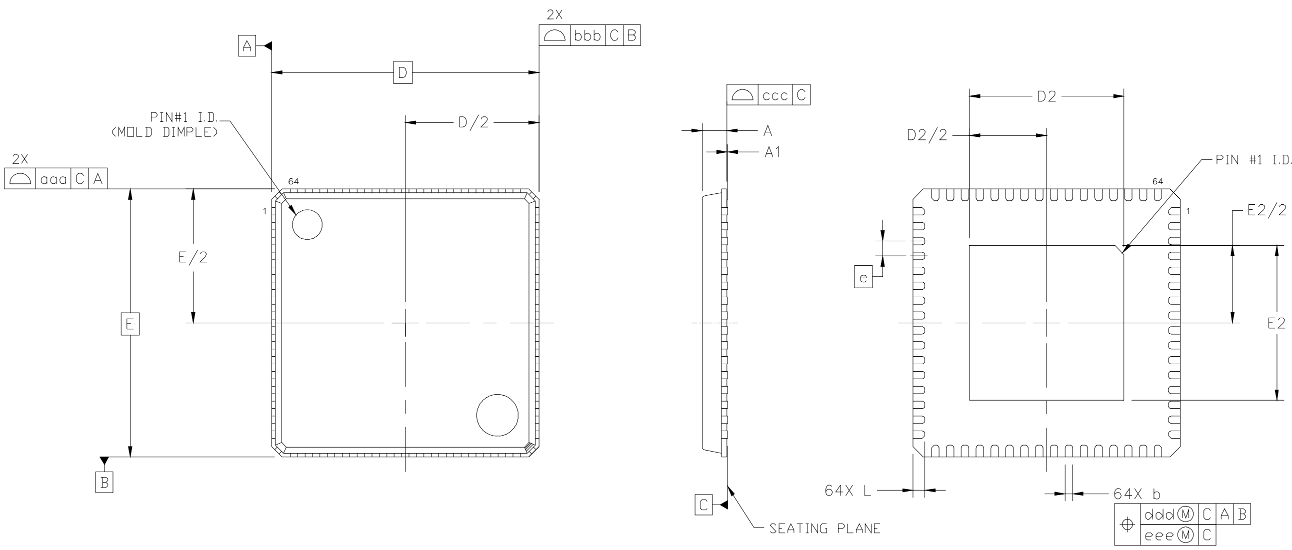


Figure 22. 64-Pin Quad Flat No-Lead (QFN)

Table 17. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	9.00 BSC		
D2	5.10	5.20	5.30
e	0.50 BSC		
E	9.00 BSC		
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2. Si5346 7x7 mm 44-QFN Package Diagram

Figure 23 illustrates the package details for the Si5346. Table 18 lists the values for the dimensions shown in the illustration.

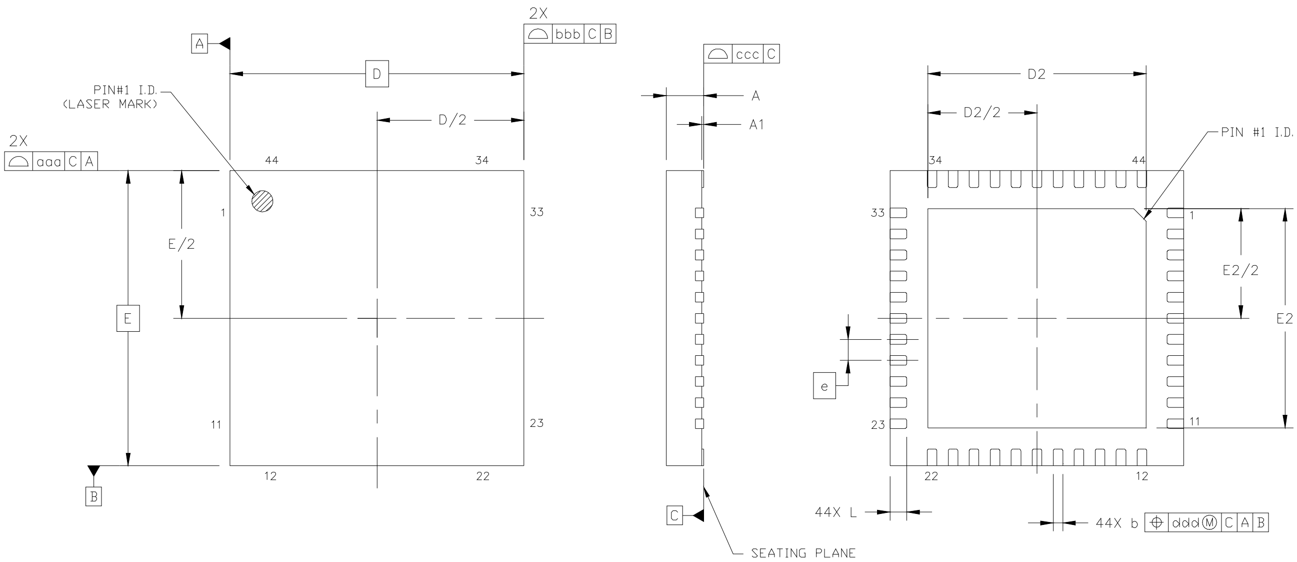


Figure 23. 44-Pin Quad Flat No-Lead (QFN)

Table 18. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	7.00 BSC		
D2	5.10	5.20	5.30
e	0.50 BSC		
E	7.00 BSC		
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. PCB Land Pattern

Figure 24 illustrates the PCB land pattern details for the devices. Table 19 lists the values for the dimensions shown in the illustration.

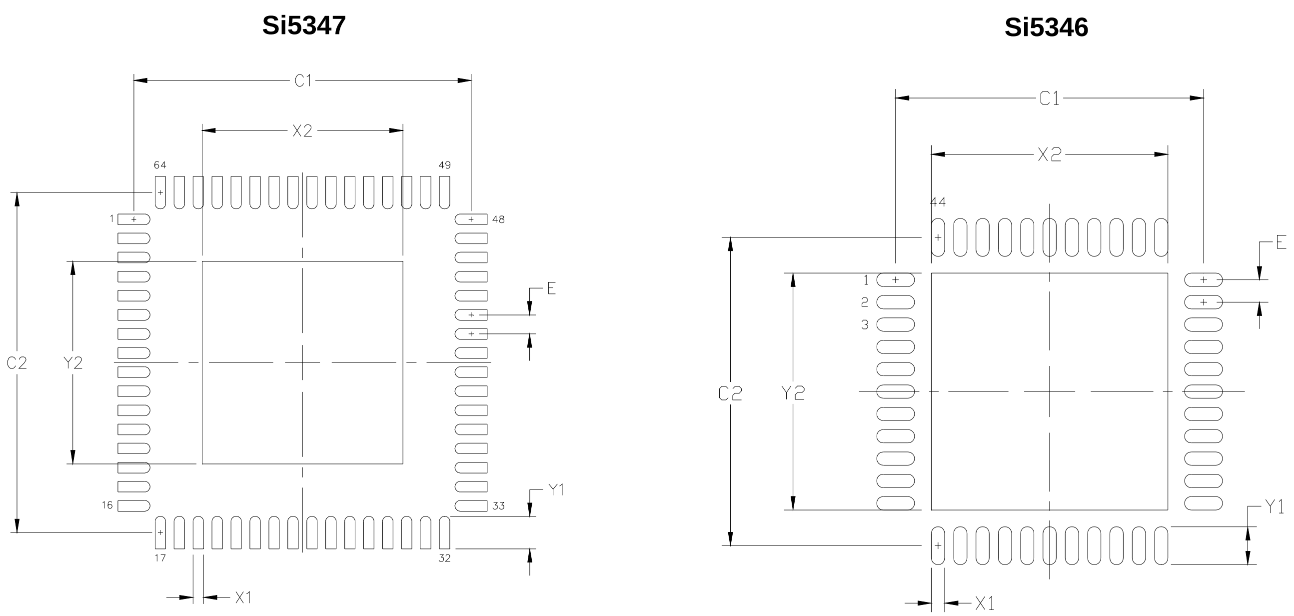


Figure 24. PCB Land Pattern

Table 19. PCB Land Pattern Dimensions

Dimension	Si5347 (Max)	Si5346 (Max)
C1	8.90	6.90
C2	8.90	6.90
E	0.50	0.50
X1	0.30	0.30
Y1	0.85	0.85
X2	5.30	5.30
Y2	5.30	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

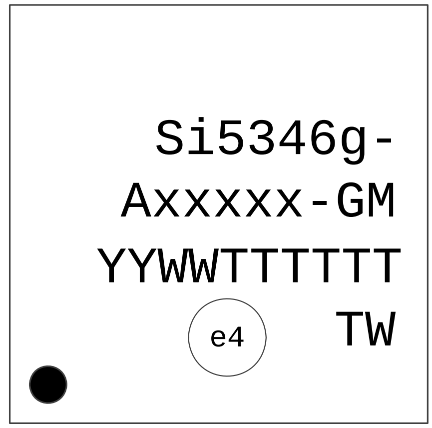
Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Top Marking



Line	Characters	Description
1	Si5347g- Si5346g-	Base part number and Device Grade. Si5347: Quad PLL; 64-QFN Si5346: Dual PLL; 44-QFN g = Device Grade. See Ordering Guide for more information. – = Dash character.
2	Axxxxx-GM	A = Product revision. xxxxx = Customer specific NVM sequence number. (Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices). See "7. Ordering Guide" on page 44 for more information. -GM = Package (QFN) and temperature range (–40 to +85 °C).
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) or 1.4 mm (44-QFN) diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

11. Device Errata

Please log in or register at www.silabs.com to access the device errata document.

APPENDIX—ADVANCE PRODUCT INFORMATION REVISION HISTORY

Table 20 lists the advance product information revision history.

Table 20. Advance Product Information Revision History

Revision	Change Description	Date
0.10	First draft	Aug 2012
0.12	Swapped two serial interface pins ■ SCLK 17 to 19 ■ A1/SDO 19 to 17 Updated the Serial Interface Section (3.5) Updated Section 2 ■ Updated Table 9, 10 ■ Added Table 11, 12 ■ Added Figure 2, 3	Aug 2012
0.13	■ Added Pull-in specification ■ Other minor edits	Dec 2012
0.20	■ Combined Si5347 and Si5346 datasheets ■ Verified pin-outs ■ Added package information	June 2013
0.21	■ Finalized Pinouts ■ Added application diagram ■ Added high level register map information ■ Added DCO description ■ Added gapped clock description ■ Updated the serial interface section	Aug 2013

Table 20. Advance Product Information Revision History (Continued)

Revision	Change Description	Date
0.22	■ Removed OE2 and OE3 pin functions. Updated diagrams. ■ Added P_{REF} divider to Figures 2, 3, 6. ■ Si5347 pin changes: • Renamed pin 13: VDD33 to VDDA • Renamed pins 32, 46, 60: VDD18 to VDD • Changed pin 3 from INTR to LOL_A • Changed pin 4 from LOL_A to LOL_B • Changed pin 5 from LOL_B to LOL_C • Changed pin 6 from I2C_SEL to RST • Changed pin 11 from LOL_C to OE0 • Changed pin 12 from OE0 to INTR • Changed pin 16 from OE1 to SCLK • Changed pin 19 from SCLK to A0/CS • Changed pin 20 from FINC to RSVD • Changed pin 21 from FDEC to RSVD • Changed pin 25 from OE2 to LOS_XAXB • Changed pin 26 from OE3 to DSPLL_SEL0 • Changed pin 27 from A0/CS to DSPLL_SEL1 • Changed pin 39 from RST to I2C_SEL • Changed pin 40 from RSVD to VDDS • Changed pin 41 from RSVD to OE1 • Changed pin 42 from RSVD to FDEC • Changed pin 48 from LOS_XAXB to FINC • Changed pin 55 from OUT7 to RSVD • Changed pin 56 from OUT7 to RSVD • Changed pin 58 from DSPLL_SEL0 to OUT7 • Changed pin 59 from DSPLL_SEL1 to OUT7 ■ Si5346 pin changes: • Renamed pin 8, 9: VDD33 to VDDA • Renamed pins 21, 32, 39, 40: VDD18 to VDD • Renamed pin 26: VDD18 to VDDS	Oct 2013
0.23	■ Change the DCO mode granularity on the front page to 0.01 ppb steps ■ Corrections to the Si5347 pin diagram of section 6-Pin Descriptions: • Renamed pin 28 from RSVD to NC ■ Corrections to the Si5347 pin list of “6. Pin Descriptions” : • Pin 11 OE0 - changed internal pull-up to internal pull-down • Pin 41 OE1 - changed internal pull-up to internal pull-down • Pins 26 (DSPLL_SEL0) and 27 (DSPLL_SEL1) - added internal pull-down • Renamed pin 25 from LOS_XAXB to LOS_XAXB • Renamed pin 28 from RSVD to NC ■ Corrections to the Si5346 pin diagram of “6. Pin Descriptions” : • Renamed pin 22 from RSVD to NC ■ Corrections to the Si5346 pin list of “6. Pin Descriptions” : • Renamed pin 33 from LOS_XAXB to LOS_XAXB • Renamed pin 22 from RSVD to NC • Pin 12 OE0 - changed internal pull-up to internal pull-down • Pin 37 OE1 - changed internal pull-up to internal pull-down	Nov 2013

Table 20. Advance Product Information Revision History (Continued)

Revision	Change Description	Date
0.30	■ Moved the register descriptions to the Si5347/46 Reference Manual. ■ Moved the majority of the contents of the Serial Interface section to the Si5347/46 Reference Manual. ■ Updated LVCMOS output impedance values in Table 14. ■ Added Control Input and Status Output table specifications.	Apr 2014
0.31	■ Added serial interface timing diagrams and specifications ■ Renamed XGND pins to X1, X2	Jun 2014
0.32	■ Minor edits	Jun 2014

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