

Si5386 Evaluation Board User's Guide

The Si5386E-E-EB is used for evaluating the Ultra Low Jitter, Any-Frequency, 12-output JESD204B Clock Generator. The Si5386 employs fourth-generation DSPLL technology to enable clock generation for LTE/ JESD204B applications which require the highest level of jitter performance. The Si5386E-E-EB has four independent input clocks and a total of 12 outputs. The Si5386E-E-EB can be easily controlled and configured using Silicon Labs' Clock Builder Pro[™] (CBPro[™]) software tool.

The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "Si5386E-E-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

EVB FEATURES

- Powered from USB port or external power supply
- Internal 48.0231 MHz crystal provides holdover mode of operation on the Si5386
- CBPro™ GUI programmable VDDO supplies allow each of the ten primary outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro™ GUI-controlled voltage, current, and power measurements of VDD, VDDA, and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5386
- SMA connectors for input clocks, output clocks and optional external timing reference clock



1. Si5386 Functional Block Diagram

Below is a functional block diagram of the Si5386E-E-EB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults or 5.1 Installing ClockBuilderPro (CBPro) Desktop Software for more information.

Note: All Si5386 schematics, BOMs, User's Guides, and software can be found online at the following link: http://www.silabs.com/si538x-4x-evb





2. Quick Start and Jumper Defaults

Perform the following steps to quick-start the ClockBuilderPro software.

- 1. Install ClockBuilderPro desktop software. http://www.silabs.com/CBPro
- 2. Connect a USB cable from the Si5386E-E-EB to the PC where the software was installed.
- 3. Leave the jumpers as installed from the factory, and launch the ClockBuilderPro software.
- 4. You can use ClockBuilderPro to create, download, and verify a frequency plan on the Si5386E-E-EB.
- 5. For the Si5386 data sheet, go to: http://www.silabs.com/si538x-4x-evb.



	5 1				
		Table 2.1. Si5386 EV	/B Jumper Defaults*		ju S
Location	Туре	I = Installed	Location	Туре	I=Installed
		O= Open			O= Open
JP1	2 pin	0	JP23	2 pin	0
JP2	2 pin	0	JP24	3 pin	all open
JP3	2 pin	0	JP25	2 pin	0
JP4	2 pin	I	JP26	3 pin	all open
JP5	2 pin	0	JP27	2 pin	0
JP6	2 pin	0	JP28	3 pin	all open
JP7	2 pin	I	JP29	2 pin	0
JP8	2 pin	0	JP30	3 pin	all open
JP9	2 pin	0	JP31	2 pin	0
JP10	2 pin	0	JP32	3 pin	all open
JP13	2 pin	0	JP33	2 pin	0
JP14	2 pin		JP34	3 pin	all open
JP15	3 pin	1 to 2	JP35	2 pin	0
JP16	3 pin	1 to 2	JP36	3 pin	all open
JP17	2 pin	0	JP39	2 pin	0
JP18	3 pin	all open	JP40	2 pin	0
JP19	2 pin	0	JP41	2 pin	0
JP20	3 pin	all open			
JP21	2 pin	0			
JP22	3 pin	all open	J36	5x2 Hdr	All 5 installed

3. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D11	INTRB	Blue	DUT Interrupt Active
D12	LOLB	Blue	DUT Loss of Lock Indicator
D21	READY	Green	MCU Ready
D22	3P3V	Blue	DUT +3.3 V is present
D24	BUSY	Green	MCU Busy
D25	INTR	Red	MCU Interrupt active
D26	VDD DUT	Blue	DUT VDD voltage present
D27	5VUSBMAIN	Blue	Main USB +5 V present

Table 3.1. Si5386 EVB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5386 +3.3 V, and Si5386 Output +5 V supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. D11 and D12 are status indicators from the DUT.



4. Clock Input and Output Circuits

4.1 Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5386E-E-EB has eight SMA connectors (IN0/IN0B–IN2/IN2B and IN3(FB_IN)/IN3B(FB_INB)) for receiving external clock signals. All input clocks are terminated as shown in the figure below. Note input clocks are ac coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5386 data sheet.



4.2 Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5386E-E-EB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5386E-E-EB, and provide locations on the PCB for optional dc/ac terminations by the end user.



5. Using the Si5386 EVB and Installing ClockBuilderPro (CBPro) Desktop Software

5.1 Installing ClockBuilderPro (CBPro) Desktop Software

To install the CBPro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/cbpro and download the ClockBuilderPro software.

Installation instructions, release notes, and a user's guide for ClockBuilderPro can be found at the download link shown above. Please follow the instructions as indicated.

5.2 Connecting the EVB to Your Host PC

Once ClockBuilderPro software in installed, connect to the EVB with a USB cable as shown below.



5.3 Additional Power Supplies

The Si5386E-E-EB comes preconfigured with jumpers installed on JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain +5 V power to all EVB power solely through the J37 USB connector. This setup is the default EVB configuration and is sufficient to configure the device and run multiple clock outputs simultaneously.

In some cases when enabling all outputs or at high output frequencies, the EVB requires more power than a single USB connection can provide. This may result in intermittent device behavior or unexplained increases in jitter/phase-noise. This condition may be checked using the EVB GUI, which is described further below. Selecting the "**All Voltages**" tab of the GUI and clicking on the "**Read All**" button produces a display similar to this one:



Figure 5.2. EVB GUI - Power Supply Check

Verify that the "**RAIL_5V**" measurement shows the EVB voltage > 4.7 V. An EVB voltage lower than this level may cause the issues described above.

In this case, J33 can be used to provide power to the output drivers separately from the main Si5386 device supplies. To make this change, move jumper JP15 to connect pins 2-3 "EXT". Connect J33 to an external 5 V, 0.5A or higher, power source. Make sure that the polarity of the +5 V and GND connections are correct. Verify that the RAIL_5V voltage is 4.7 V or higher. The EVB should be powered by the USB connector when turning this auxiliary 5 V supply on or off.

See the figure below for the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.



5.4 Overview of ClockBuilderPro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilderPro installer will install two main applications.

Application 1:





Use the CBPro Wizard to do the following:

- · Create a new design.
- · Review or edit an existing design.
- Export: Create in-system programming files.

Application 2:

	Si5386 Rev D EVB	- ClockBuilder Pro	×				
	File Help						
	Info DUT SPI	DUT Register Editor	Regulator	All Voltages	GPIO Sta	tus Registers	
				Voltage	Current	Power	
	VDD	1.80V	Off	1.786 V	268 mA	479 mW	Read
	VDDA	3.30V	Off	3.290 V	129 mA	424 mW	Read
	VDDO0	2.50V	Off	2.485 V	49 mA	122 mW	Read
	VDD01	2.50V	Off	2.481 V	22 mA	55 mW	Read
	VDDO2	2.50V	Off	0.001 V	0 mA	0 mW	Read
	VDDO3	2.50V	Off	2.497 V	24 mA	60 mW	Read
	VDDO4	2.50V	Off	0 V	0 mA	0 mW	Read
	VDDO5	2.50V	Off	2.468 V	16 mA	39 mW	Read
$\sim \circ$	VDDO6	2.50V	Off	0.006 V	0 mA	0 mW	Read
	VDDO7	2.50V	Off	2.481 V	16 mA	40 mW	Read
	VDDO8	2.50V	Off	0.008 V	0 mA	0 mW	Read
X	VDDO9	2.50V	Off	2.480 V	16 mA	40 mW	Read
	All Output	- Select Voltage		Total	540 mA	1.259 W	Read All
	Supplies	Power On Po	ower Off	Compa	re Design Esti	mates to Meas	urements

Figure 5.5. EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5386).
- · Control the EVB's regulators.
- · Monitor voltage, current, power on the EVB.

Designe

5.5 Common ClockBuilderPro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5386E-E-EB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-created Device Configuration
- Workflow Scenario #3: Testing a User-created Device Configuration

Each is described in more detail in the following sections.

5.6 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

Verify that the PC and EVB are connected, then launch ClockBuilder Pro by clicking on this icon on your PC's desktop:



Figure 5.6. ClockBuilder Pro Icon

CBPro automatically detects the EVB and device type. When the EVB has been detected, click on the "Open Default Plan" button.

SILICON LABS	ClockBuilder Pro We Make Timing Simp
Work With a Desig	yn
Create New [Design
늘 Open Design	Project File
ex Open Sample	2 Design
Evaluation Bo	Open Default Plan EVB GUI

Figure 5.7. CBPro—Open Default Plan Button

Once you open the default plan, a popup will appear.

ClockBuilder Pro v2.15.7	De te	
The EVB may be out-of-sync w your design to the EVB?	vith your design.	Would you like to write

Figure 5.8. CBPro—Write Design Dialog

Select "Yes" to write the default plan to the Si5386 device mounted on your EVB. This ensures the device on the EVB is configured with the latest parameters from Silicon Labs. Jesil

Si5386E Design Write	10	Expost	×
Writing Si5386E Design to EVB			
Address 0x0325			

Figure 5.9. CBPro—Write Progress Window

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown in the figure below

Si538	6 EVB Default Configuration - ClockBuilder Pro	
Cloc	kBuilder Pro v2.15.7 🍫 (standard frequency planner)	(no setting overrides) SILICON LABS
Desigr	n Dashboard 🔻	Configuring Si5386E Rev D
You	have not made any edits to the default Si5386E EVB configuration	in.
**	Edit Configuration with Wizard Desian ID. & Notes - Revision - Host Interface - Internal Reference - Free Run - ZDM - Inputs - Input Select - Outputs - Output Skew - DSPLL - LOS - OOF - LOL - INTR	Evaluation Board Detected Si5386 Rev DubVB Write Parsion OLEVB Open EVB GUI

Figure 5.10. CBPro-Open EVB GUI Button

The EVB GUI window will appear on the desktop. Note all power supplies on the "Regulators" tab will be set to the values defined in the device's default CBPro project, as shown in the figure below.

Photo Laboration					
File Help					
Info DUT SPI	DUT Register Edit	Regulators All Voltage	s GPIO	Status Registers	
	\mathbf{O}	Voltage	Current	Power	
VD	D 1.80V	Off 1.786 V	268 mA	479 mW	Read
VDC	3.30V	OII 3.290 V	129 mA	424 mW	Read
VDDC	2.50V	0ff 2.485 V	49 mA	122 mW	Read
VDDC	2.50V	Off 2.481 V	22 mA	55 mW	Read
VDDC	2.50V	Off 0.001 V	0 m/	0 mW	Read
VDDC	03 2.50V	Off 2.497 V	24 mA	60 mW	Read
VDDC	2.50V	Off 0 V	0 mA	0 mW	Read
VDDC	05 2.50V	Off 2.468 V	16 mA	39 mW	Read
VDDC	06 2.50V	Off 0.006 V	0 m.4	0 mW	Read
VDDC	07 2.50V	Off 2.481 V	16 mA	40 mW	Read
VDDC	2.50V	0.008 V	0 m/	0 mW	Read
VDDC	9 2.50V	Off 2.480 V	16 m.A	40 mW	Read
All Output	Select Voltage	Total	540 m/	A 1.259 W	Read A
Supplies	Power On	Power Off Comp	are Design I	Estimates to Meas	urements

5.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have yet been connected to the INPUT CLOCK differential SMA connectors, labeled "INx/INxB" and located around the perimeter of the EVB, the DUT should now be operating in free-run mode and locked to the internal crystal.

You can run a quick check to determine if the device is powered up, generating output clocks, and consuming power by clicking on the "**Read All**" button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Turning V_{DD} or V_{DDA} "Off" will power-down and reset the DUT. Once both of these supplies are turned "On" again, you must reload the desired frequency plan back into the device memory by selecting the "**Write Design to EVB**" button on the CBPro home screen:



Figure 5.12. CBPro—Write Design Button

Failure to do the step above will cause the device to read in the preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks, running in free-run mode from the crystal, using external instrumentation connected to the output clock SMA connectors, labeled OUTx/OUTs. To verify plan inputs, go to the appropriate configuration page or click on "**Frequency Plan Valid**" to see the design report.



Figure 5.13. CBPro—Design Report Button and Link

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

sign Report		
art:	S15386E Rev D	
esign ID:	<none></none>	
reated By:	ClockBuilder Pro v2.15.7 [2017-07-06]	
imestamp:	2017-07-12 15:04:01 GMT-05:00	
esign Rule	Check	
rrors:		
No errors		
arnings:		
DSPLL: nor	-default OLPD gain of 16x may reduce input jitter tolerance	
esign		
lost Interfa	C0:	
I/O Power	Supply: VDD (Core)	
SPI Mode:	4-Wire	
I2C Addre	ss Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins)	8
nternal Ref	erence:	
48.0231 M	Hz [48 + 231/10000 MHz] (XTAL - Crystal)	
nputs:		
INU: Unu	sed	
IN1: 30.	72 MHz [30 + 18/25 MHz]	
Sta	ndard	
IN2: Unu	sed	
IN3: Unu	ised	
-		
utputs:		
OUTUA: 2.9	4912 GHz [2 + 2966/3125 GHz]	
Ena	bled, High-Speed Diff 2.5 V	
OUT0: Unu	sed	
OUT1: 983	.04 MHz [983 + 1/25 MHz]	
	L1_J TIMA 1 E H	
copy to Clipbo	ard Save Report Ask for Help	Close

Figure 5.14. CBPro—Design Report

5.6.2 Verify Locked Mode Operation

Now, assuming that you connect the input clocks to the EVB as shown in the Design Report above, the DUT on your EVB will be running in "locked" mode.

5.7 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the configuration using the CBPro Wizard, click on the appropriate category. The category may also be selected from a dropdown list by clicking on the "**Design Dashboard**" button above this section.

SI5386 EVB Default Configuration - ClockBuilder Pro	
ClockBuilder Pro v2.15.7 🍫	SILICON LABS
esign Dashboard	Configuring Si5386E Rev D
You have made edite to the EVB design. You can also save your new con Design to Project File" link.	nfiguration to a project file for future use by clicking the "Save
Edit Configuration with Wizard Desian ID & Notes · Revision · Host Interface · Internal Reference · Eree Run · ZDM · Inputs · Input Select · Outputs · Output Skew · DSPLL · LOS · OOF OL · INTR	Evaluation Board Detected SI5386 Rev D EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a draft datasheet addendum (PDF) for your design.	Documentation Si5380 Rev D Reference Manual Si5380 Rev D Datasheet
Silicon Labs Cloud Services You can <u>create a custom part number</u> for your design, which can be used to order factory pre-programmed devices. Or <u>request a phase noise report</u> for this design.	Ask for Help Have a question about your design? Elick here to get assistance.
🕒 Frequency Plan Valid 🚺 1 Warning 🛞 Pd: 1.186 W, Tj: 95 °C	Home Close

Figure 5.15. CBPro—Edit Settings Links and Pulldown

You will now be taken to the Wizard's step-by-step menu pages to allow you to change any of the default plan's operating configurations.

Step 1 of 15 - Design ID & Notes	Gonfiguring Si5386E R
Design ID The device has 8 registers, DESIGN_ID0 through 0ESIGN_ID7, that can be used to Design ID: 5386EV81 tophionals max & characters) The stifting you enter here is stored as ASCII bytes in register Padding Mode: If you'do not enter the full 8 characters, the remaining thatacter). Space Padded If you do not enter the full 8 characters, the remaining character). Design Note Enterlamything you want here. The text is stored in your project file and included While the text is word wrapped in reports, you can use newlines to start a new p	o store a design/configuration/revision identifier. rs DESIGN_ID0 through DESIGN_ID7. bytes of DESIGN_IDx will be padded with 0x00 bytes (aka NULL bytes of DESIGN_IDx will be padded with 0x20 bytes (space

Figure 5.16. CBPro—Design ID and Notes Edit Page

4

As you edit the settings, you may notice the "Frequency Plan Valid" link in the lower left corner updating. You can click on this link to bring up the design report to confirm that the information is correct. When you are finished editing each page, you may click on the "> Next" or "< Back" buttons to move from page to page. When you are done making all your desired changes, you can click on "Write to EVB" to reconfigure your device. The Design Write status window will appear each time you write to the EVB.

Writing Si5386E D	esign to EVB	
Address 0x0325		

Figure 5.17. CBPro—Design Write Progress Window

ris ertre When you have verified your design settings, you may save the design project. Click on the "Finish" button to return to the home page and then click on the "Save Design to Project File" link. You can use the windows file browser to reach the correct location and enter a filename for this new project.

5.8 Workflow Scenario #3: Testing a User-Created Device Configuration



Figure 5.18. CBPro—Open Design Project Link

Using the windows file browser popup, locate your CBPro design file (*.slabtimeproj or *.sitproj file).



Figure 5.19. CBPro—Windows File Browser

Select "Yes" when the WRITE DESIGN to EVB popup appears:



The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

5.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

gn Dashboard 🔻	Configuring Si5386E Rev D
fault plan for Si5386 EVB has been loaded. You can make edits to t	ne EVB's configuration using the interactive Wizard.
Edit Configuration with Wizard Desian ID & Notes - Revision - Host Interface - Internal Reference - Free Run - ZDM - Inputs - Input Select - Outputs - Output Skew - DSPLL - LOS - OOF - LOL - INTR	Evaluation Board Detected Si5386 Rev D EVB Write Design to EVB Open EVB GUL
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	Export ou carrexport your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation Si5380 Rev D Reference Manual Si5380 Rev D Datasheet
Silicon Labs Cloud Services You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Charbere to get assistance.

Figure 5.21. CBPro-Export Design Programming File

You can now write your device's complete configuration to file formats suitable for in-system programming.

📰 Si5386	E Export
Introd	uction Register File Settings File Multi-Project Register/Settings Regmap
Abo Thi ach Pile wri cor	at Register Export is export will contain the registers that need to be written (in sequence) to the Si538x/4x device to ieve your design/configuration see refer to the Si538k/4x Family Reference Manual for information on register addressing and how to a the data contained written this export. command line version of this tool is available. Type CBProProjectRegistersExport help from a nmand prompt to learn more.
Opt Exp	ons art Type: Comma Separated Values (CSV) File EactWine in the file is an address,data pair in hexadecimal format. A comma separates the address and data fields. C Code Header File The register write sequence is expressed in C code via an array of address,data pairs. This can be used directly in firmware code.
G	nclude summary header f checked, an informational header will be included at the top of the file. Each line in the header will be refixed by the # character. The header will contain some basic information about the design, tool, and a timestamp.
	Include pre- and post-write control register writes Zertain control registers must be written before and after writing the volatile configuration registers. This ensures the device is stable during configuration download and resumes normal operation after the download is complete. You can turn inclusion of this sequence off if your host system is managing this process already.
	Preview Export Save to File

Figure 5.22. CBPro—Export Configuration Window

6. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

The Si5386 device loads the Non-Volatile Memory (OTP) on either a powerup or a hard reset, overwriting any previous volatile register changes. This allows the device to begin functioning as desired on powerup/hard-reset without manual intervention. To restart the device while preserving volatile changes and without loading the OTP, use soft-reset through the registers or EVB-GUI.

Note: Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5386 using ClockBuilder-Pro on the Si5386 EVB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5386 RAM space and can be done virtually an unlimited number of times. Writing to OTP is limited as described below.

Recommended Refer to the Si5386 Family Reference Manual and device datasheet for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of two times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

7. Serial Device Communications (Si5386 <-> MCU)

7.1 Onboard SPI Support

The MCU on-board the Si5386E-E-EB communicates with the Si5386 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5386 device is the SPI slave. The Si5386 device can also support a 2-wire I²C serial interface, although the Si5386E-E-EB does NOT support the I²C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I²C.

7.2 External I²C Support

I²C can be supported if driven from an external I²C controller. The serial interface signals between the MCU and Si5386 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I²C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5386 device. The shunt at J4 (I2C_SEL) must also be removed to select I²C as Si5386 interface type. An external I²C controller connected to the Si5386 side of J36 can then communicate to the Si5386 device. (For more information on I²C signal protocol, please refer to the Si5386 data sheet.)

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5386 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4, I²C operation should use J36 pin 4 (DUT_SDA_SDIO) as the I²C SDA and J36 pin 8 (DUT_SCLK) as the I²C SCLK. Please note the external I²C controller will need to supply its own I²C signal pull-up resistors.



Figure 7.1. Serial Communications Header J36

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8. Si5386E-E-EB Schematic and Bill of Materials (BOM)

The Si5386 EVB Schematic and Bill of Materials (BOM) can be found online at: http://www.silabs.com/si538x-4x-evb

Note: Please be aware the Si5386 EVB schematic is in OrCad Capture *hierarchical format* and not in a typical "flat" schematic format.

Recommended for New Desit



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