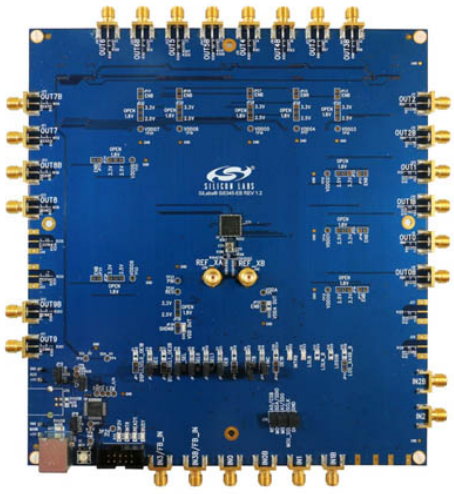
UG352: Si5391A-A Evaluation Board User's Guide

The Si5391A-A-EVB is used for evaluating the Si5391A Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier revision D. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text “SI5391-A-EB” installed in the lower left hand corner of the board. (For ordering purposes only, the terms “EB” and “EVB” refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

EVB FEATURES

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL allows free-run mode of operation on the Si5391A or up to 3 input clocks for synchronous clocking.
- Feedback clock input for optional zero delay mode.
- ClockBuilder® (CBPro) GUI programmable VDD supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI programmable VDDO supplies allow each of the 10 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies.
- Status LEDs for power supplies and control/status signals of Si5391A.
- SMA connectors for input and output clocks.



1. Functional Block Diagram

Below is a functional block diagram of the Si5391A-A-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See Section 3. Quick Start or Section 8. Installing ClockBuilder Pro Desktop Software for more information.

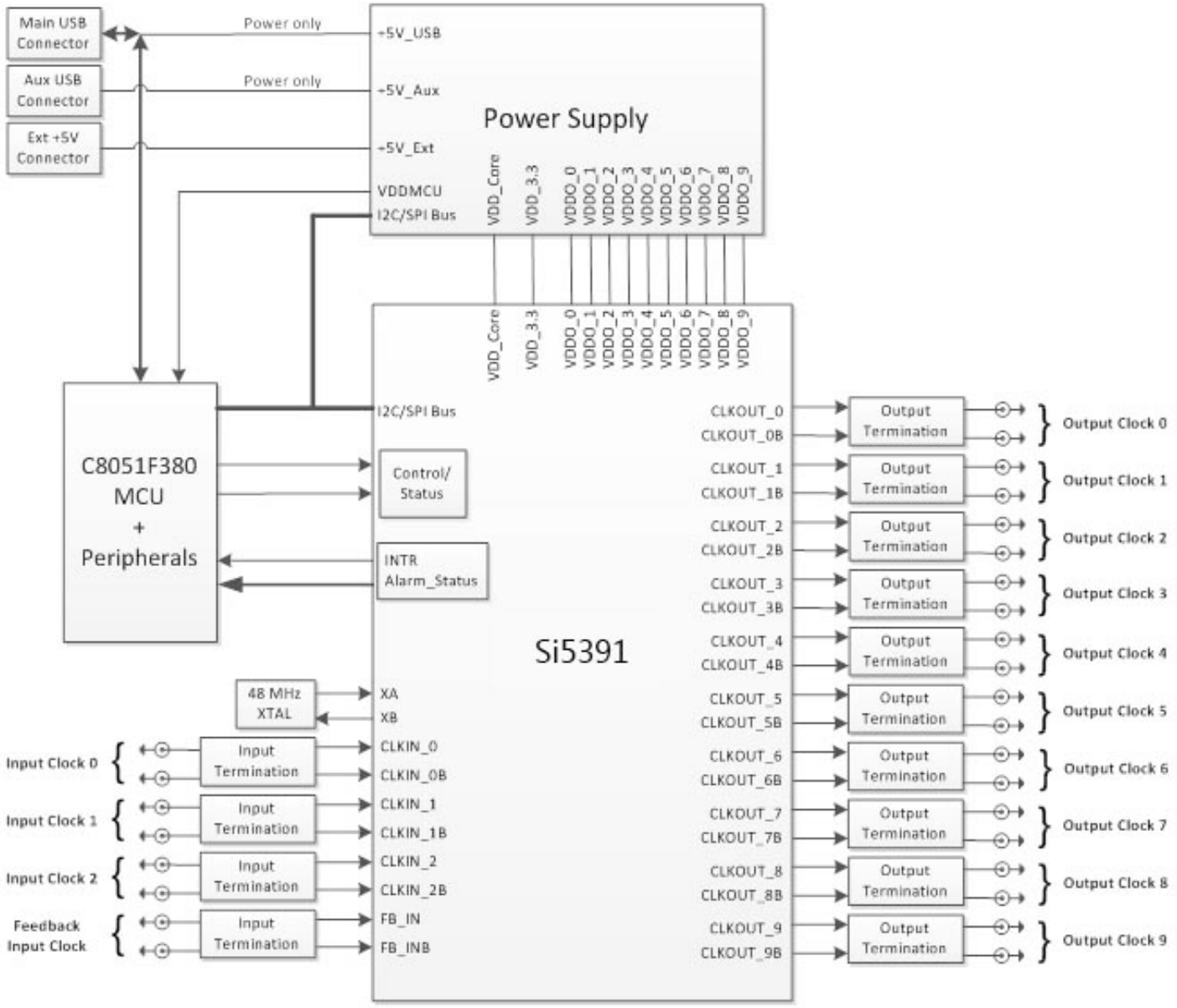


Figure 1.1. Si5391A-A EB Functional Block Diagram

2. Si5391A-A-EVB Support Documentation and ClockBuilder Pro Software

All Si5391A-A-EVB schematics, BOMs, User’s Guides, and software can be found online at the following link: Clock Development Tools

3. Quick Start

1. Install ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.
2. Connect a USB cable from Si5391A-A-EB to the PC where the software was installed.
3. Confirm jumpers are installed as shown in Table 4.1 Si5391A-A-EB Jumper Defaults on page 5.
4. Launch the ClockBuilder Pro Software.
5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5391A-A-EB.
6. For the Si5391A data sheet, go to http://www.silabs.com/timing.

4. Jumper Defaults

Table 4.1. Si5391A-A-EB Jumper Defaults

Location	Type	I = Installed 0 = Open		Location	Type	I = Installed 0 = Open
JP1	2 pin	O		JP23	2 pin	O
JP2	2 pin	I		JP24	2 pin	O
JP3	2 pin	O		JP25	2 pin	O
JP4	2 pin	I		JP26	2 pin	O
JP5	2 pin	I		JP27	2 pin	O
JP6	2 pin	I		JP28	2 pin	O
JP7	2 pin	I		JP29	2 pin	O
JP8	2 pin	I		JP30	2 pin	O
JP9	2 pin	O		JP31	2 pin	O
JP10	2 pin	I		JP32	2 pin	O
JP13	2 pin	O		JP33	2 pin	O
JP14	2 pin	I		JP34	2 pin	O
JP15	3 pin	1 to 2		JP35	2 pin	O
JP16	3 pin	1 to 2		J36	2 pin	O
JP17	2 pin	O		JP38	3 pin	All Open
JP18	2 pin	O		JP39	2 pin	O
JP19	2 pin	O		JP40	2 pin	O
JP20	2 pin	O		JP41	2 pin	O
JP21	2 pin	O		J36	5 x 2 Hdr	All 5 installed
JP22	2 pin	O				

Note: Refer to the Si5391A-A-EB schematics for the functionality associated with each jumper.

5. Staus LEDs

Table 5.1. Si5391A-A-EB Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy

D27, D22, and D26 are illuminated when USB +5 V, Si5391A +3.3 V, and Si5391A VDD supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity.

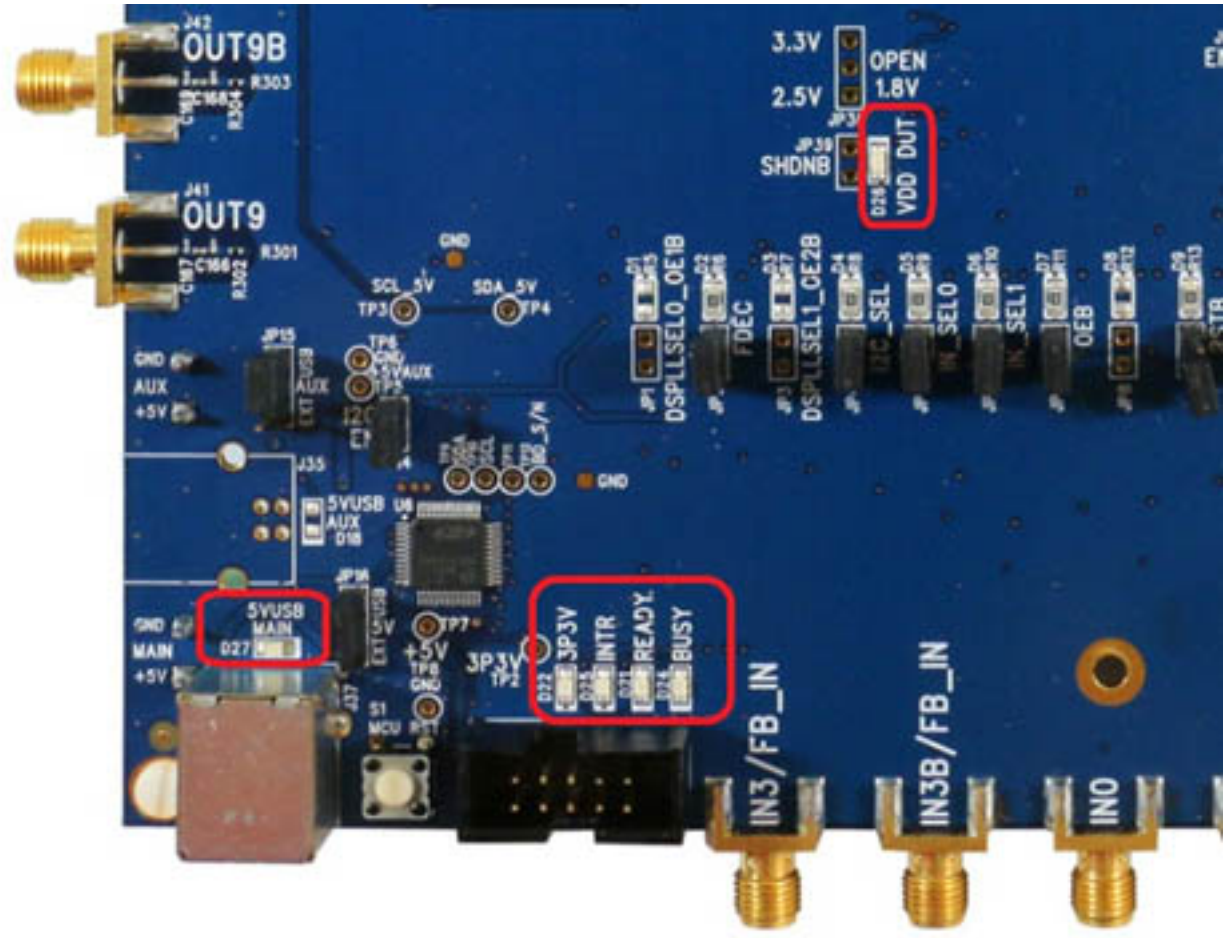


Figure 5.1. Status LEDs

6. Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5391A-A-EB has eight SMA connectors (IN0/IN0B–IN2/IN3B and FB_IN/FB_INB) for receiving external clock signals. All input clocks are terminated as shown in figure below. Note input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5391 Data Sheet.

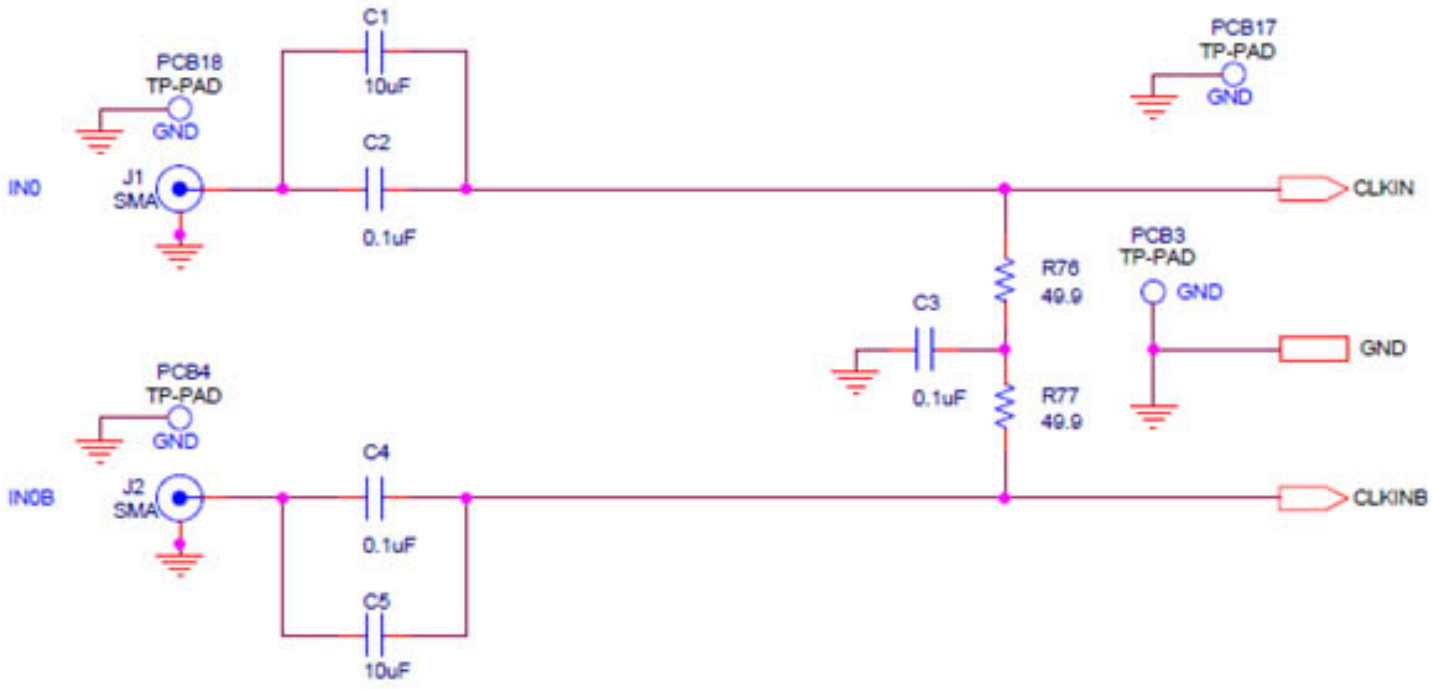


Figure 6.1. Input Clock Termination Circuit

7. Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5391A-A-EVB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic “NI” designation are not normally populated on the Si5391A-A-EB and provide locations on the PCB for optional dc/ac terminations by the end user.

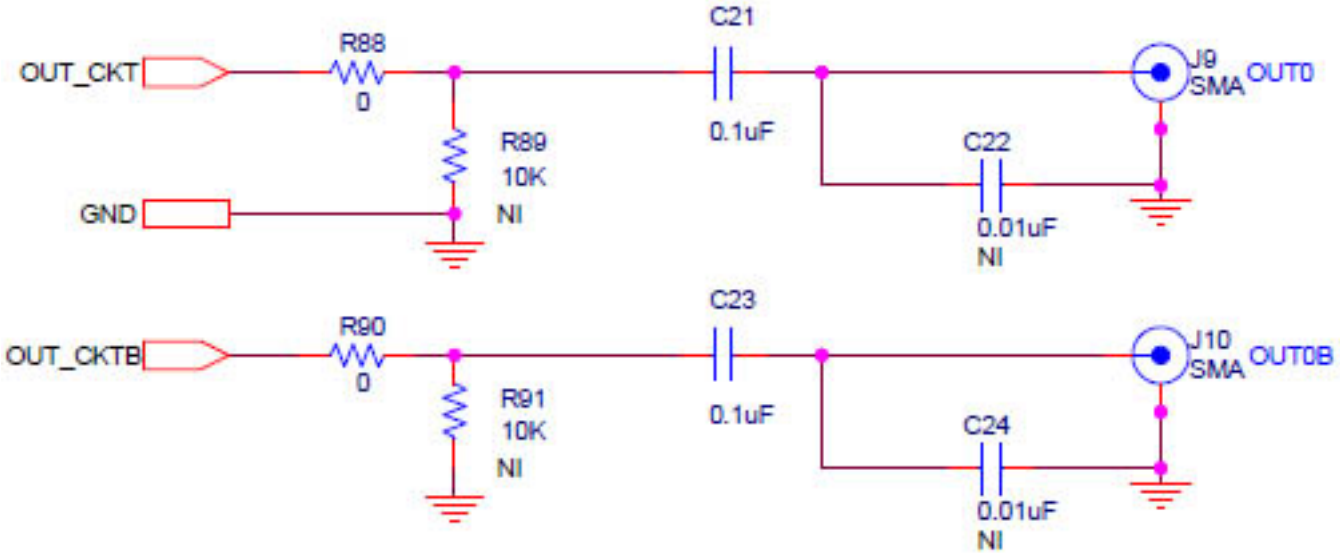


Figure 7.1. OUtput Clock Termination Circuit

8. Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any **Windows 7 or Windows 10** PC, go to http://www.silabs.com/CBPro and download ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above. Follow the instructions as indicated.

9. Using the Si5391A-A-EVB

9.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the evaluation board with a USB cable as shown below.

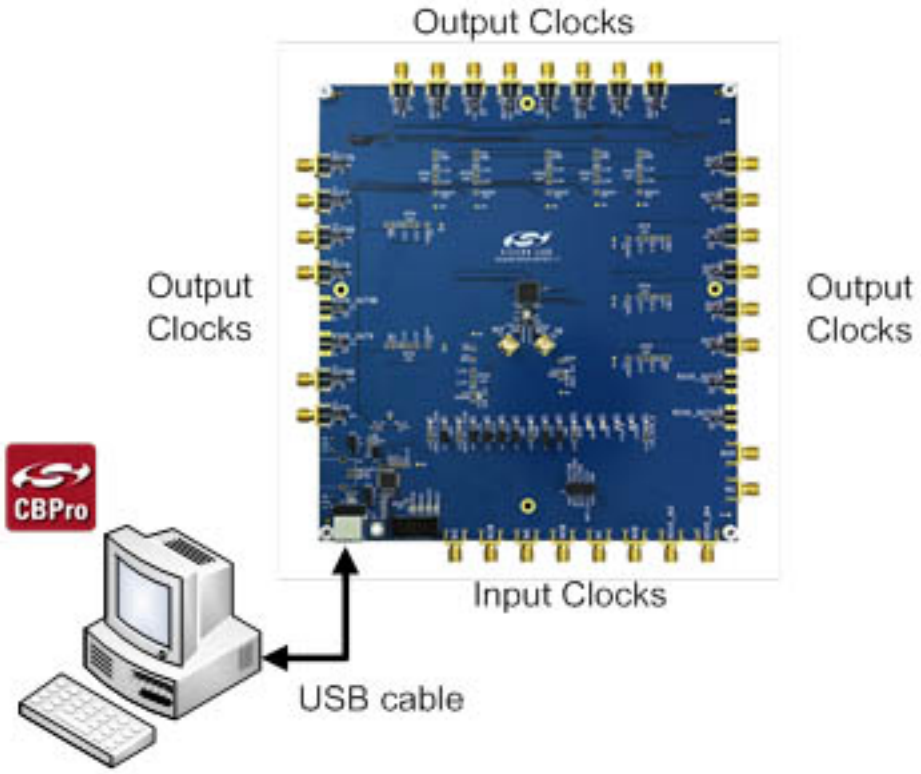


Figure 9.1. EVB Connection Diagram

9.2 Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is not needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5391A-A-EB schematic for details.

The Si5391A-A-EB comes preconfigured with jumpers installed at JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The figure below shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

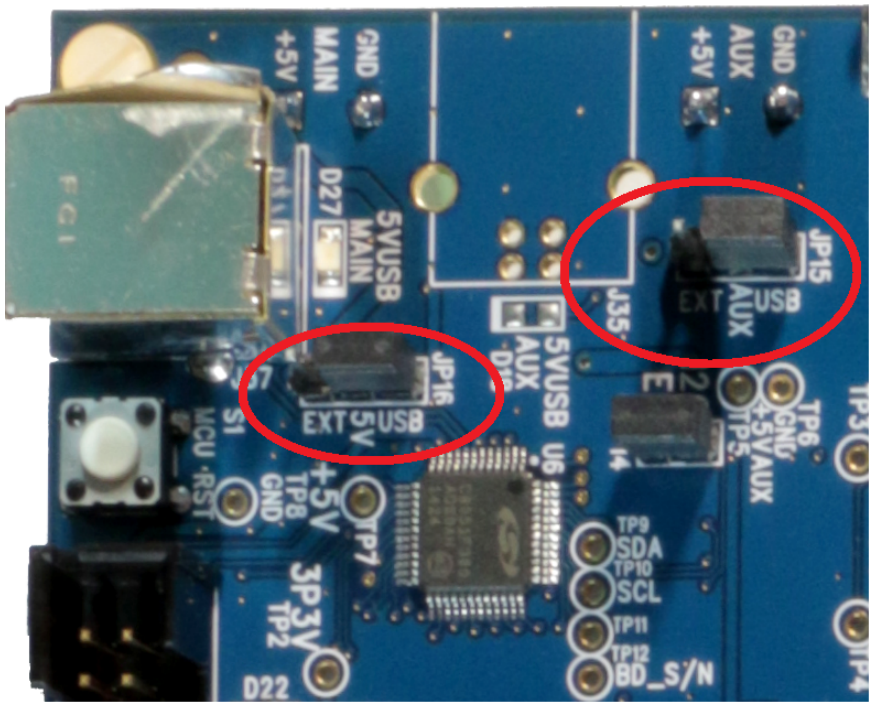


Figure 9.2. JP15-JP16 Standard Jumper Shunt Installation

Note: Some early versions of the 64-pin Si534x-EBs may have the silkscreen text at JP15-JP16 reversed regarding EXT and USB, i.e., USB EXT instead of EXT USB. Regardless, the correct installation of the jumper shunts for default or standard operation is on the right hand side as read and viewed in the figure above.

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, re-configure the EB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
  - Connect external +5 V power supply to terminal block J33 on the back side of the PCB.
  - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.

9.3 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilder Pro installer will install **two** main applications:

Figure 9.3. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to:

- Review or edit an existing design
- Export: Create in-system programming
- Create a new design

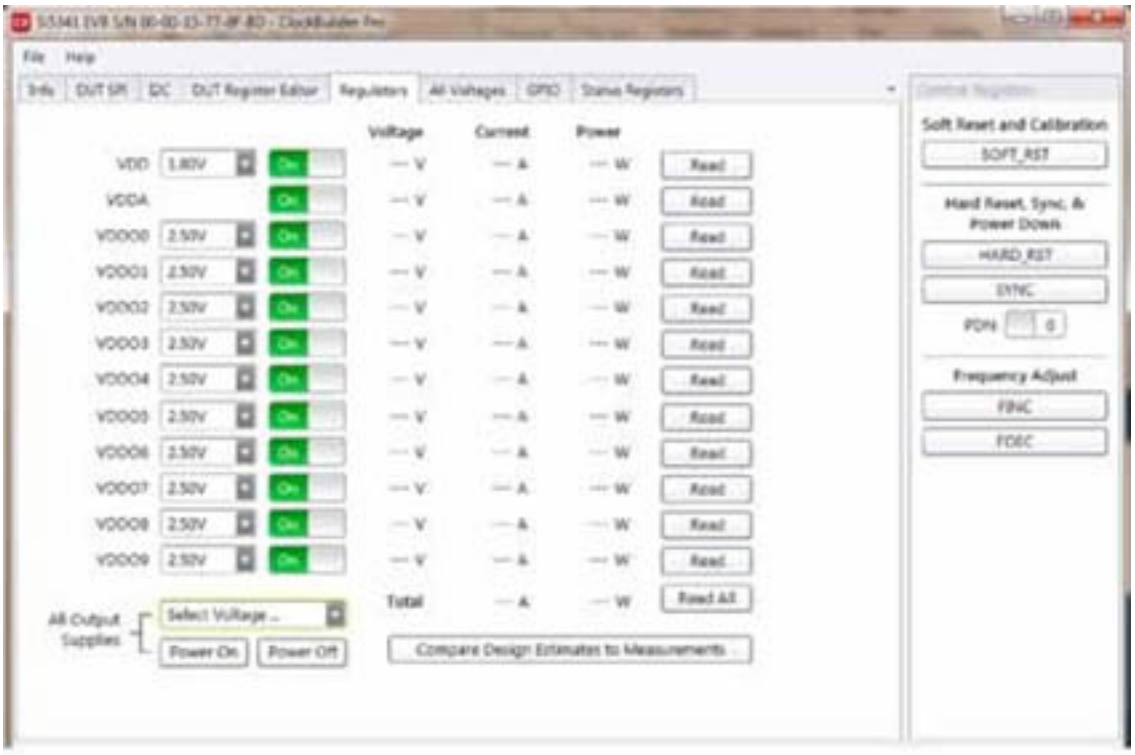


Figure 9.4. Application #2: EVB GUI

Use the EVB to:

- Download configuration to EVB's DUT (Si5391A)

- Control the EVB's regulators
- Monitor voltage, current, power on the EVB

9.4 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5391A-A-EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration Each

Each workflow is described in more detail in the following subsections.

9.5 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch **ClockBuilder Pro** by clicking on this icon on your PC's desktop.

Figure 9.5. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

Figure 9.6. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.

Figure 9.7. Write Design to EVB Dialog

Select “Yes” to write the default plan to the Si5391A device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

Figure 9.8. Writing Design Status

After CBPro writes the default plan to the EVB, click on “Open EVB GUI” as shown below.

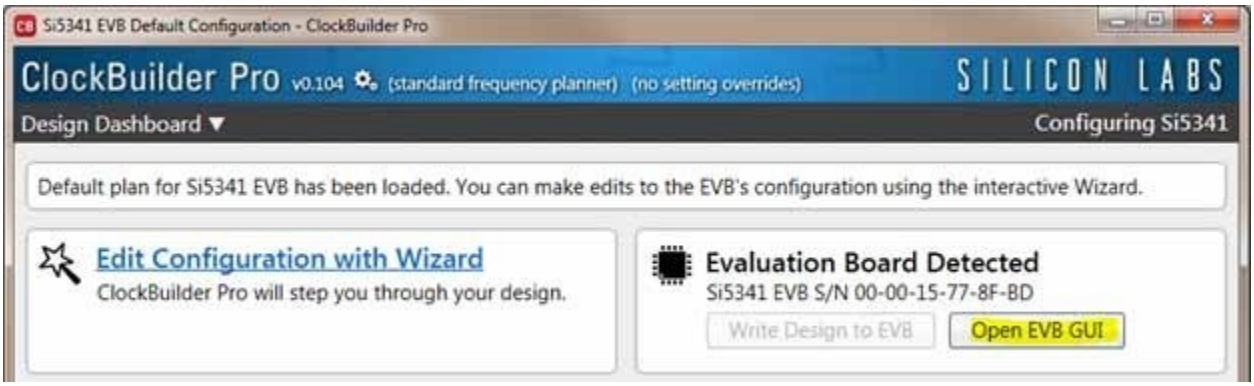


Figure 9.9. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device’s default CBPro project file created by Silicon Labs, as shown below.

Figure 9.10. EVB GUI Window

9.5.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled “INx/INxB”) located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting “Off” then “On” of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT’s register space, you must go back to the Wizard’s main menu and select “Write Design to EVB”:

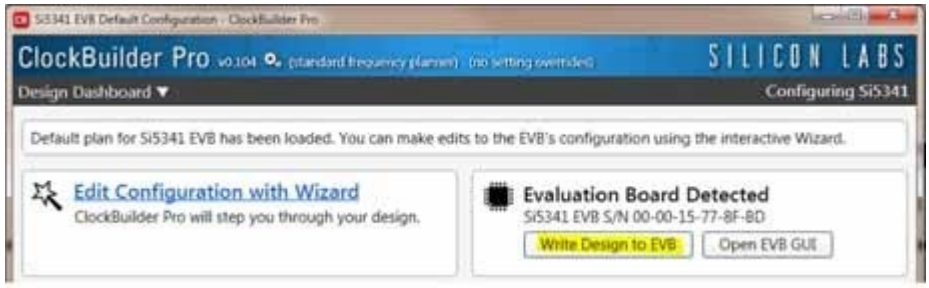


Figure 9.11. Write Design to EVB

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below

Figure 9.12. View Design Report

Your configuration’s design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project’s Design Report.

Figure 9.13. Design Report Window

9.5.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in “locked” mode.

9.6 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the “default” configuration using the CBPro Wizard, click on Edit Configuration with Wizard:

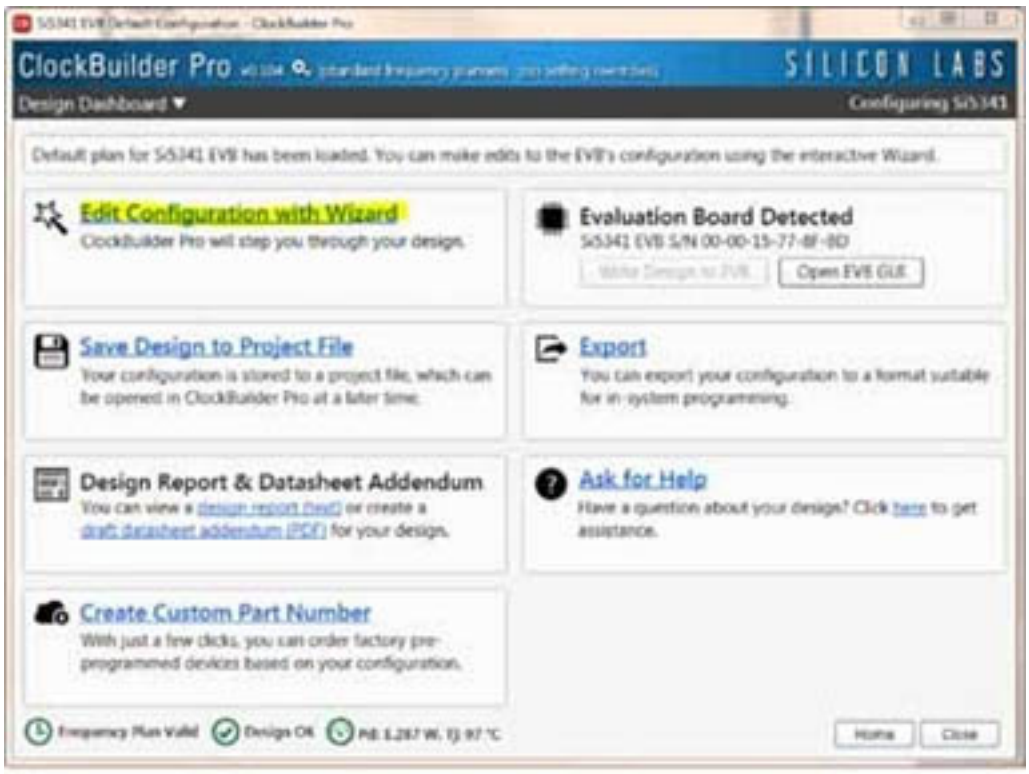


Figure 9.14. Edit Configuration with Wizard

You will now be taken to the Wizard’s step-by-step menus to allow you to change any of the default plan’s operating conditions

Figure 9.15. Design Wizard

Note: You can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

Figure 9.16. Writing Design Status

9.7 Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

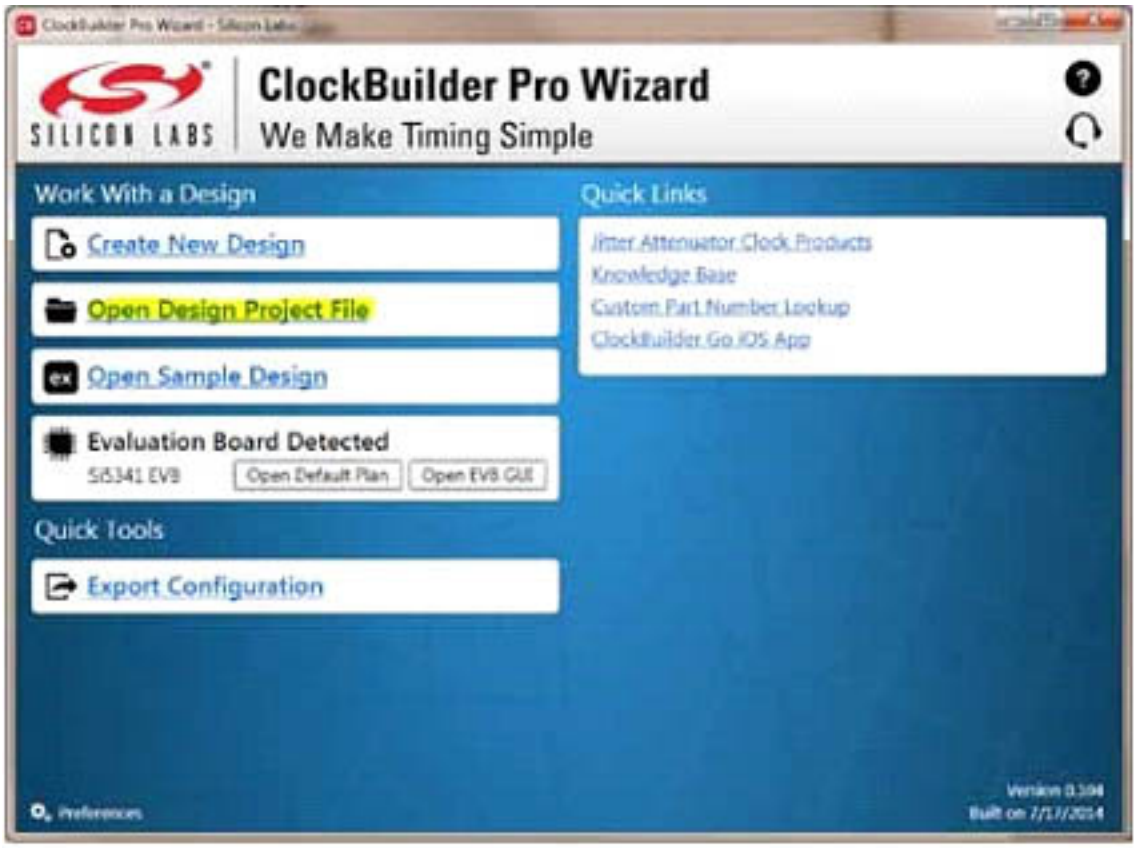


Figure 9.17. Open Design Project File

Locate your CBPro design file (`*.slabtimeproj` or `*.sitproj file`).design file in the Windows file browser.

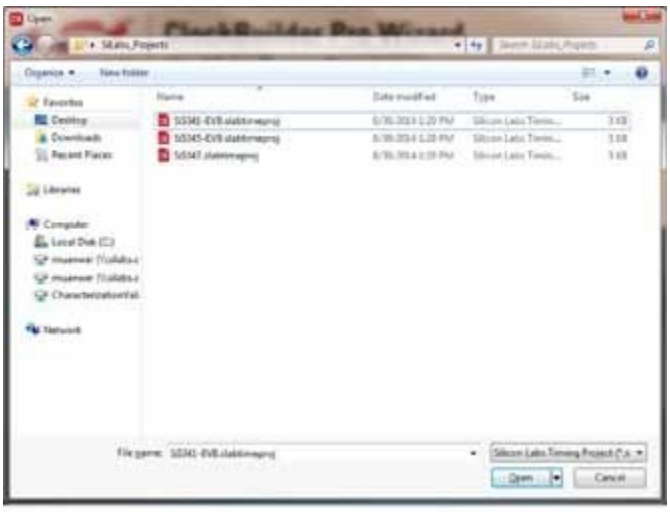


Figure 9.18. Browse to Project File

Select [**Yes**] when the WRITE DESIGN to EVB popup appears:

Figure 9.19. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

9.8 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:

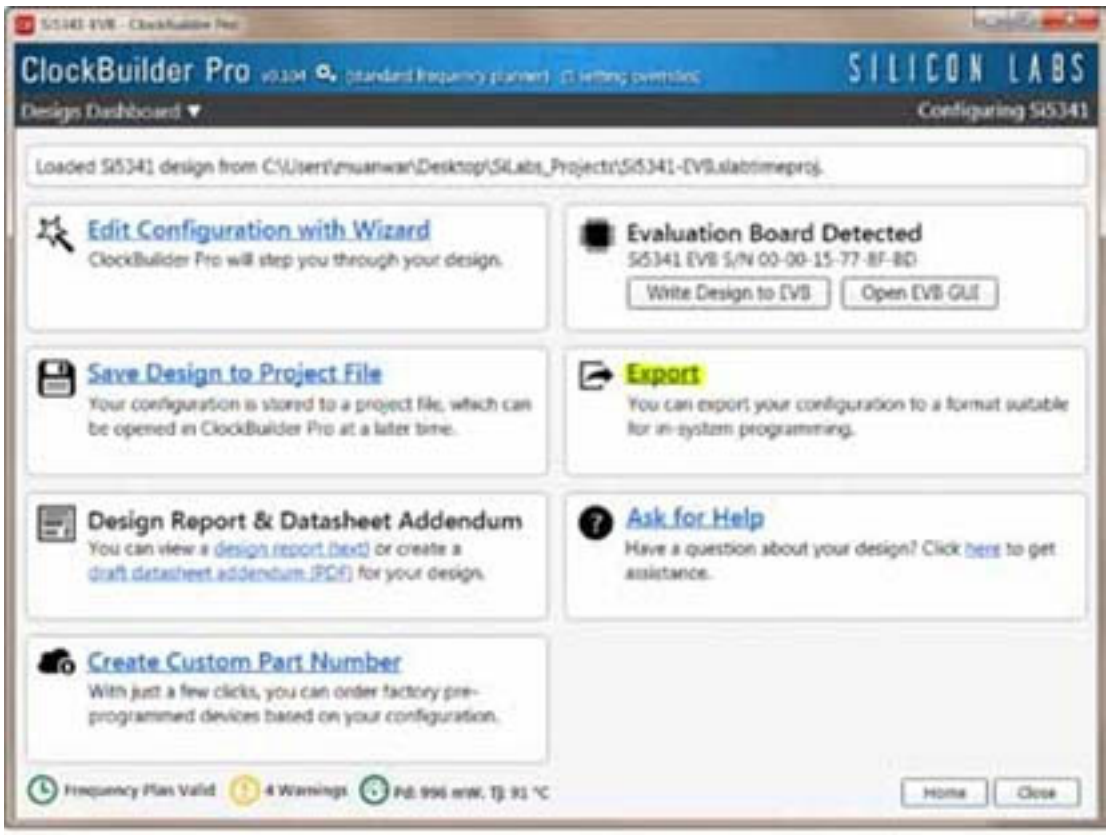


Figure 9.20. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

Figure 9.21. Export Settings

10. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5391A using ClockBuilder Pro on the Si5391A-A-EB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5391A RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

11. Si5391A-A-EVB Schematic and Bill of Materials (BOM)

The Si5391A-A-EVB Schematic and Bill of Materials (BOM) can be found online at Clock Development Tools

Note: Please be aware that the Si5391A-A-EB schematic is in **OrCad Capture***hierarchical format* and not in a typical “flat” schematic format.

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