

UG352: Si5391A-A Evaluation Board User's Guide

The Si5391A-A-EVB is used for evaluating the Si5391A Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier revision D. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5391-A-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

EVB FEATURES

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL allows free-run mode of operation on the Si5391A or up to 3 input clocks for synchronous clocking.
- Feedback clock input for optional zero delay mode.
- ClockBuilder[®] (CBPro) GUI programmable VDD supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI programmable VDDO supplies allow each of the 10 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies.
- Status LEDs for power supplies and control/status signals of Si5391A.
- SMA connectors for input and output clocks.



1. Functional Block Diagram

Below is a functional block diagram of the Si5391A-A-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See Section 3. Quick Start or Section 8. Installing ClockBuilder Pro Desktop Software for more information.

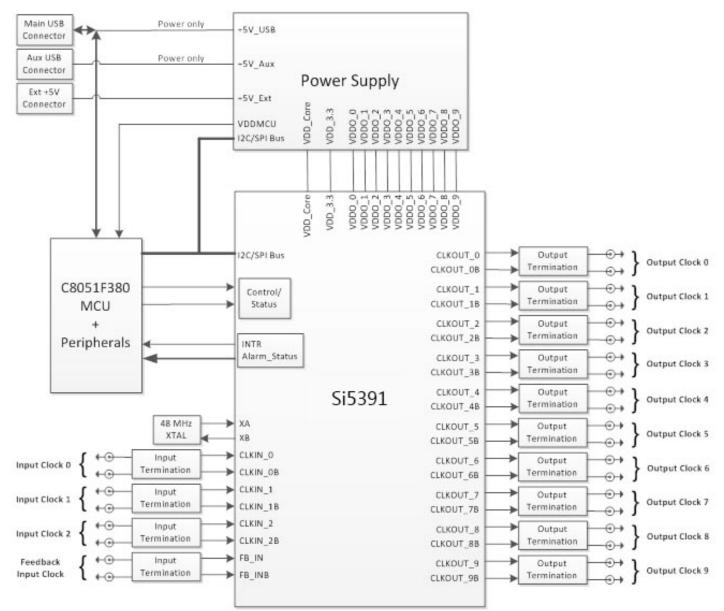


Figure 1.1. Si5391A-A EB Functional Block Diagram

UG352: Si5391A-A Evaluation Board User's Guide • Si5391A-A-EVB Support Documentation and ClockBuilder Pro Software

2. Si5391A-A-EVB Support Documentation and ClockBuilder Pro Software

All Si5391A-A-EVB schematics, BOMs, User's Guides, and software can be found online at the following link: Clock Development Tools

UG352: Si5391A-A Evaluation Board User's Guide • Quick Start

3. Quick Start

- 1. Install ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.
- 2. Connect a USB cable from Si5391A-A-EB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in Table 4.1 Si5391A-A-EB Jumper Defaults on page 5.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5391A-A-EB.
- 6. For the Si5391A data sheet, go to http://www.silabs.com/timing.

4. Jumper Defaults

Location	Туре	l = Installed 0 = Open	 Location	Туре	I = Installed 0 = Open
JP1	2 pin	0	JP23	2 pin	0
JP2	2 pin	I	JP24	2 pin	0
JP3	2 pin	0	JP25	2 pin	0
JP4	2 pin	I	JP26	2 pin	0
JP5	2 pin	I	JP27	2 pin	0
JP6	2 pin	I	JP28	2 pin	0
JP7	2 pin	I	JP29	2 pin	0
JP8	2 pin	I	JP30	2 pin	0
JP9	2 pin	0	JP31	2 pin	0
JP10	2 pin	I	JP32	2 pin	0
JP13	2 pin	0	JP33	2 pin	0
JP14	2 pin	I	JP34	2 pin	0
JP15	3 pin	1 to 2	JP35	2 pin	0
JP16	3 pin	1 to 2	J36	2 pin	0
JP17	2 pin	0	JP38	3 pin	All Open
JP18	2 pin	0	JP39	2 pin	0
JP19	2 pin	0	JP40	2 pin	0
JP20	2 pin	0	JP41	2 pin	0
JP21	2 pin	0	J36	5 x 2 Hdr	All 5 installed
JP22	2 pin	0			

Table 4.1. Si5391A-A-EB Jumper Defaults

5. Staus LEDs

Table 5.1. Si5	391A-A-EB	Status LED	S
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Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy

D27, D22, and D26 are illuminated when USB +5 V, Si5391A +3.3 V, and Si5391A VDD supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity.

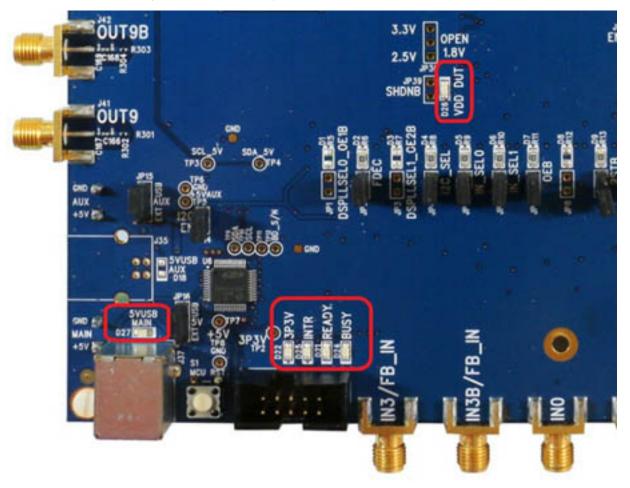
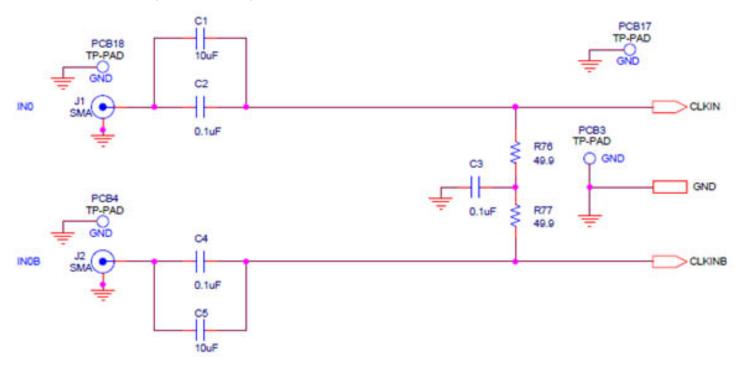


Figure 5.1. Status LEDs

UG352: Si5391A-A Evaluation Board User's Guide • Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

6. Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5391A-A-EB has eight SMA connectors (IN0/IN0B–IN2/IN3B and FB_IN/FB_INB) for receiving external clock signals. All input clocks are terminated as shown in figure below. Note input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5391 Data Sheet.





7. Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5391A-A-EVB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5391A-A-EB and provide locations on the PCB for optional dc/ac terminations by the end user.

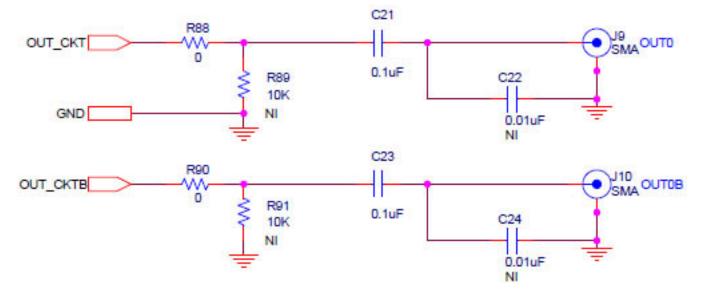


Figure 7.1. OUtput Clock Termination Circuit

UG352: Si5391A-A Evaluation Board User's Guide • Installing ClockBuilder Pro Desktop Software

8. Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any Windows 7 or Windows 10 PC, go to http://www.silabs.com/CBPro and download ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above. Follow the instructions as indicated.

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9. Using the Si5391A-A-EVB

9.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the evaluation board with a USB cable as shown below.

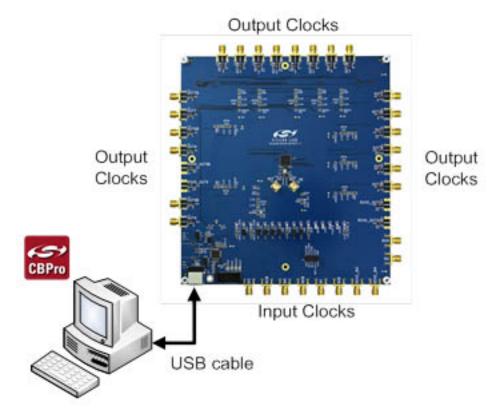


Figure 9.1. EVB Connection Diagram

9.2 Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is not needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5391A-A-EB schematic for details.

The Si5391A-A-EB comes preconfigured with jumpers installed at JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The figure below shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

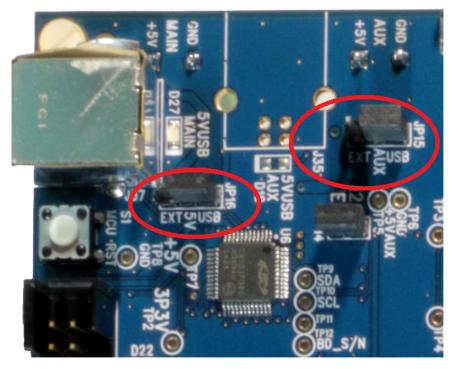


Figure 9.2. JP15-JP16 Standard Jumper Shunt Installation

Note: Some early versions of the 64-pin Si534x-EBs may have the silkscreen text at JP15-JP16 reversed regarding EXT and USB, i.e., USB EXT instead of EXT USB. Regardless, the correct installation of the jumper shunts for default or standard operation is on the right hand side as read and viewed in the figure above.

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, re-configure the EB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
 - Connect external +5 V power supply to terminal block J33 on the back side of the PCB.
 - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.

9.3 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilder Pro installer will install two main applications:



Figure 9.3. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to:

- · Review or edit an existing design
- · Export: Create in-system programming
- · Create a new design

VIDO LINV Mail V A W Read Hard Read	nd Calibrat 1,457 et. Sync. A
VDD LRIV Dis -V -A -W Rand SOF VDD LRIV Dis -V -A -W Rand Hand Rand Hand Rand Hand Rand House Report House Report	T,AST
VCD LAIV M <th></th>	
V0000 2.57V Con -V -A -W Read Prove V0001 2.57V Con -V -A -W Read HAR V0002 2.57V Con -V -A -W Read 10 V0003 2.57V Con -V -A -W Read 10 V0003 2.57V Con -V -A -W Read 10 V0004 2.57V Con -V -A -W Read Point	H. Sync. A
V0000 2.537 Co -V -A -W Read HAR V0001 2.537 Co -V -A -W Read HAR V0001 2.537 Co -V -A -W Read IN V0003 2.537 Co -V -A -W Read IN V0003 2.537 Co -V -A -W Read PDH V0004 2.537 Co -V -A -W Read PDH	
V0001 2.50V 0 V A W Read IN V0002 2.50V 0 V -A W Read IN V0003 2.50V 0 V -A W Read IN V0003 2.50V 0 V -A W Read IN V0004 2.50V 0 V -A W Read Frequence	
V0002 233V Con -V -A -W Reed PDH V0003 233V Con -V -A W Reed PDH PDH V0003 233V Con V A W Reed PDH PDH V0004 233V Con V A W Reed PDH	
V0003 233V C C - V - A - W Rest Post	NC.
V0004 2.52V 📓 💽 - V - A - W Real	6
	cy Adjust
VD005 2.50V 2 -V -A -W Asst	NC .
V0006 2577 E -V -A -W Reat	96C
V0007 250V 🖬 💽	
V0000 250V 🖬 ன -V -A -W Real	
V2009 233V 📓 🚾 V A W Ased	
All Cudput p Select Willage_ D Total -A -W Food AT	
Supplies. Power On Power Ot Compare Design Estimates to Measurements	

Figure 9.4. Application #2: EVB GUI

Use the EVB to:

Download configuration to EVB's DUT (Si5391A)

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- · Control the EVB's regulators
- · Monitor voltage, current, power on the EVB

9.4 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5391A-A-EVB. These workflow scenarios are:

- · Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- · Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration Each

Each workflow is described in more detail in the following subsections.

9.5 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.



Figure 9.5. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.



Figure 9.6. Open Default Plan

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Once you open the default plan (based on your EVB model number), a popup will appear.



Figure 9.7. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5391A device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

CB Si5341 Design Write	
Writing Si5341 Design to EVB Address 0x0119	

Figure 9.8. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.

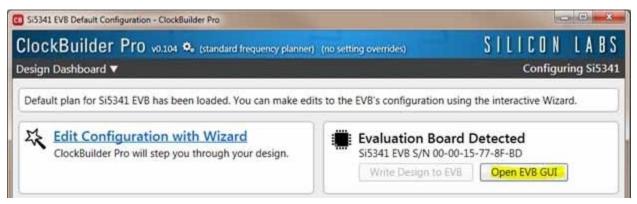


Figure 9.9. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown below.

to DUTSPI D	2C DUT Register Edito	or Regulators	All Voltages GP2	O Status Regist	ers
		Voltage	Current	Power	
VDD	1.80V 🔄 💽	1.306 V	488 mA	637 mW	Read
VDDA	(Cm)	3.294 V	112 mA	369 mW	Read
VDD00	2.50V 📔 🔼	2514 V	14 mA	35 mW	Read
VDD01	2.50V 📓 💁	2.500 V	17 mA	43 mW	Read
VDD02	2.50V 🖬 💽	2.507 V	14 mA	35 mW	Read
VDDO3	2.50V 📓 💽	2.496 V	14 mA	35 mW	Read
VDDO4	2.50V 📓 💽	2.499 V	15 mA	37 mW	Read
VDD05	2.50V 🔲 🔭	2.501 V	16 mA	40 mW	Read
VDD06	2.50V 🔄 💽	2.504 V	14 mA	35 mW	Read
VDD07	2.50V 🔛 🙆	2.485 V	14 mA	35 mW	Read
VODOS	2.50V 💽 어	2.500 V	14 mA	35 mW	Read
VD009	2.50V 🖬 💽	2.490 V	16 mA	40 mW	Read
All Output [Select Voltage	Total	748 mA	1.376 W	Read Al

Figure 9.10. EVB GUI Window

9.5.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting "Off" then "On" of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB":

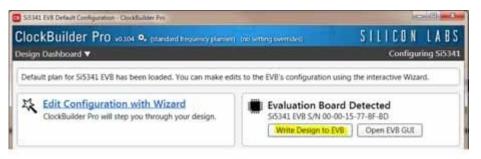


Figure 9.11. Write Design to EVB

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below

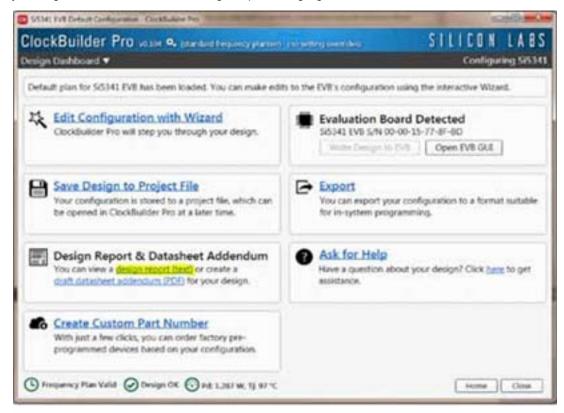


Figure 9.12. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

```
408 100
                                                                                          10
55341 Design Report
 Design Report
  5153410
               100 Hz to 330 MHz
                                                                                           *
              100 Hz to 300 2018 Integes (150 fs) only
  2133410
  2153410
              100 Hz to 350 MHz
  * Dased on your calculated frequency plan, a Si33414 grade device is
  required for your design. See the datasheet Ordering Guide for more
  information.
  Design
  Nost interface:
     L/O Power Supply: VOD (Care)
     191 Hode: 4-Hire
     IIC Address Range: 1165 to 1155 / Cult to Oxil (selected via AS/A1 pins)
  33/331
     48 HDis (KTAL - Crystal)
  Inguts
      1801 48 30ta
            Differential
      INC: 45 101#
           Differential
      TH2: 48 104a
            Differential
     COTO: 161.1328128 MMz | 161 + 17/128 MMz |
Enabled, LVIN 2.8 V
     CUT1: 025 Hite
            Enabled, LVID 2.5 V
     OUT2: 156.25 MHz ( 156 + 1/8 MHz )
Enabled, LV25 2.8 V
     OUTS: 156.25 MME [ 154 + 1/4 MME ]
            Enabled, LVTS 2.5 V
     OUT4: 168.041013425 HHz | 168 + 21/312 HHz |
            Enabled, LVIS 2.5 V
     CUTS: 472.1440425 HHz [ 672 + 21/128 HHz ]
     Enabled, LVDS 2.5 V
OUT4: 174.7030537004405264... HHz | 174 + 750/1195 HHz |
     Enabled, 1VD9 2.5 V
COT7: 155.52 NHs [ 155 + 15/25 NHz ]
            Enabled, 1918 2.5 V
     OUTE: 155.12 Mis : 155 + 12/23 Hiss |
     Enabled, LVES 3.5 V
OUT9: 622.05 HHz | 623 + 2/18 HHz |
Enabled, LVES 2.5 V
  Copy to Clipboard
                         Save Report
                                                                                     Close
```

Figure 9.13. Design Report Window

9.5.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

9.6 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on Edit Configuration with Wizard:

ClockBuilder Pro Josef & prantised trepping provent Design Databoard V	SILICON LABS Configuring Sitient
Default plan for S5343 EVE has been loaded. You can make edd	a to the EVIPs configuration using the interactive Waand.
Cockbuilder Pro will step you through your design.	Evaluation Board Detected So341 EVE 5/N 00-00-13-77-6F-8D Utiting Simple to 2VE Copen EVE GUE
Save Design to Project File Your configuration is stored to a project file, which can be opened in Occilitation Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum. You can view a <u>datasheet hodd</u> or create a draft <u>datasheet addendum (FCF)</u> for your design.	Ask for Help Have a question about your design? Clok tang to get assistance.
Create Custom Part Number With just a few clicks, you can order factory pre- programmed devices based on your configuration.	
() Energiaency Rus Vallel @ Design OK () PdL L287 W. 13 87 °C	Huma

Figure 9.14. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating conditions



Figure 9.15. Design Wizard

Note: You can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

CB Si5341 Design Write	
Writing Si5341 Design to EVB Address 0x0119	

Figure 9.16. Writing Design Status

9.7 Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

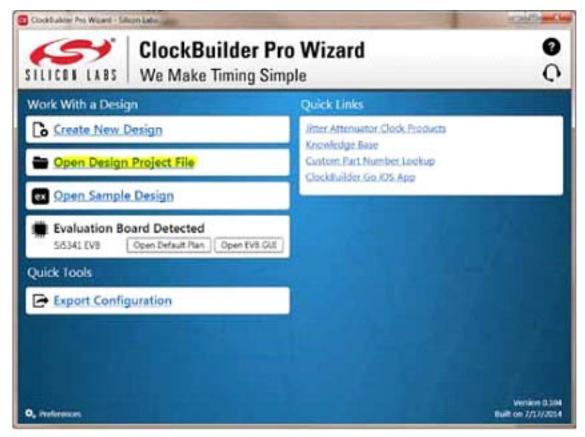


Figure 9.17. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file).design file in the Windows file browser.

Departer . New Yolds	1			11 e	. 0
2 Favorina	Name	Data modified	Tipe.	Sie	
ME Cesting	SSHE-EVE-autometers	6/36/3033 1/20 PM	Bion Lais Term.	34	6
# Downlash	103345-EV8 statemeters)	5/99-0034 L30 PM	Store Late Term.	3.8	1
35 Pasant Piaces	Sci Stat at a training agore	\$170.004 c.0194	Street Later Toreits	11	κ.
14 Librariae					
Computer Excert Dok (C) Provement (Nodeltac) Provement (Nodeltac) Provement (Nodeltac) Provement (Nodeltac)					
A Tenunt					
	ere S2H Withdows		• Short Late Tex		

Figure 9.18. Browse to Project File

Select [Yes] when the WRITE DESIGN to EVB popup appears:

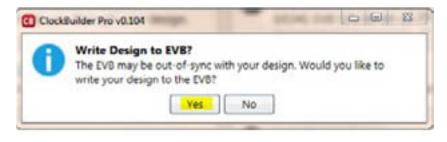


Figure 9.19. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

9.8 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:



Figure 9.20. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.



Figure 9.21. Export Settings

UG352: Si5391A-A Evaluation Board User's Guide • Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

10. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5391A using ClockBuilder Pro on the Si5391A-A-EB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5391A RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

UG352: Si5391A-A Evaluation Board User's Guide • Si5391A-A-EVB Schematic and Bill of Materials (BOM)

11. Si5391A-A-EVB Schematic and Bill of Materials (BOM)

The Si5391A-A-EVB Schematic and Bill of Materials (BOM) can be found online at Clock Development Tools

Note: Please be aware that the Si5391A-A-EB schematic is in OrCad Capturehierarchical format and not in a typical "flat" schematic format.

SKYWORKS

ClockBuilder Pro

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