UG482: Si8284v2-EVB User's Guide

This document describes the operation of the Si8284v2-EVB.

The Si8284 Evaluation Kit contains the following items:

- Si8284v2-EVB
- Si8284DD-IS installed on the evaluation board

Kit Capabilities

- Demonstrates driver functionality
- Demonstrates operating with a Capacitive Driver Load
- Demonstrates switching with a SiC FET, IGBT, or Si MOSFET (not included)

This document includes:

- Board configuration details
- Feature descriptions
- Schematics
- Layout
- Bill of materials

KEY FEATURES

- Si8284 low voltage side connections
- DC-DC Operation
- Si8284 isolated gate drive connections
- Gate Current Boost Option
- Alternative Configurations

Table of Contents

1. Overview and Setup

Si8284v2-EVB can be used to demonstrate the isolated gate drive capabilities of the installed Si8284DD-IS. The Si8284 includes a DC-DC converter used to supply isolated power to the gate driver.

The following scenarios are specifically supported:

- Demonstration of gate driver with no load, observing V_{GS} and V_{DS}
- Demonstration of gate driver with pre-installed capacitive load, observing load current
- Demonstration of gate driver with SiC / MOSFET / IGBT gate load (switch devices not included in Kit)
- Demonstration of gate driver / Switch desaturation functionality, with Fault Indication and Fault clearing by Reset
- Evaluation of gate driver / Switch performance with double pulse test and inductive load

1.1 Hardware

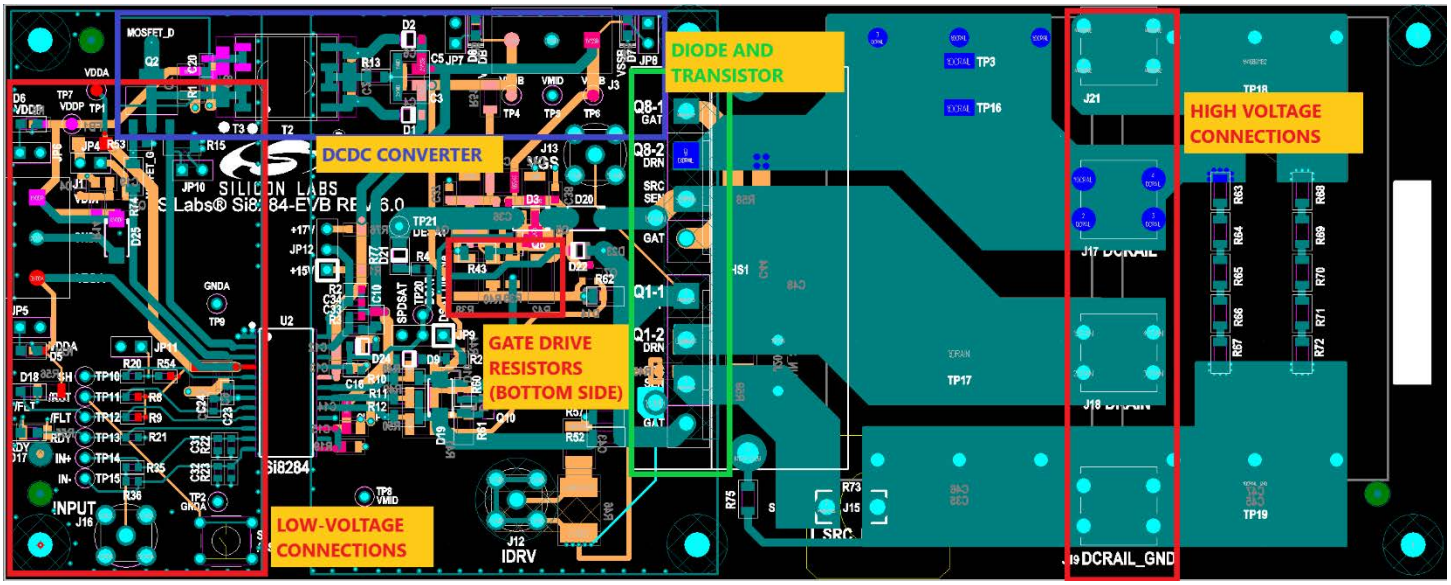


Figure 1.1. Si8284v2-EVB Functional Areas

1.1.1 Si8284 Low Voltage Side Connections

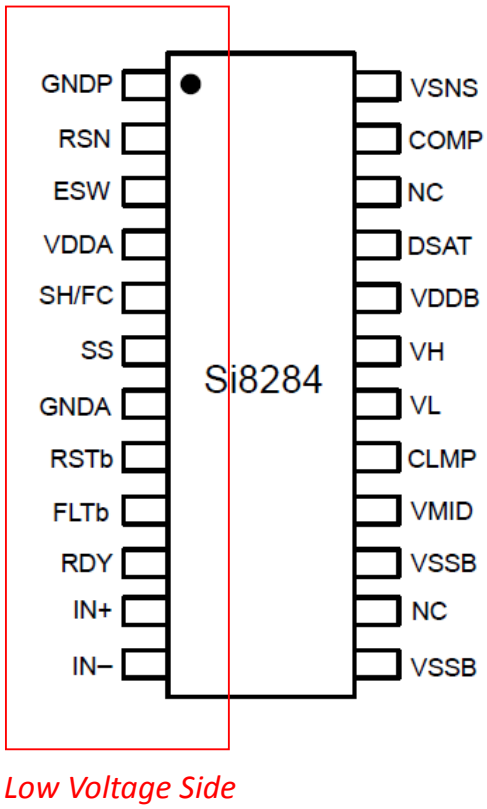


Figure 1.2. Low Voltage Side

Supply power to the input side of Si8284 by applying +9 to +24 VDC (at least 0.5 A) to VDDP at terminal block J1 pin 1 and applying its return at pin 2, labeled GNDA. Green LED D6 above terminal block J1 illuminates to show power applied. The jumper at header JP6 (installed by default) may be removed to disable LED D6. For interfacing to the low voltage side of Si8284, VDDA supply must be between 3.0 and 5.5 VDC. Either a separate supply can be connected to VDDA terminal on J1 pin 3 (with return on pin 2, JP4 must be removed) or 5 VDC can be derived from VDDP through the on-board regulator circuit and directed to VDDA through a jumper at header JP4 (installed by default). Green LED D5 below terminal block J1 illuminates to show VDDA power is applied. The jumper at header JP5 (installed by default) may be removed to disable LED D5.

SMA connector J16 (found on the back side of the board) provides access to the IN+ input through a 50 Ω resistor. The reference pin of J16 and the IN- input of the Si8284 are grounded to the low-voltage reference GNDA. The pins IN+ and IN- may also be monitored at test points TP14 and TP15, respectively. Driver functionality can be exercised without a controller by applying a GNDA-referenced PWM signal from a function generator to J16. Maximum allowable input voltage is VDDA.

The RSTb pin (shown as /RST in the schematic) is controlled by momentary switch S1. The pin may be monitored or externally controlled at test point TP11. RSTb is passively pulled up by a 10 kΩ resistor, R8.

The active high SH input pin is normally held low by a jumper installed at header JP11 (installed by default) which also serves as a sink for the frequency control (FC) current, but the DC-DC converter may be disabled by removing the jumper and allowing the input to be pulled high by 1k resistor, R54. The pin may be monitored at test point TP10.

The Ready pin indicates to the controller that power is available on both sides of the isolation, i.e., at VDDA and VDDB. RDY goes high when both the primary side and secondary side UVLO circuits are disengaged. If either VDDA or VDDB drops below its UVLO threshold, the ready pin will return low. RDY is a push-pull output pin and can be floated if not used. An active RDY is visually indicated by illumination of the green LED D17.

FLTb (/FLT in the schematic) is an open-drain type output. A pull-up resistor R9 takes the pin high. When the desaturation condition is detected, the Si828x indicates the fault by bringing the FLTb pin low. FLTb stays low until the controller or the user brings the RSTb pin low.

An active FLTb is visually indicated by illumination of the red LED D18.

The FLTb and RDY outputs of the Si8284 may be monitored at test points TP12 and TP13, respectively. The open drain FLTb output allows multiple gate drivers' FLTb outputs to share the same microcontroller input. The RDY output has a pull-down resistor to GNDA.

1.1.2 DC-DC Operation

The isolated DC-DC converter is configured to generate (with respect to VMID) +15 V for VDDB and -3.5 V for VSSB. Green LEDs D8 and D7 illuminate when VDDB and VSSB are powered respectively. LED D8 may be disabled by removing the jumper at header JP7 (installed by default), and LED D7 may be disabled by removing the jumper at header JP8 (installed by default). DC-DC operation can be disabled by removing the jumper at header JP11 (installed by default).

1.1.3 Si8284 Isolated Gate Drive Connections

There is a provision for a 3- or 4-pin SiCFET, a MOSFET, or an IGBT in a TO-247 package (not supplied) at Q1. The same part number should be used at Q8, which is connected in the off mode as a rectifying diode between Q1 drain and the DCRAIL connector.

From top to bottom in the layout, the through holes for the transistor leads are Gate, Drain/SiC Drain, Source/SiC Source, SiC Source Kelvin Sense, and SiC Gate. The top three holes accommodate a 3-pin (including SIC) device in TO-247 (G, D, S). Alternately, the bottom four holes accommodate a 4-pin SiC device in TO-247 (D, S, SK, G). The fourth hole (SK) is offset to accommodate the hole size.

The switching FET (load) transistor is biased by applying voltage across DCRAIL (J17) and DCRAIL_GND (J19). This voltage should not exceed the rated VDS of the transistor or 1000 V (the output capacitor voltage rating), whichever is lower. Supply voltage constraints are summarized in the table below.

Note: Si8284 can drive the gate of either high-side or low-side MOSFET or IGBT in a bridge configuration. VMID is the same net as the load when driving the gate of a high side MOSFET or IGBT. For a gate drive for a low side MOSFET or IGBT, VMID is the return for the load.

Table 1.1. Supply Voltage Constraints

3.0 V ≤VDDA – GNDA ≤ 5.5 V
9 V ≤ VDDP ≤24 V
VSSB ≤VMID < VDDB
UVLO +[1] < VDDB -VSSB < 30 V
DCRAIL < MOSFET VDS rating or 1kV, whichever is lower
|GNDA – VSSB| < 5 kV
Note: 1. UVLO+ for the Si8284DD-IS is 13 V

1.2 Configurations

1.2.1 Gate Current Boost

The Si8284v2-EVB is pre-configured to drive switch devices using an installed gate current boost circuit following the Si8284. This requires population of R48 – R51 and R62, populated by default. The gate resistors (R38, R42) are 3 ohms installed. These may be reduced to 0 ohms to get maximum gate drive current from the current boost circuit.

Option – Direct Drive from Si8284: To revert to direct, non-boosted gate drive from the Si8284, depopulate R48 – R51 and R62, and populate R10 – R12 and R52 (seen on Si8284 HV and SiC circuit page).

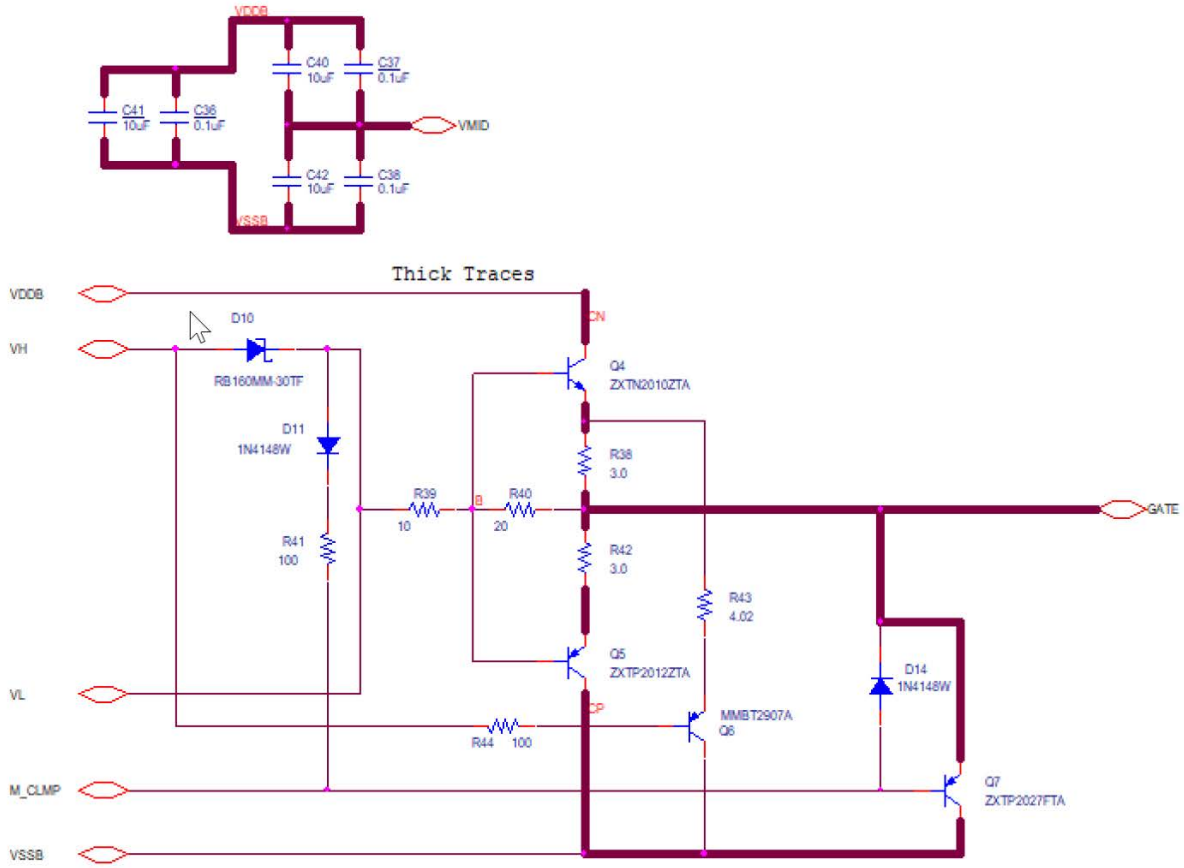


Figure 1.3. Current Boost Circuit

1.2.2 Positive Voltage Gate Drive Only

The standard configuration has the gate driver apply positive voltage, VDDB-VMID, to the gate during the high drive portion of the PWM cycle and negative voltage, VMID-VSSB, during the low drive portion of the PWM cycle. Alternatively, if only positive drive voltage is needed, remove R13 and install a 0 Ω size 0805 resistor at R19 (R13 and R19 are found in Figure 4.1 Si8284v2-EVB Low-Voltage Circuit Schematic on page 21). This will short VSSB to VMID.

1.2.3 Alternate VDDB Voltage

The EVB comes with a jumper populated to JP12, pins 1 and 2. This causes VDDB to be +15 V and VSSB to be -3.5 V. To have VDDB equal to +17 V and VSSB equal to -5 V, set the jumper at JP12 to pins 2 and 3.

2. Demonstrating Driver Functionality

Even with no load (neither capacitor nor SiC-FET switching transistor) present, the basic functionality of the Si8284 can be demonstrated. To run this demonstration, disable the on-board capacitive load (C43, 220 nF) by removing resistor 57. Save the resistor for later use.

1. Apply 9V- 24 V to VDDP at J1, pin 1 (return at pin 2) to power both sides of the Si8284. With jumpers installed at headers JP5–JP8, D5–D8 will illuminate indicating supplies are biased.
2. Apply a jumper at JP4. This allows VDDP to be regulated down to produce VDDA.
3. Leave DCRAIL unpowered. Install a jumper at JP9 pins 2 and 3. This jumper disables desaturation detection and allows for operation of the Si8284. Since both sides of the Si8284 have been powered on, RDY will output 5 V, which can be observed at green LED D17 or TP13.
4. Apply a 5 V dc signal to SMA J16 or TP14. Output VH will go High, output VL will go Hi-Z, and +15 V can be observed at SMA J13, or V_{GS}.
5. Apply a 0 V dc signal to SMA J16 or TP14. Output VH will go Hi-Z, output VL will go Low, and -3.5 V can be observed at SMA J13, or V_{GS}.
6. Gate drive voltage signal may be observed at V_{GS} (J13), an SMA-type coaxial connector.
7. A PWM signal may be applied at J16 and observed at J13 as the gate drive signal.

2.1 Driving a Capacitive Load

If the driver is exercised dynamically (with a PWM waveform at J16) with R57 installed to use C43 as a FET driver load, its drive current may be observed at IDRV (J12), an SMA-type coaxial connector. The load current develops a voltage across R46, a 0.05 Ω, 2 W resistor. R57 should be removed if the circuit is to be operated with a MOSFET installed at Q1. Note that a jumper is installed at JP9 pins 2 and 3 to disable DESAT and enable this test.

1. Populate R57 (populated by default).
2. Set up the low voltage side as described in 1.1 Hardware.
3. Apply a pulse signal to the input SMA connector J16, with value between 0 V and VDDA. A 20 us pulse width and 60 us pulse period is a useful starting point.
4. Observe the voltage output signal at J13, VGS. Display this signal on an oscilloscope. The signal will range from -3.5 V to +15 V.
5. Attach a coaxial cable to the SMA connector J12, IDRV. Display this signal on an oscilloscope. The signal is developed across a 0.05 Ω resistor, so the current can be seen at 10 A/div if the channel voltage setting is 500 mV/div

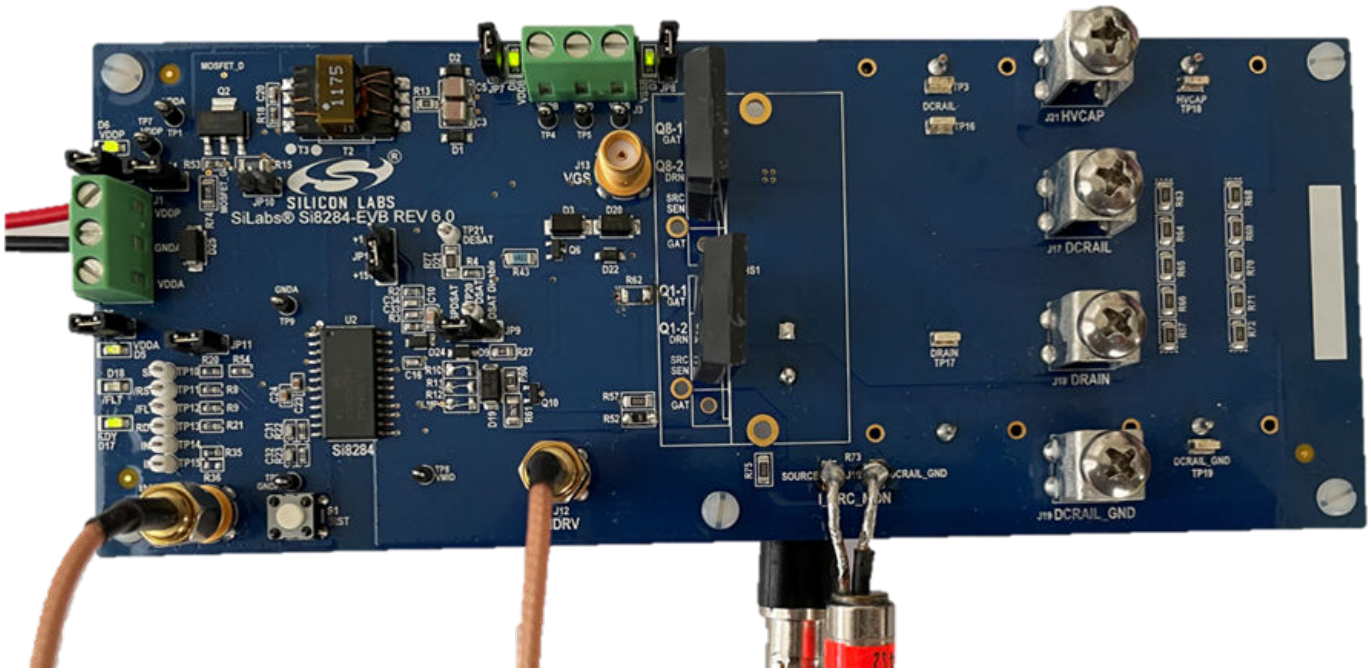


Figure 2.1. Si8284v2-EVB Connection for Driver and Capacitive Load Testing

This test can be run either with or without the current boost circuit. The board comes configured with the current boost circuit connected. If R38 and R42 (gate resistors) are both 0 Ω, then the following response can be obtained, where the yellow trace is the gate waveform and the magenta trace is the gate current.

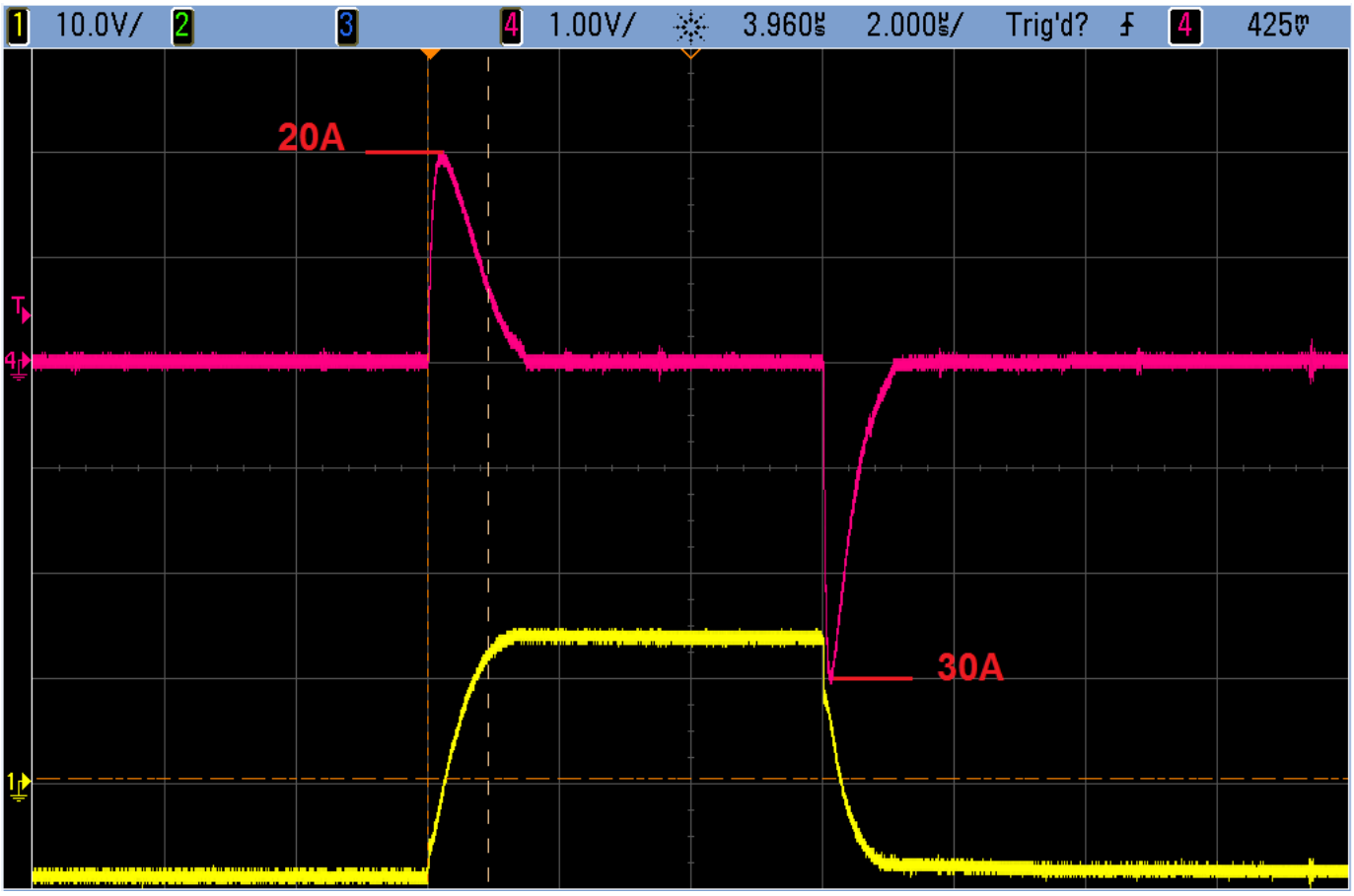


Figure 2.2. Gate Boost Circuit Response

To drive from the Si8284 directly, depopulate R48 – R51 and R62, and populate R10 – R12 and R52 (with 0 Ω, as seen in Figure 4.2 Si8284 High-Voltage Circuit Schematic on page 22). The response will look like the following:

Figure 2.3. Standard Gate Drive Response

2.2 Operating with a Switching MOSFET Installed

DANGER! This board may contain high voltages. Do not touch the board once the high voltage section has been energized.

2.2.1 Installing a Switching MOSFET

1. Ensure that R57 has been depopulated.
2. Install Q1.
3. For a 3-terminal Q1, populate R45. For a 4-terminal Q1, don't populate R45.
4. Although not required for single- or double-pulse testing, you may install a heat sink if desired at HS1 by soldering to the board. Between the MOSFET and the heat sink, use BERGQUIST SIL-PAD 900S Thermal Material Electrical Insulator. The heat sink is at DCRAIL_GND, while the drain may reach high hazardous voltages.
5. Apply CLA-TO-21E heat sink clip to ensure good thermal contact between the MOSFET and the heat sink.

2.2.2 Testing the MOSFET Response with a Capacitive Load (Short-Circuit test)

DANGER! This board may contain high voltages. Do not touch the board once the high voltage section has been energized.

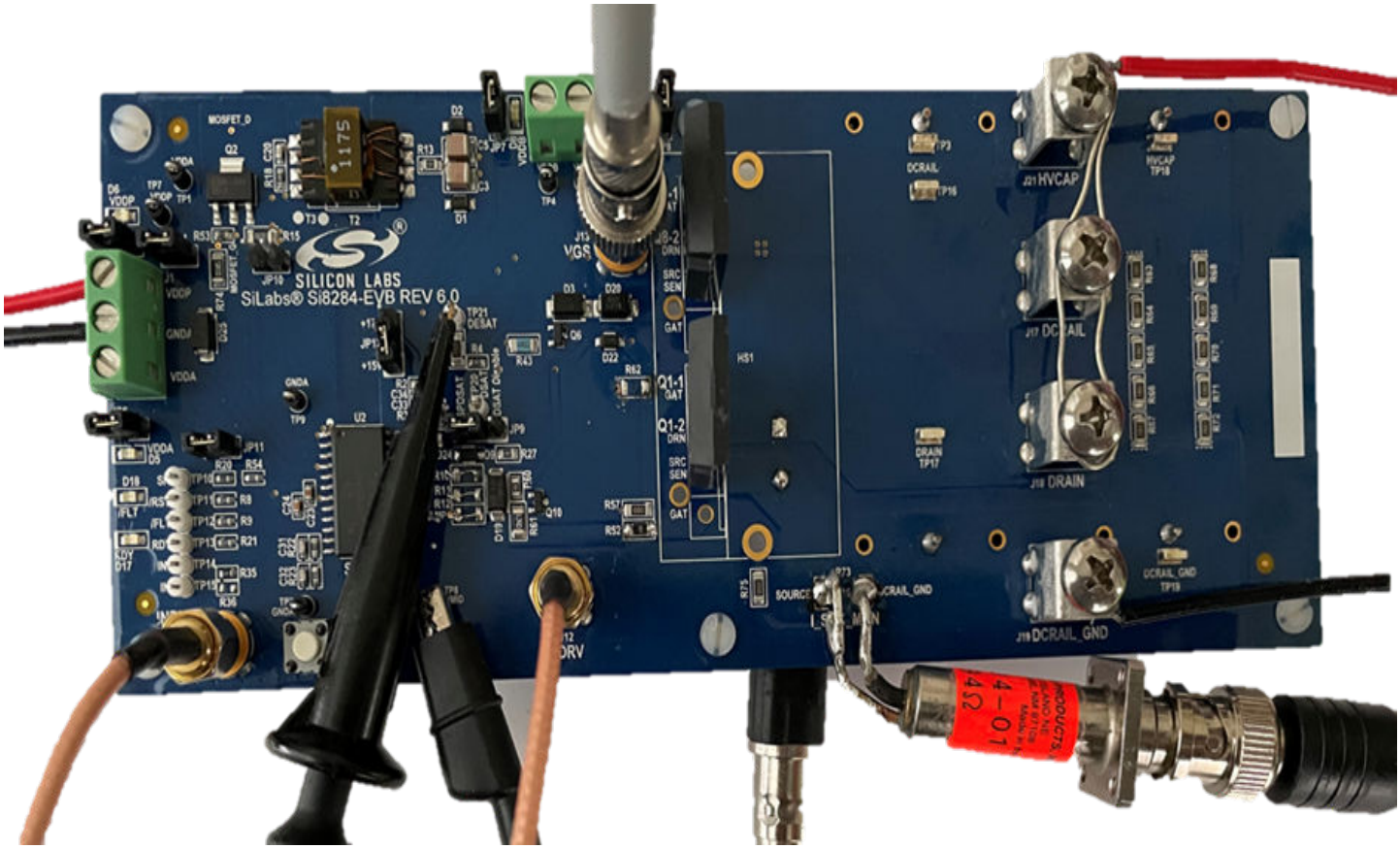


Figure 2.4. Si8284v2-EVB in SiC Shorted Load Test (Using Current Clamp Probe) with Two Load Capacitors Connected

1. Install shorting wire between terminal blocks J17 (DCRAIL), J18 (DRAIN), and J21 (HVCAP).
2. Remove jumper from JP9 to enable DESAT detection. Detection may be sped up by placing a jumper at JP9, pins 1 and 2.
3. R73 is a 5 mΩ resistor for monitoring source current. The resistor is in parallel with J15. If desired, remove resistor R73 to allow current viewing port to be installed. Install a T&M Research Products SDN Series 2-Watt current viewing port or wire loop and current clamp probe at J15.
4. Set up the low voltage side as described in 1.1 Hardware, but don't energize the low-voltage supplies.
5. Preset a DRAIN source to the desired voltage (less than the lower of 1kVrms or the FET rating), then de-energize it.
6. Attach the DRAIN voltage source to terminal block J18, with its ground lead attached to terminal block J19 (DCRAIL_GND)
7. **Perform the following step before energizing the board**. Drain voltage signal may be observed by attaching a high-voltage differential probe to the BNC connector J20, then connecting to an oscilloscope input.
8. Connect the current viewing port to an oscilloscope input.
9. Connect a scope probe as shown in figure 2.5 to observe VDS.
10. Connect a scope probe as shown in figure 2.6 to observe VGS.
11. Energize the low-voltage side of the board.
12. Prepare to apply a single 5V input pulse at J9 – J10 (IN+ - IN-). Note J10 is at GNDA.

13. Energize the trigger source but do not trigger the input pulse.
14. Energize the DRAIN source to charge the output capacitor.
15. Set a DRAIN source current limit at 100A maximum.
16. Trigger the input pulse and observe the drain and source current waveforms. Additional probes to the DSAT pin and Gate node will provide helpful images. **Place any such probes BEFORE energizing the board.**

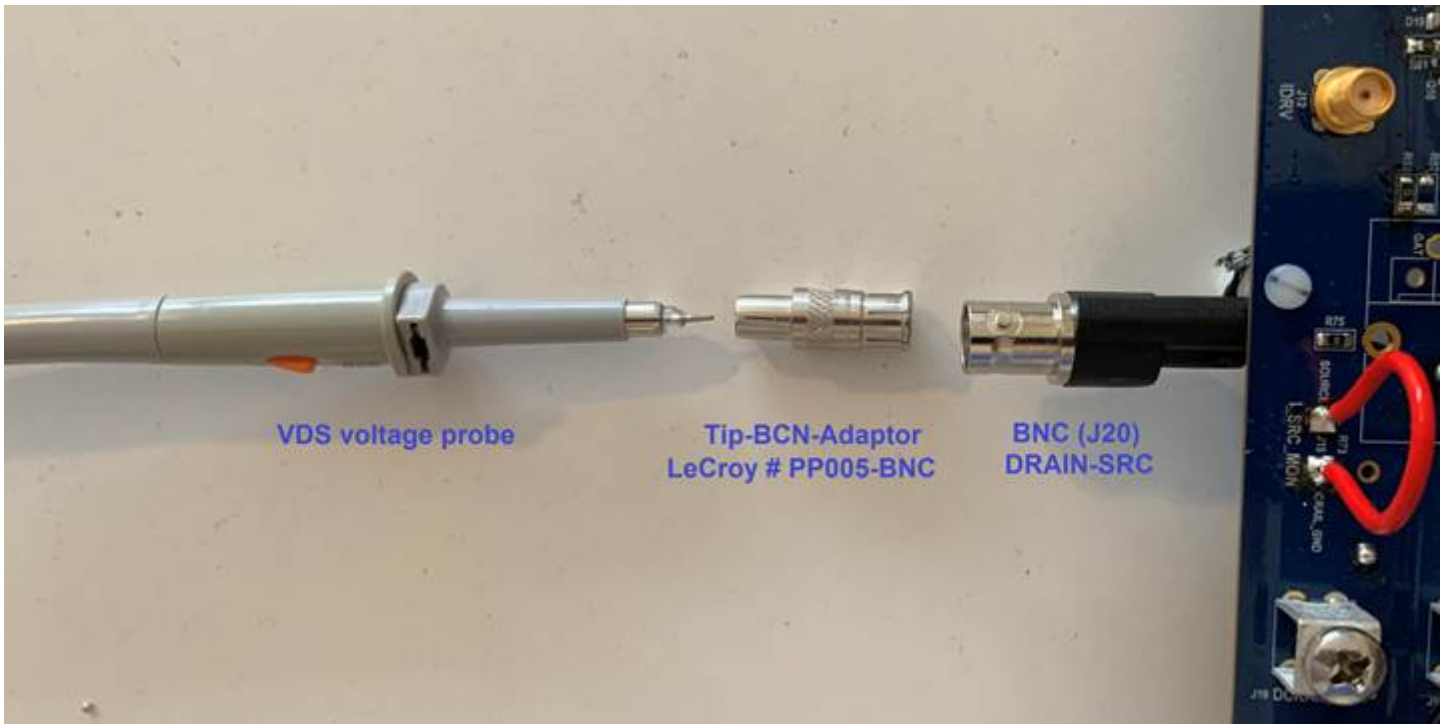


Figure 2.5. Making the VDS Scope Probe Connection

Figure 2.6. Connection for VGS Scope Probe at J13

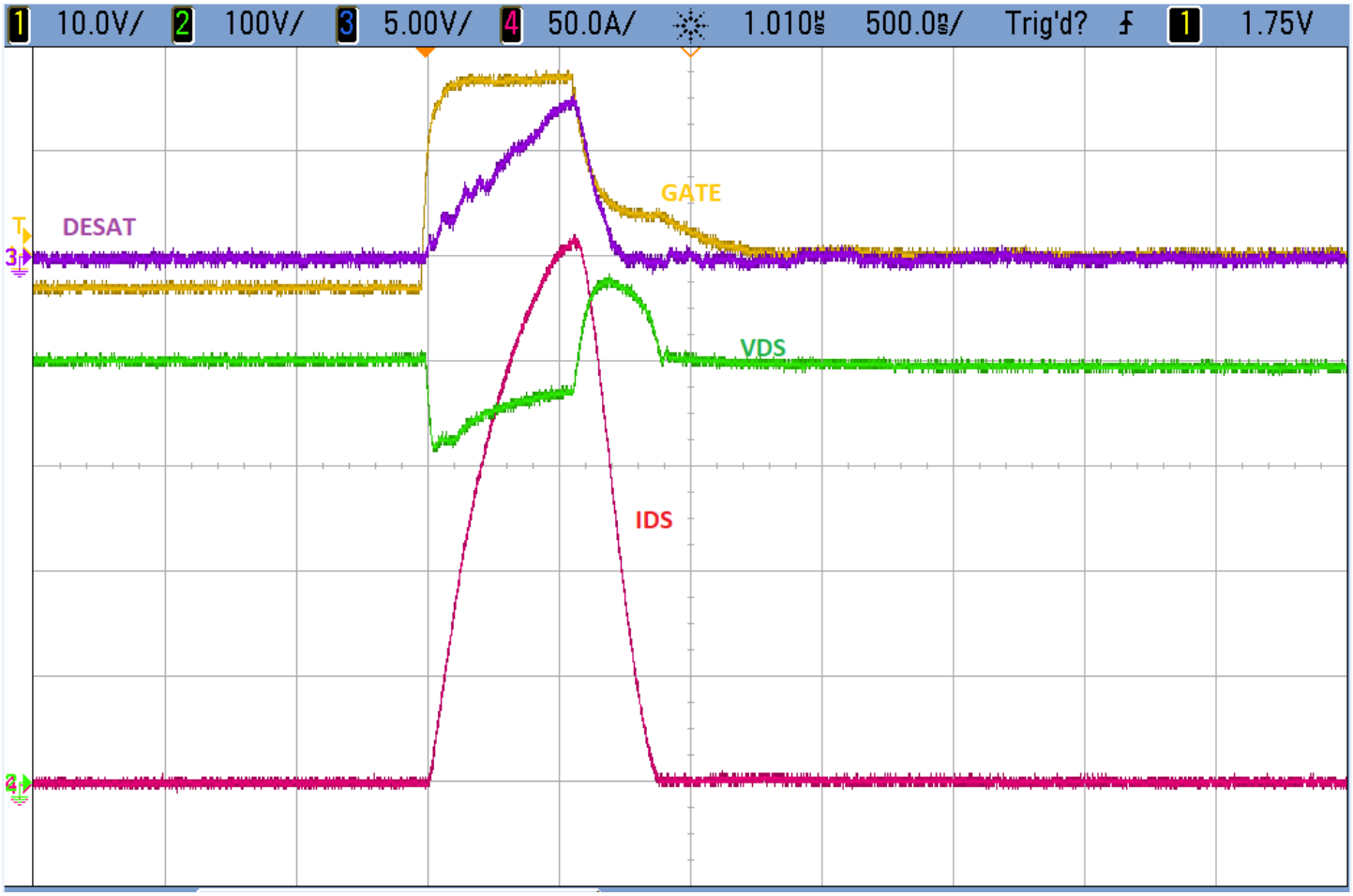


Figure 2.7. Waveforms for SiC Shorted Load Test (Current Clamp)

The Yellow Gate waveform shows fast turn on and slow turn off for soft shut down. The Purple DESAT waveform shows DESAT triggered at ~ 7.5 V. The Green VDS waveform shows some positive voltage spike after the SiC turned off. The Red source current waveform shows that the DESAT response time in less than 1uS (850nS from the time the current started at 0 A to the time the current goes back to 0 A).

2.2.3 Testing the MOSFET Response with an Inductive Load (Double-Pulse Test)

DANGER! This board may contain high voltages. Do not touch the board once the high voltage section has been energized.

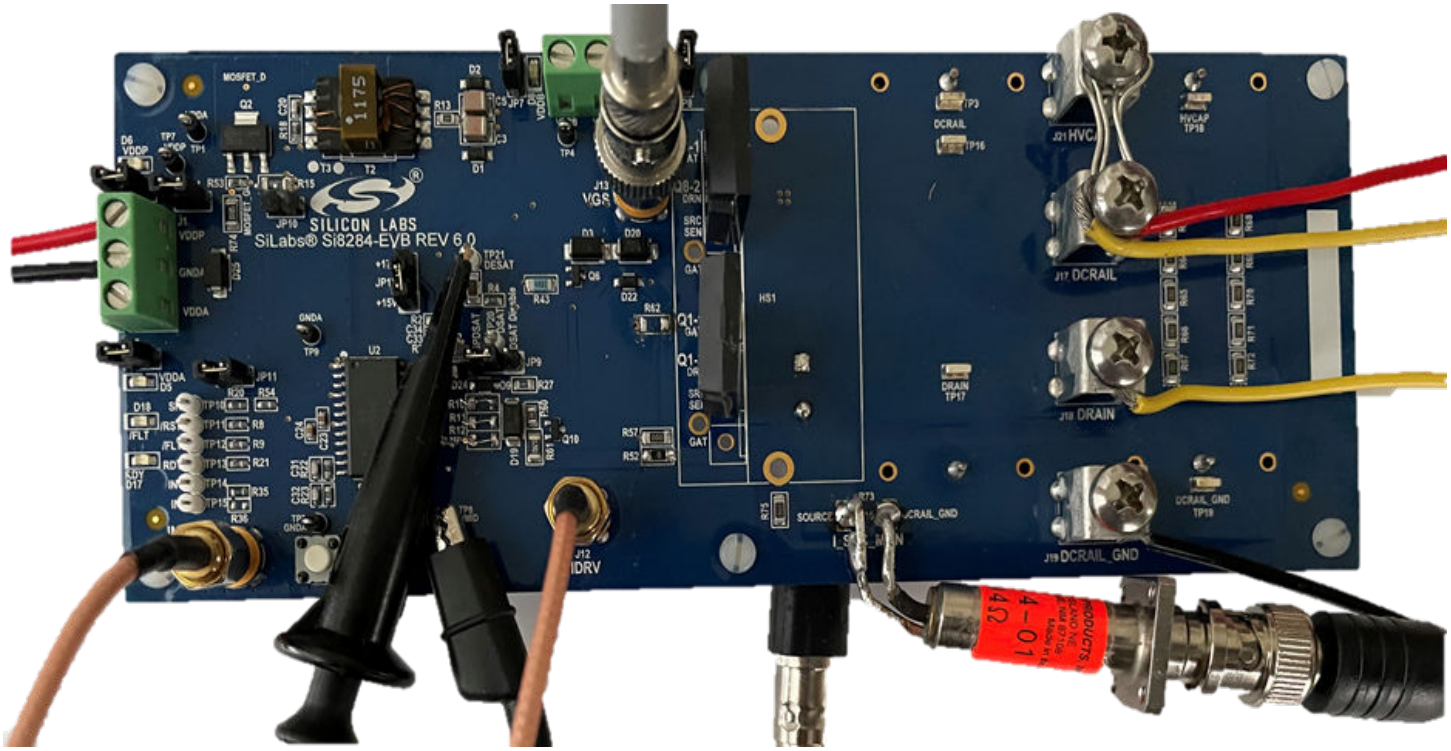
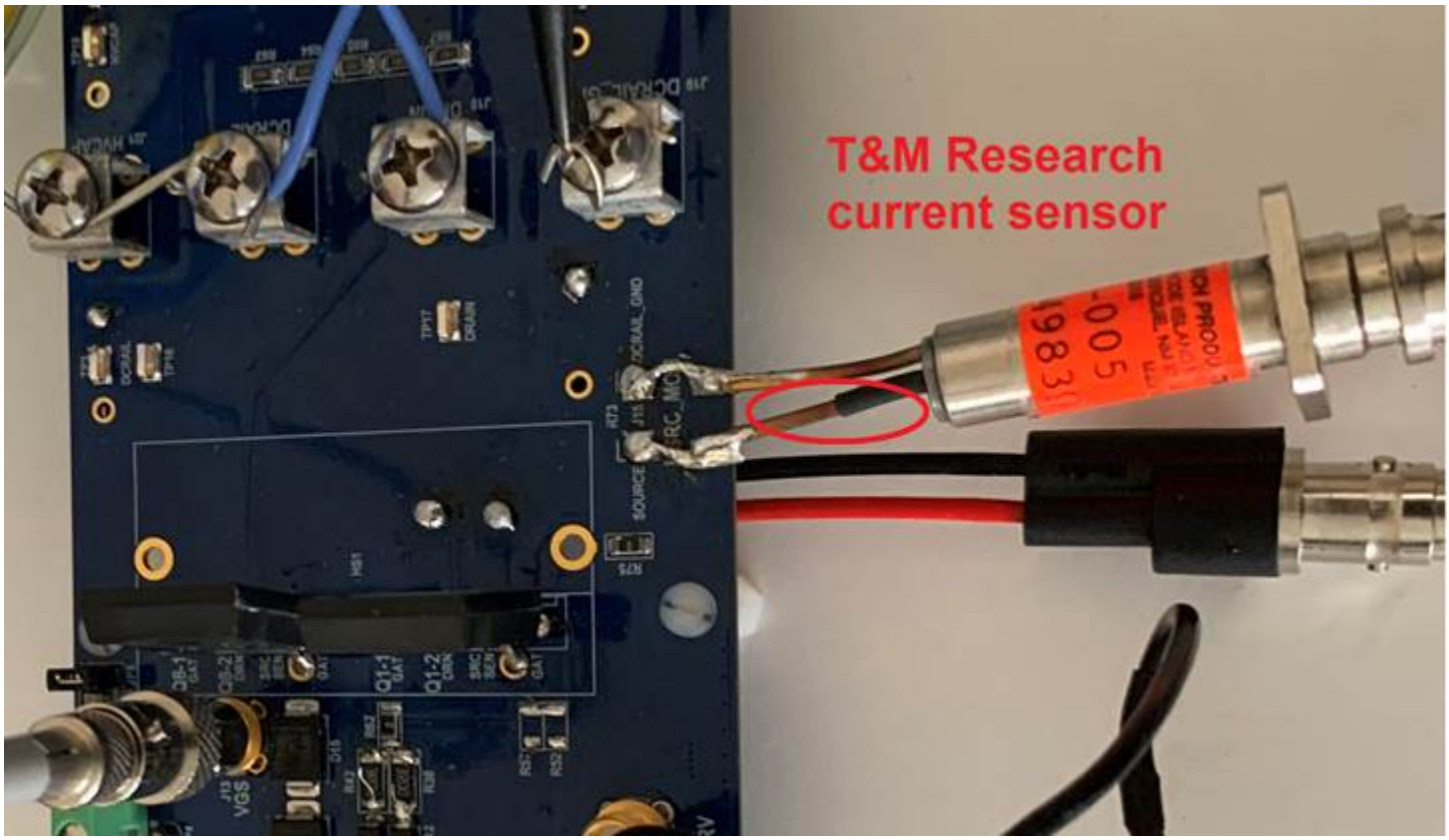


Figure 2.8. Si8284v2-EVB Connection for Double Pulse Test

1. The double pulse test will require installation of Q8, a device identical to Q1, to provide an inductor discharge path when the gate drive is low. Q8 is set up as an off device, and its body diode conducts reverse current from the inductor when gate drive is off.
2. Remove jumper from JP9 to enable DESAT detection. Detection may be sped up by placing a jumper at JP9, pins 1 and 2.
3. R73 is a 5 mΩ resistor for monitoring source current. The resistor is in parallel with J15. If desired, remove resistor R73 to allow the current viewing port to be installed. Install a T&M Research Products SDN Series 2 Watt current viewing port at J15 if this has not already been done. T&M current sensor should be installed with the center leg connected to J15-SOURCE so that all scope probes reference to the same GND. To view the current waveform from the reversed T&M current sensor connection, the scope input should be set in reversed polarity so that the current signal appears in its proper polarity (see figure Figure 2.10 Typical Signal Traces During Double Pulse Test on page 16). As shown in Figure 2.8 Si8284v2-EVB Connection for Double Pulse Test on page 14, a current monitoring loop may be installed in lieu of the current viewing port, and a current probe clamp may be used to view the source node current.
4. Set up the low voltage side as described in 1.1 Hardware, but don't energize the low-voltage supplies.
5. Install an inductor between terminal blocks J17 (DCRAIL) and J18 (DRAIN). An air core inductor of 50uH value and 150A rating is suggested. This can tolerate the DCRAIL voltage for 10 uS.
6. Preset a DCRAIL source to a value less than the lower of 1kVrms and the FET rating, and de-energize.
7. Attach the DCRAIL source to terminal block J17 (DCRAIL) with its return at J19 (DCRAIL_GND).
8. Prepare to apply a 5 V double pulse at J9 – J10 (IN+ - IN-).
9. **Perform this step before energizing the board.** Drain voltage signal may be observed by attaching a coaxial cable to the BNC connector J20, then connecting the other end of the coaxial cable to an oscilloscope input. Use a high-voltage differential probe for this measurement.

10. Energize the DCRAIL source.
11. Trigger the input pulse and observe the drain and source current waveforms.
12. Observe VGS at J13.
13. Observe source current at the current viewing port.

Figure 2.9. Detail of Current Sensor Connection



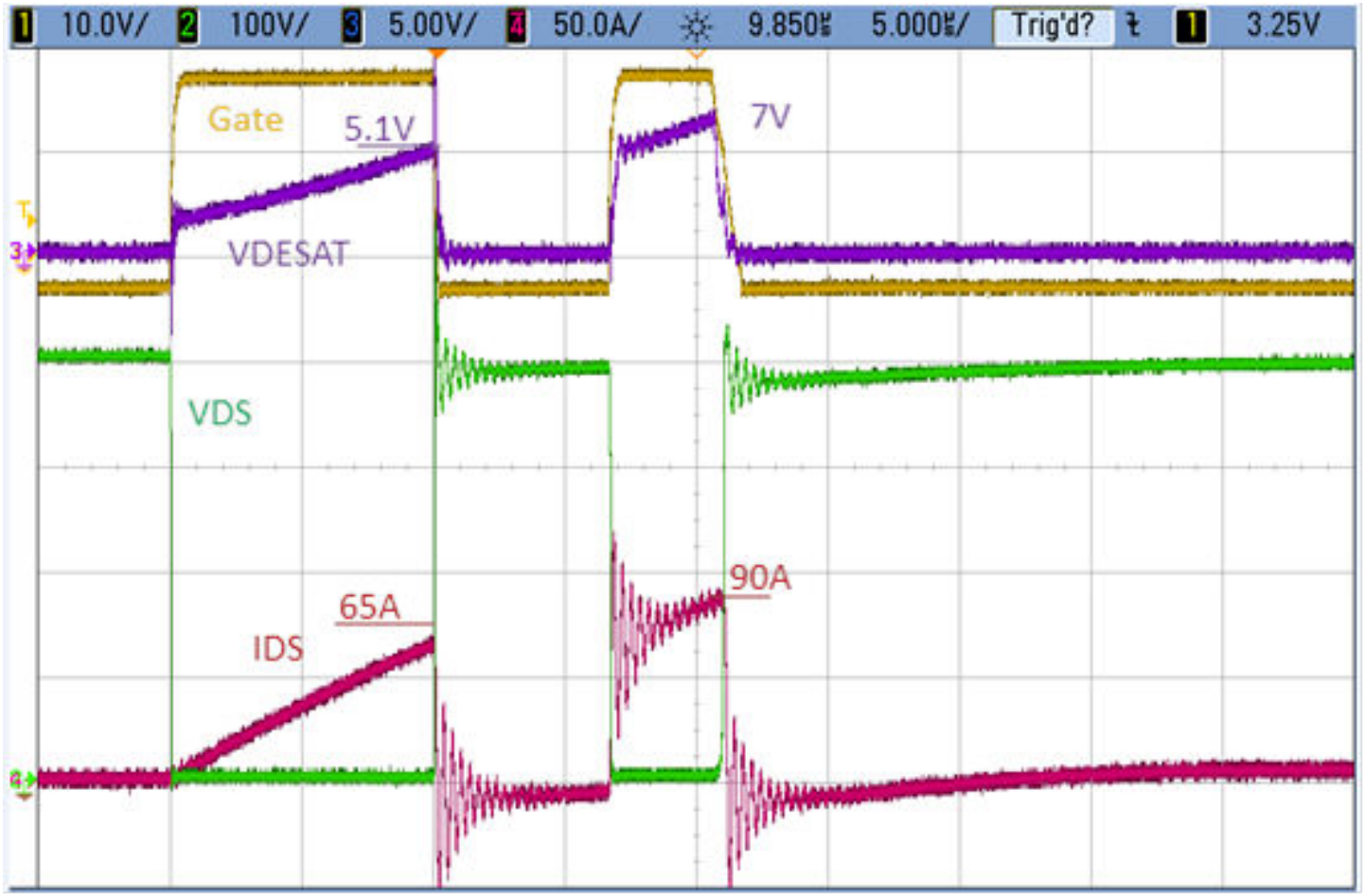


Figure 2.10. Typical Signal Traces During Double Pulse Test

2.2.4 Tuning Gate Resistor Values

Referring to Figure 4.5 Boost Circuit Schematic on page 23, there are two gate resistors, R38 and R42. R38 limits turn-on gate drive current, while R42 limits turn-off gate drive current. These resistors will typically require tuning to get optimal gate drive and emissions. The EVB comes with a nominal value of 3 Ω installed for each.

3. Features

See AN1288: Si828x External Enhancement Circuits for additional information.

3.1 DESAT Speed up/Disable

The DESAT function blanking time may be reduced, whether or not you are using the driver BOM enhancements for SiC devices. Placing a jumper at header JP9 pins 1 and 2 will add current from the VH pin to the CBL charging current when the DESAT blanking function is active, causing the CBL C16 to be charged more rapidly and the output to be pulled low sooner than otherwise. Placing the jumper at header JP9 pins 2 and 3 will disable the DESAT function.

3.2 DESAT Threshold

The DESAT threshold may be altered by removing R77 and replacing it with Zener diode D21. The Zener value will be subtracted from the nominal DESAT threshold of 7.0 V. Another approach is to change the value of R4 according to the description in AN1288: Si828x External Enhancement Circuits.

3.3 Soft Shutdown Duration

Soft shutdown duration may be modified by changing the value of R43 according to the description in AN1288: Si828x External Enhancement Circuits. Decreasing the value will reduce the duration.

3.4 Source Current Viewing Port

There is a 5 mOhm resistor (R73) in parallel with a BNC connector (J15) for easy monitoring of source current. The resistor is in parallel with J15. There is also a provision for a current view port at J15. This is for the insertion of a device such as T&M Research Products SDN Series 2-Watt Unit, or a wire loop for use with a current clamp probe. If this will not be used, install the resistor R73. If using the T&M Research current sensor, the sensor should be connected with the center pin connected to J15-SOURCE. The scope polarity should be set to inverted polarity with 50 Ohms input impedance. Adjust the scope's current setting to match the T&M sensor V/A rating.

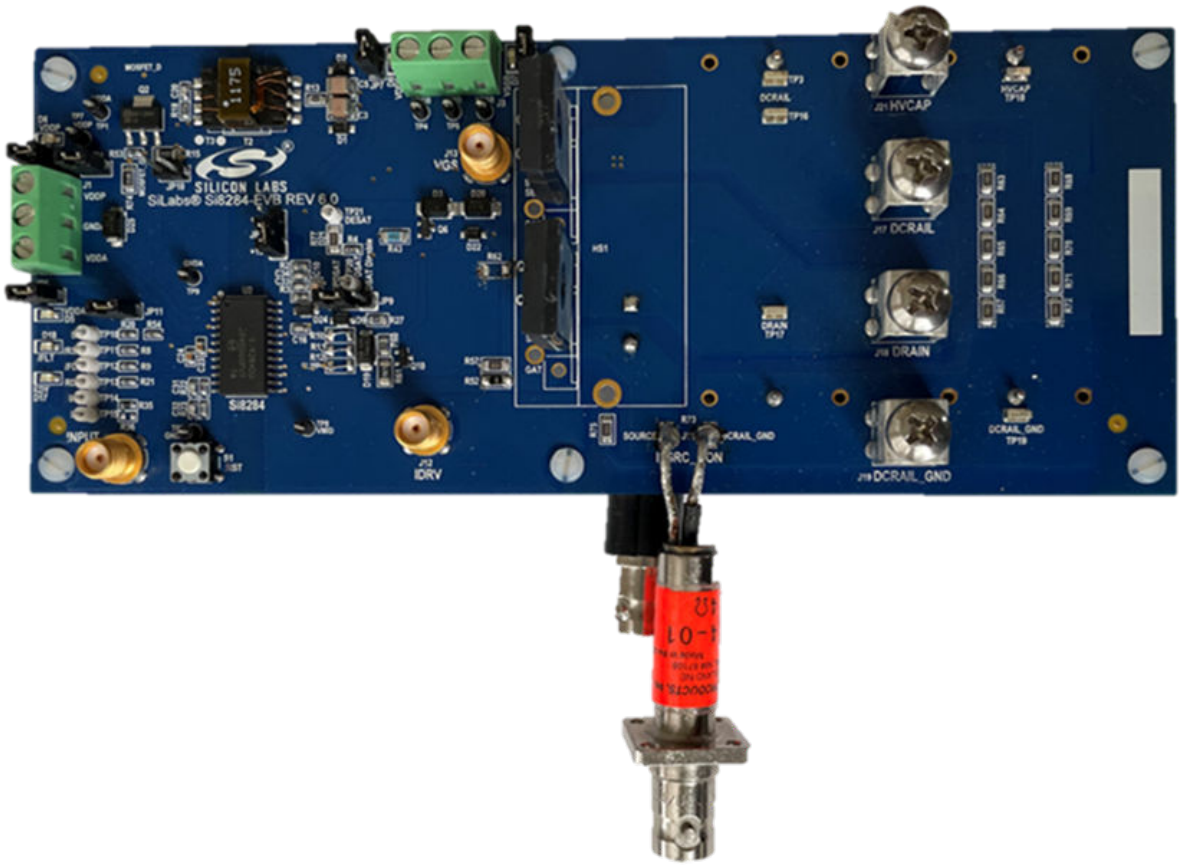


Figure 3.1. Si8284v2-EVB with T&M Current Sensor

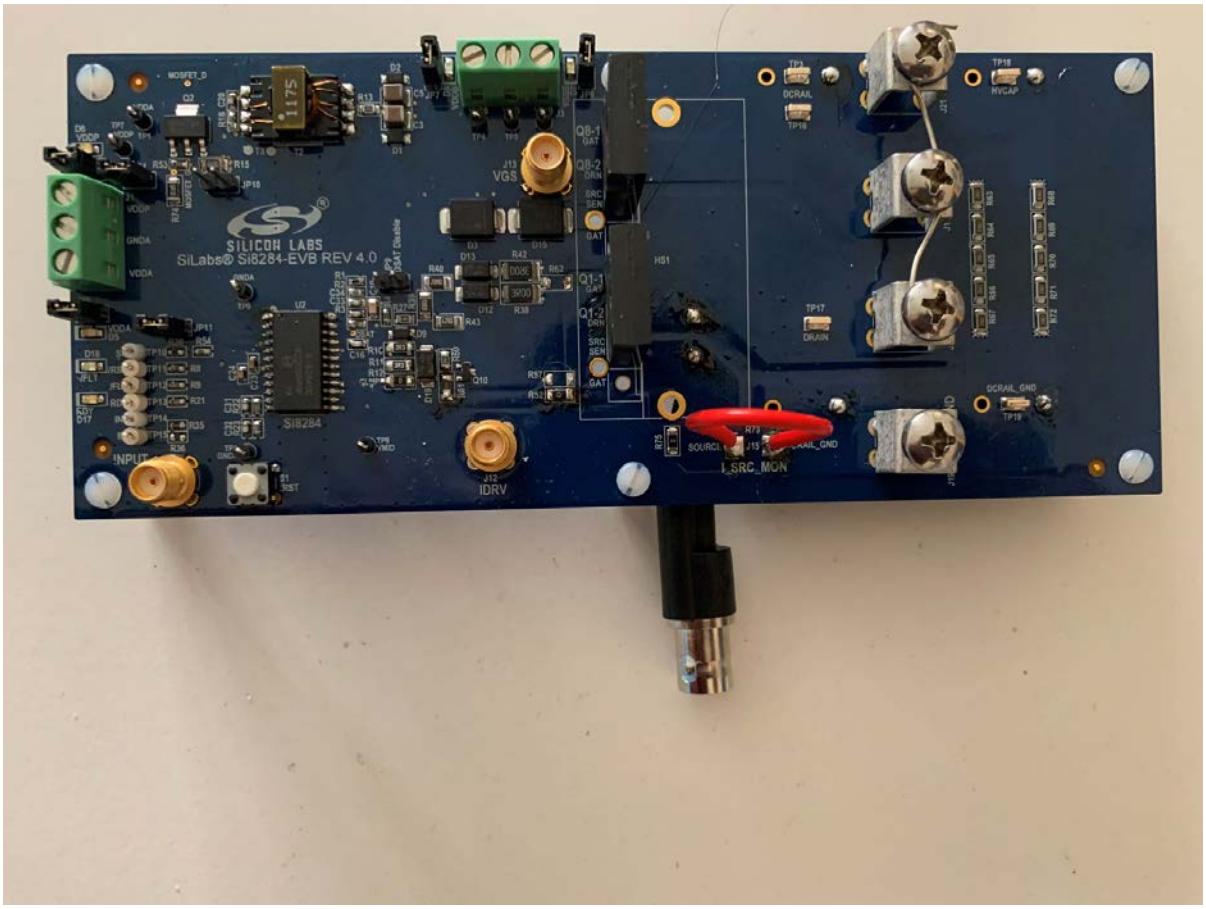


Figure 3.2. Si8284v2-EVB with Loop Current Sense

3.5 FET Gate Observation

J13 is an SMA-type coaxial connector for direct observation of the FET gate drive voltage. Its reference voltage is VMID/GNDB. The best approach to monitor this point is by using an SMA-to-BNC converter, then a BNC to scope probe adapter. Use a compensated probe and the high impedance input setting of the oscilloscope.

3.6 FET Drain Observation

Drain-source voltage of Q1 may be observed at BNC connector J20 by connecting a coaxial cable between J20 and a differential probe.

3.7 Gate Drive Test Load

A Gate Drive Test Load comprises C43 (220 nF) and R46 (0.05 Ω, 2 W). The current in this test load may be observed at J12, an SMA-type coaxial connector labeled IDRV. Its reference voltage is VMID. This is normally used with no FET installed at Q1. When installing Q1, remove C43 so there is no unnecessary load on the gate drive.

3.8 Switch Device Q1/Q8 Heatsink

There is a footprint provision for attaching a heat sink to Q1/Q8. The suggested parts are Ohmite CR101-25-AE or CR101-50-AE. Also use BERGQUIST SIL-PAD 900S Thermal Material Electrical Insulator between the heat sink and the MOSFET, as the heat sink is grounded to DCRAIL_GND while the drain of the MOSFET may be at hazardous high voltages.

3.9 Secondary Side Supply Voltage Modification Using JP12

JP12 provides a means to select VDDB and VSSB for use with either SiC devices or IGBT devices. The default jumper position is at pins 1 and 2 for VDDB = 15 V and VSSB = -3.5 V. Moving the jumper to pins 2 and 3 changes VDDB to 17 V and VSSB to -4.5 V for use with IGBT devices.

3.10 Quick Reference Table

Table 3.1. Test Point Descriptions

Test Point	Description	Referenced to:
TP1	VDDA	GNDA
TP2	GNDA	N/A
TP3	DCRAIL	DCRAIL_GND
TP4	VDDB	VMID
TP5	VMID	N/A
TP6	VSSB	VMID
TP7	VDDP	GNDA
TP8	VMID	N/A
J12	IDRV	VMID
J13	VGS	VMID
J15	I_SRC_MON	DCRAIL_GND
J20	DRAIN_SRC	N/A
TP9	GNDA	N/A
TP10	SH	GNDA
TP11	/RST	GNDA
TP12	/FLT	GNDA
TP13	RDY	GNDA
TP14	IN+	IN-
TP15	IN-	GNDA
TP16	DCRAIL	DCRAIL_GND
TP17	DRAIN	DCRAIL_GND
TP18	HVCAP	DCRAIL_GND
TP19	DCRAIL_GND	N/A
TP20	DSAT	VMID
TP21	DESAT	VMID
TPV10	MOSFET_D	GNDA
TPV11	MOSFET_G	GNDA
TPV12	CLMP	VSSB

4. Schematics

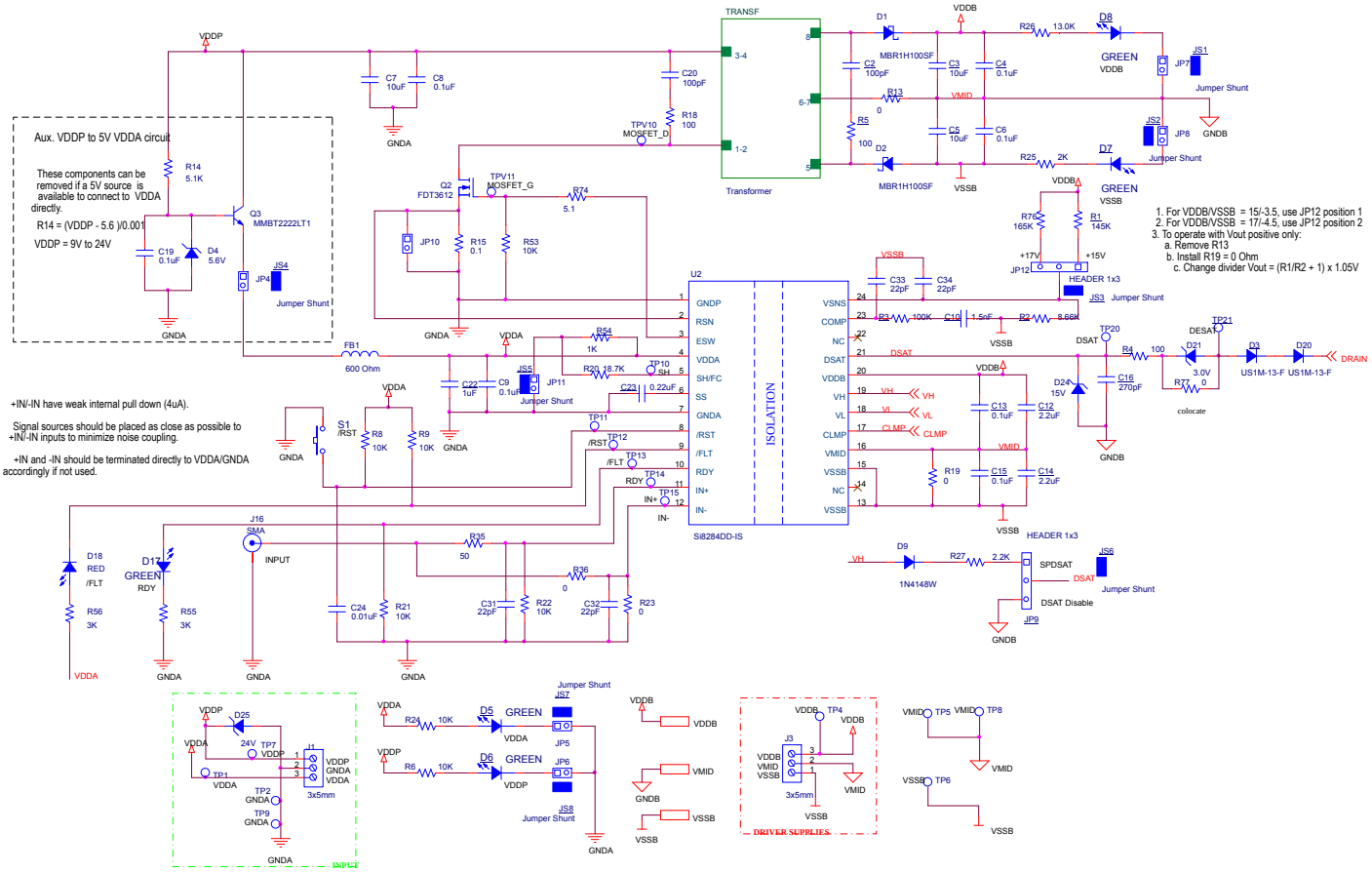


Figure 4.1. Si8284v2-EVB Low-Voltage Circuit Schematic

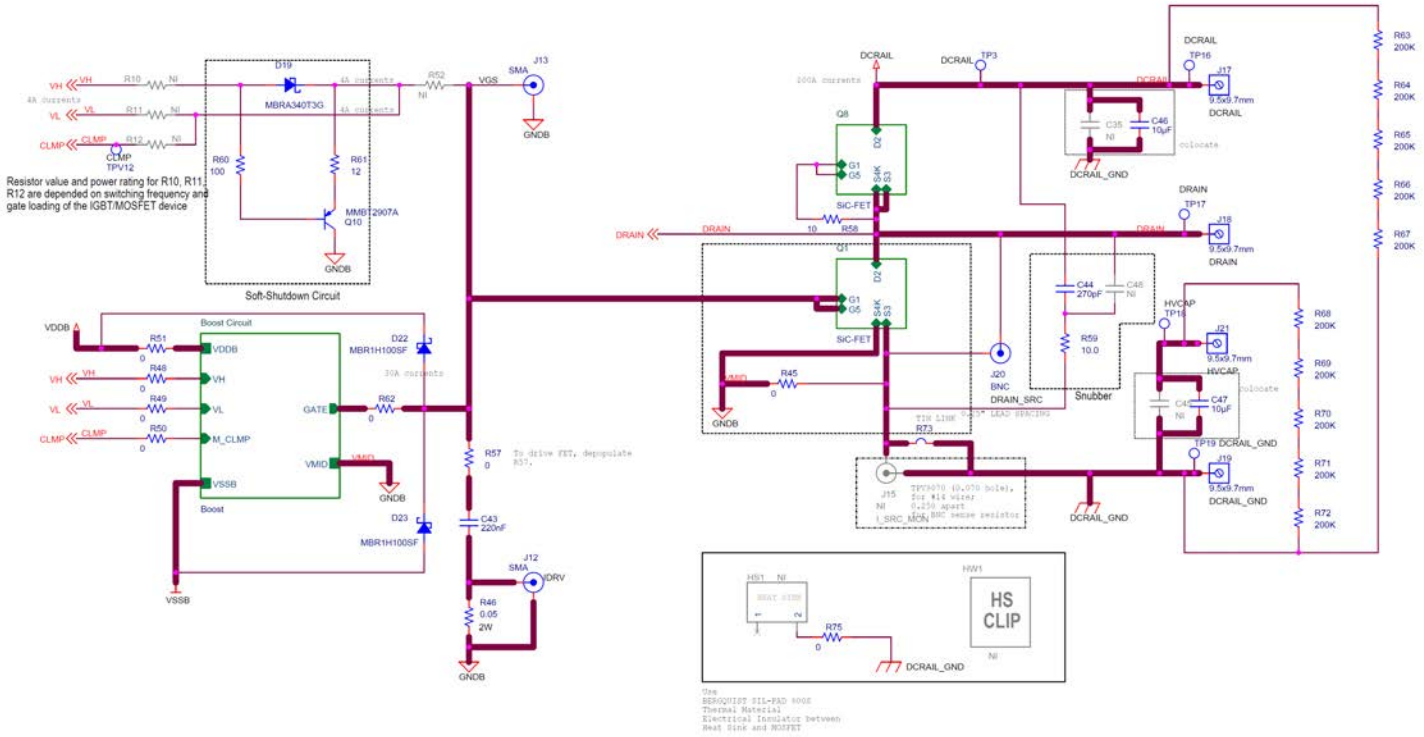


Figure 4.2. Si8284 High-Voltage Circuit Schematic

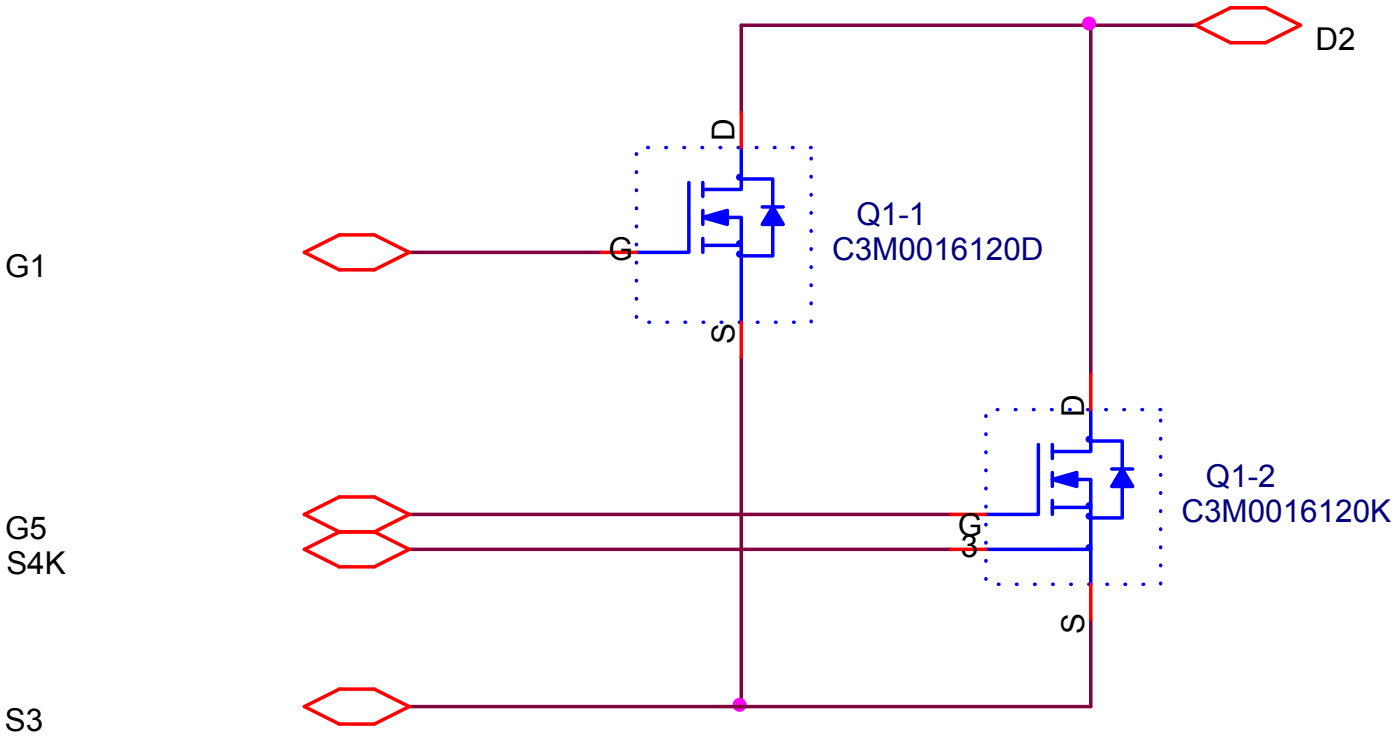


Figure 4.3. Switching Transistor Options

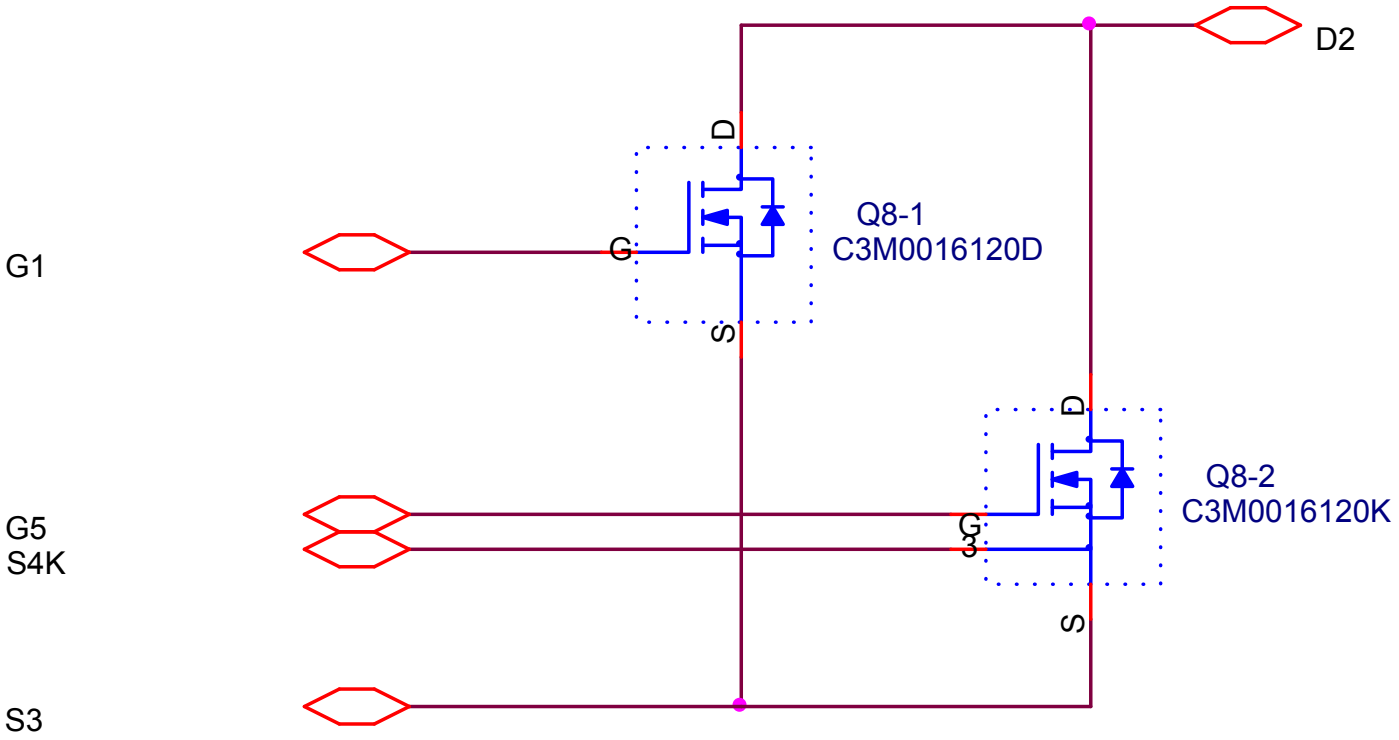


Figure 4.4. Diode-Connected Transistor Options

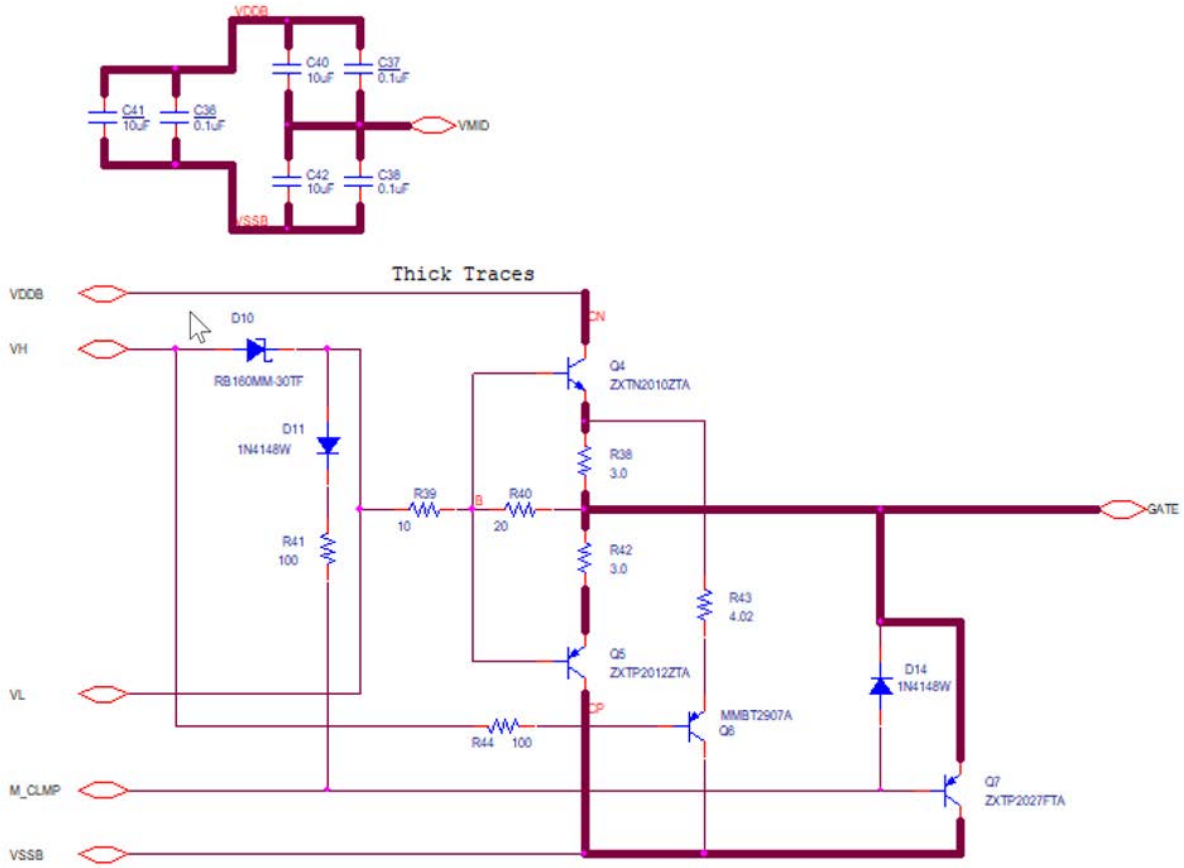


Figure 4.5. Boost Circuit Schematic

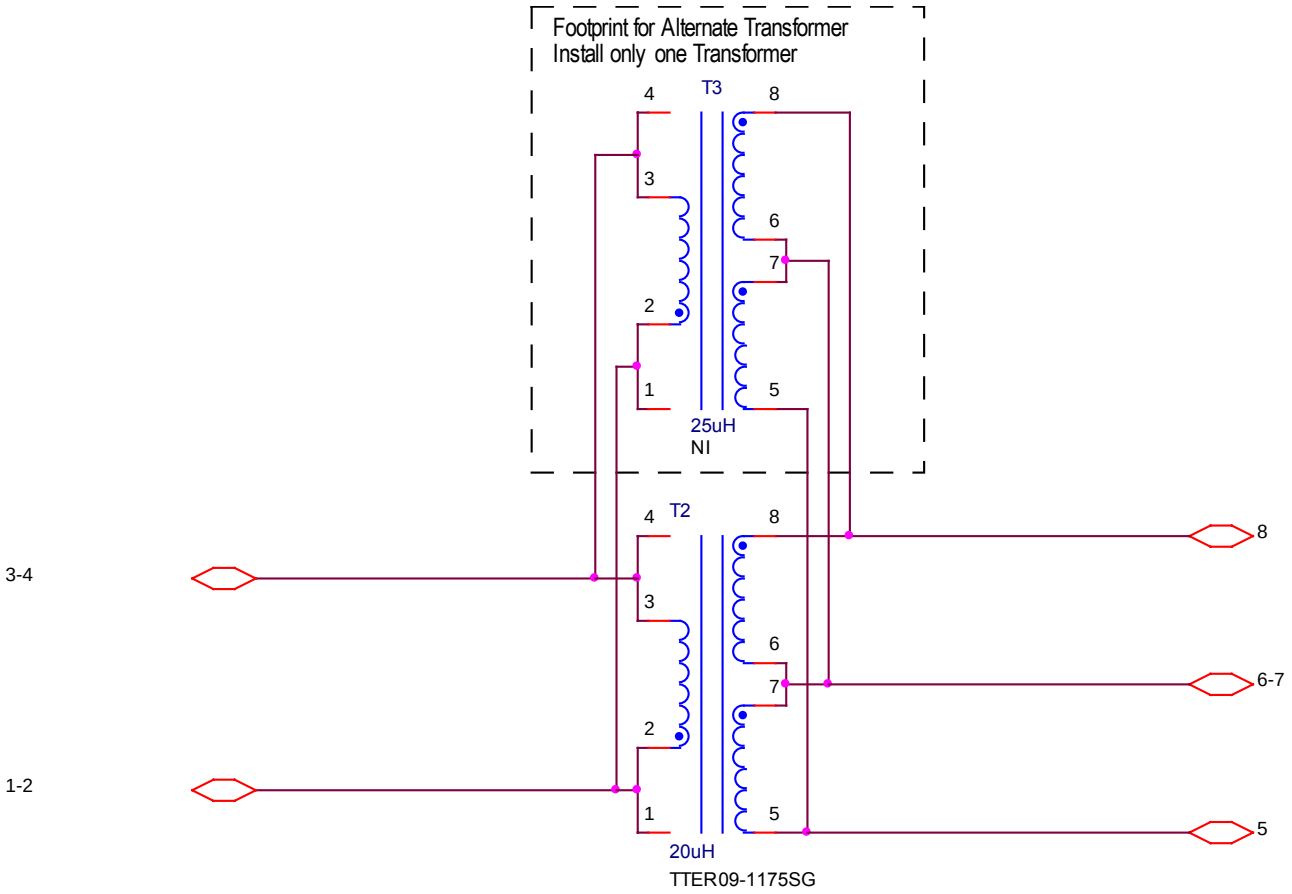


Figure 4.6. Transformer Options Schematic

5. Layout

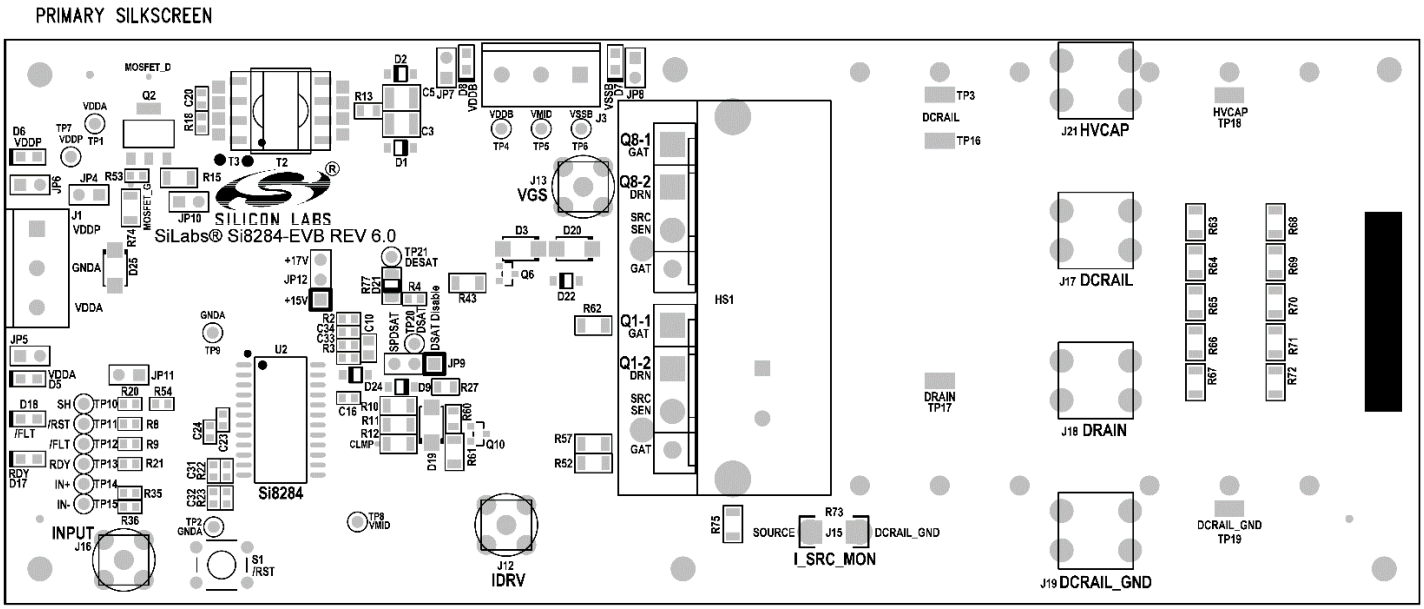


Figure 5.1. Si8284v2-EVB Top Silkscreen

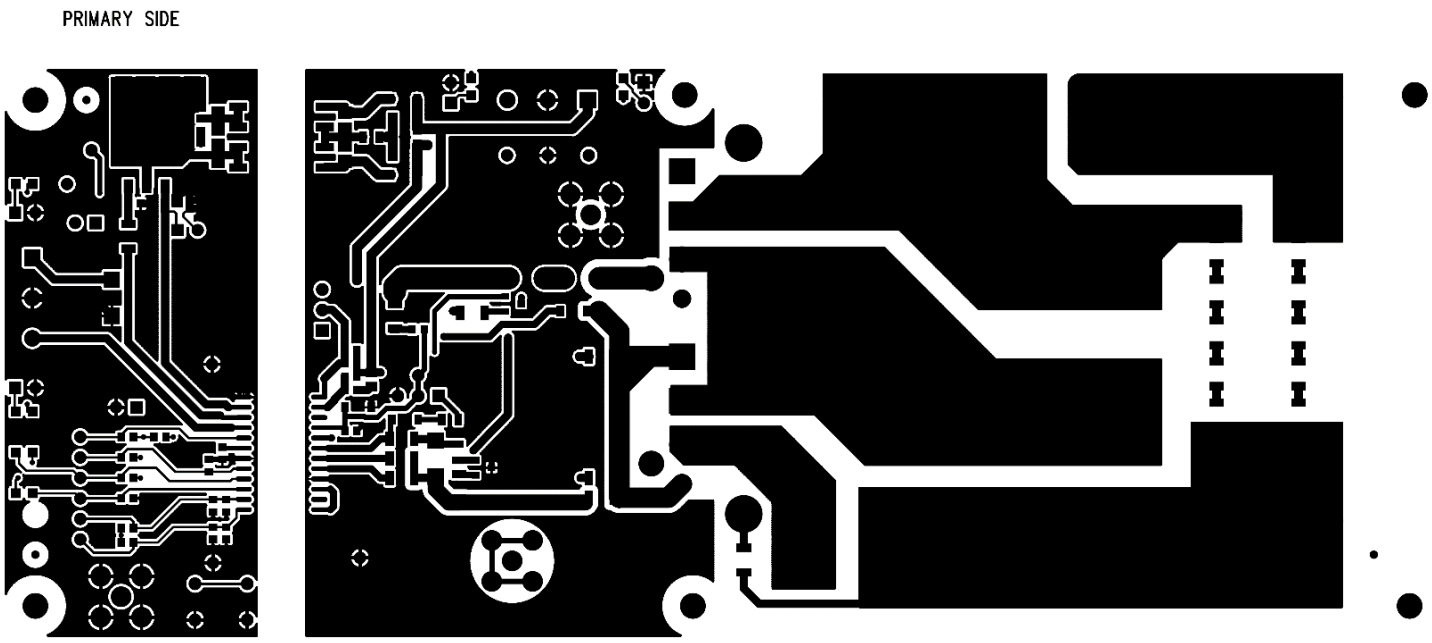


Figure 5.2. Si8284v2-EVB Top Copper

L02 – GND/HV ROUTE

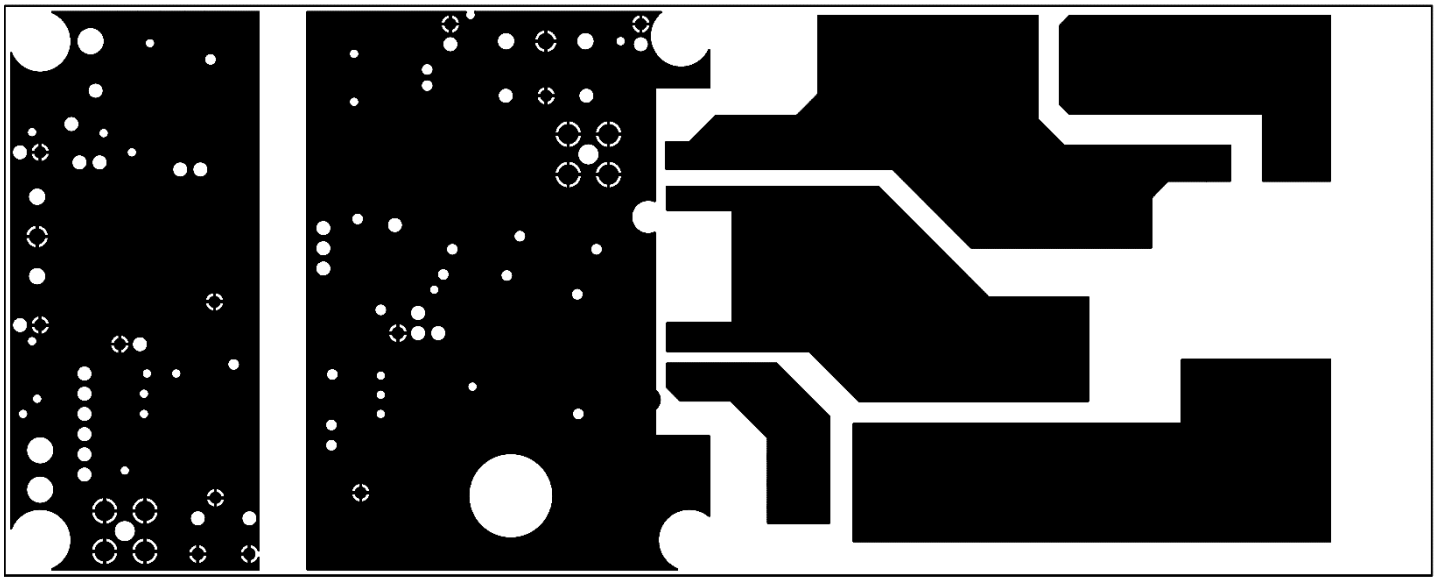


Figure 5.3. Si8284v2-EVB Copper Layer 2

L03 – GND/HV ROUTE

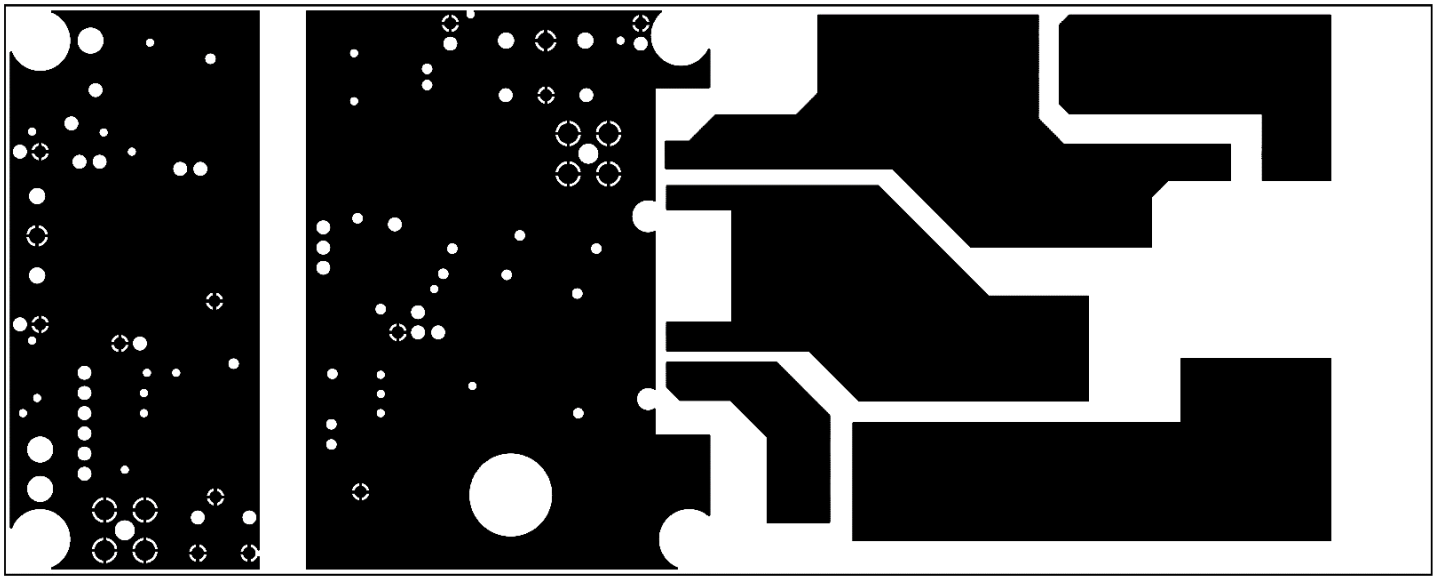


Figure 5.4. Si8284v2-EVB Copper Layer 3

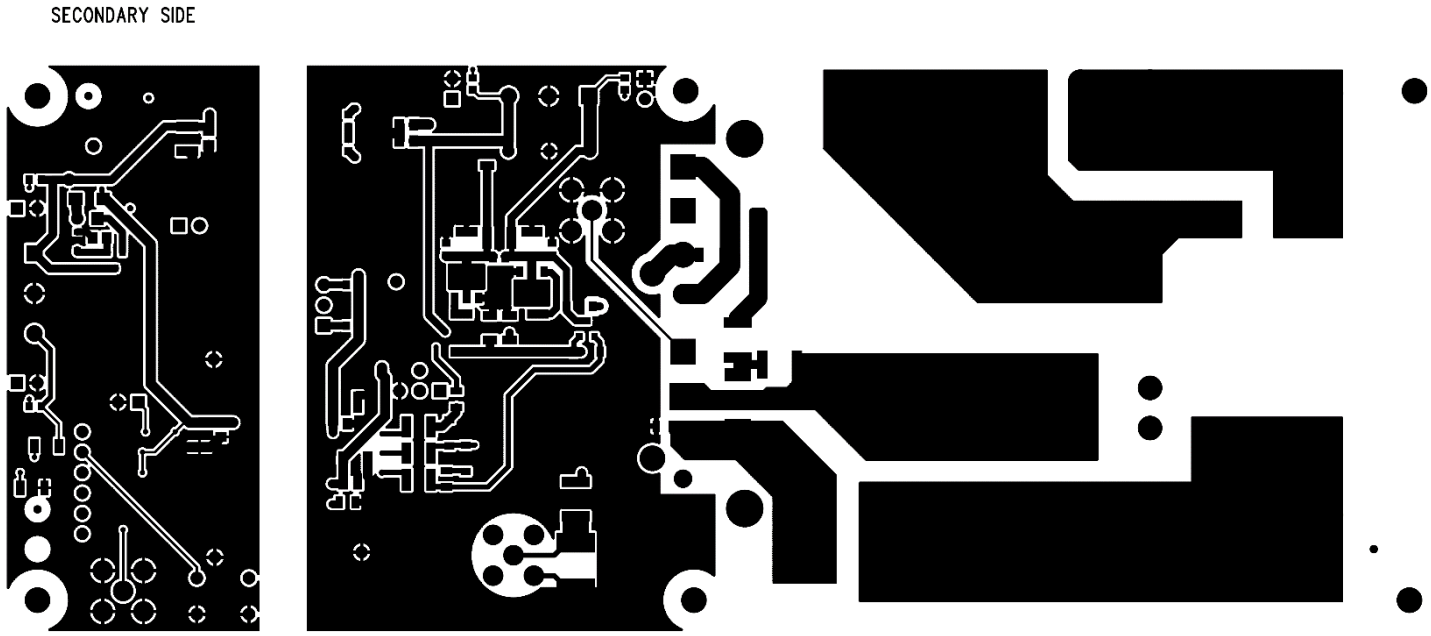


Figure 5.5. Si8284v2-EVB Bottom Copper

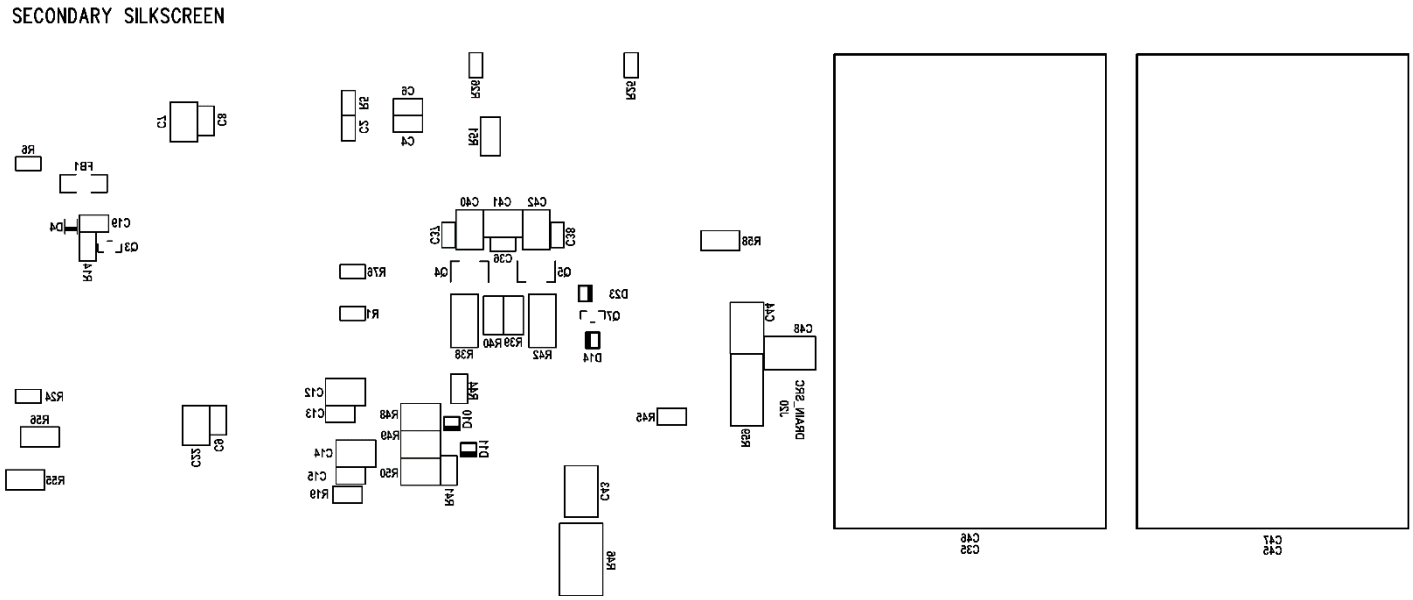


Figure 5.6. Si8284v2-EVB Bottom Silkscreen

6. Bill of Materials

Table 6.1. Si8284v2-EVB Bill of Materials

Part Reference	NI	Description	Manufacturer	Manufacturer Part Number
C2, C20		CAP, 100 pF, 50 V, ±20%, C0G, 0603	Venkel	C0603C0G500-101M
C3, C5, C7, C40, C41, C42		CAP, 10 uF, 50 V, ±20%, X7R, 1210	Venkel	C1210X7R500-106M
C4, C6, C8, C9, C13, C15, C19		CAP, 0.1 uF, 50 V, ±10%, X7R, 0805	Venkel	C0805X7R500-104K
C10		CAP, 1.5 nF, 250 V, ±10%, X7R, 0805	Venkel	C0805X7R251-152K
C12, C14		CAP, 2.2 uF, 50 V, ±10%, X7R, 1210	Kemet	C1210C225K5RACTU
C16		CAP, 270 pF, 50 V, ±10%, C0G, 0603	Venkel	C0603C0G500-271K
C22		CAP, 1 uF, 100 V, ±10%, X7R, 1210	Venkel	C1210X7R101-105K
C23		CAP, 0.22 uF, 25 V, ±10%, X7R, 0603	Venkel	C0603X7R250-224K
C24		CAP, 0.01 uF, 10 V, ±20%, X7R, 0603	Venkel	C0603X7R100-103M
C31, C32		CAP, 22 pF, 50 V, ±5%, C0G, 0603	KEMET	C0603C220J5GAC7013
C33, C34		CAP, 22 pF, 50 V, ±5%, C0G, 0603	Venkel	C0603C0G500-220J
C36, C37, C38		CAP, 0.1 uF, 50 V, ±10%, X7R, 0603	Yageo	CC0603KPX7R9BB104
C43		CAP, 220 nF, 50 V, ±5%, C0G, 1812	Venkel	C1812C0G500-224JNE
C44, C48		CAP, 270 pF, 2500 V, ±5%, C0G, 1812	Kemet	C1812C271JZGACTU
C46, C47		CAP, 10 µF, 1000 V, ±5%, Poly-Film, PTH	Vishay	MKP1848S61010JY2B
D1, D2, D22, D23		DIO, Schottky, 100 V, 1A, SOD123	On Semi	MBR1H100SF
D3, D20		DIO, DIODE, 1000 V, 1A, SMA	Diodes Incorporated	US1M-13-F
D4		DIO, ZENER, 5.6 V, 200mW, SOD323	DIODES INC	BZT52C5V6S-F-7
D5, D6, D7, D8, D17		LED, GREEN, 0805	LITE_ON INC	LTST-C170GKT
D9, D11, D14		DIO, fAST, 100 V, 2 A, SOD123	Diodes Inc	1N4148W
D10		DIO, SCHOTTKY, 30 V, 1 A, SOD123	Rohm Semiconductors	RB160MM-30TF
D18		LED, RED, 631 nM, 30 mA, 2 V, 54 mcd, 0805	LITE-ON TECHNOLOGY CORP	LTST-C170KRKT

Part Reference	NI	Description	Manufacturer	Manufacturer Part Number
D19		DIO, SCHOTTKY, 40 V, 3 A, SMA	On Semiconductor	MBRA340T3G
D21		DIO, ZENER, 3.0 V, 500 mW, SOD123	On Semi	MMSZ4683T1G
D24		DIO, ZENER, 15 V, 500 mW, SOD123	On Semi	MMSZ4702T1G
D25		DIO, ZENER, 24 V, 1000 mW, SMA	Diodes Inc.	SMAZ24-13-F
FB1		FERRITE BEAD, 600 Ohm @100 MHZ, 1206	Wurth	7.43E+08
JP4, JP5, JP6, JP7, JP8, JP10, JP11		Header, 2x1, 0.1in pitch, Tin Plated	Samtec	TSW-102-07-T-S
JP9, JP12		Header, 3x1, 0.1in pitch, gold/tin	Samtec	TSW-103-07-L-S
J1, J3		Terminal Block, 3 pos, 5 mm, 14-30AWG, 300 V, 10 A	Phoenix Contact	1729021
J12, J13, J16		CONN, SMA 50 Ohm, Straight, PTH	Johnson Components	142-0701-201
J17, J18, J19, J21		CONN, TERM SCREW, 10-32, PTH	Keystone Electronics	8174
J20		CONN, BNC, TEST LEAD, 4 in. LEADS , PTH	Mueller Electric Co	BU-5200-A-4-0
MH1, MH2, MH3, MH4, MH5, MH6		HDW, SCREW, 4-40 x 1/4 in. Pan Head, Slotted, Nylon	Richco Plastic Co	NSS-4-4-01
PCB1		PCB, BARE BOARD, Si8284v2-EVB REV 6.0	Silicon Labs	Si8284v2-EVB REV 6.0
Q2		TRANSISTOR, MOSFET, N-CHNL, 100 V, 3.7 A, 3 W, Switching, SOT223	Fairchild	FDT3612
Q3		TRANSISTOR, NPN, 30 V, 600 mA, SOT23	On Semi	MMBT2222LT1
Q4		TRANSISTOR, NPN, 60 V, 5 A, LO SAT, SOT89	Diodes Inc.	ZXTN2010Z
Q5		TRANSISTOR, PNP, -60 V, -4.3 A, MEDIUM POWER LOW SAT, SOT89	Zetex	ZXTP2012Z
Q6,Q10		TRANSISTOR, PNP, 60 V, 600 mA, SOT23	Diodes Inc.	MMBT2907A
Q7		TRANSISTOR, PNP, -60 V, -4 A, MEDIUM POWER, SOT23	Diodes Inc	ZXTP2027FTA
R1		RES, 145K, 1/10 W, ±1%, Metal-Film, 0603	KOA Speer	RN73H1JTTD1453F100
R2		RES, 8.66K, 1/16 W, ±1%, Thick-Film, 0603	Venkel	CR0603-16W-8661F
R3		RES, 100K, 1/10 W, ±1%, Thick-Film, 0603	Venkel	CR0603-10W-1003F
R4, R5, R18		RES, 100 Ohm, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-1000F

Part Reference	NI	Description	Manufacturer	Manufacturer Part Number
R6, R8, R9, R21, R24		RES, 10K, 1/16 W, ±1%, Thick-Film, 0603	Venkel	CR0603-16W-1002F
R13, R45		RES, 0 Ohm, 2 A, ThickFilm, 0805	Venkel	CR0805-10W-000
R14		RES, 5.1K, ¼ W, ±1%, ThickFilm, 0805	KOA Speer	RK73H2ATTD5101F
R15		RES, 0.1 Ohm, ½ W, ±1%, Thick-Film, 1206	Venkel	LCR1206-R100F
R20		RES, 18.7K, 1/16 W, ±1%, Thick-Film, 0603	Venkel	CR0603-16W-1872F
R22		RES, 10K, 1/10 W, ±5%, Thick-Film, 0603	Venkel	CR0603-10W-103J
R23		RES, 0 Ohm, 1 A, ThickFilm, 0603	Venkel	CR0603-16W-000
R25		RES, 2K, 1/10 W, ±1%, Thick-Film, 0603	Venkel	CR0603-10W-2001F
R26		RES, 13.0K, 1/16 W, ±1%, Thick-Film, 0603	Venkel	CR0603-16W-1302F
R27		RES, 2.2K, 1/10 W, ±5%, Thick-Film, 0805	Venkel	CR0805-10W-222J
R35		RES, 50 Ohm, 1/10W, ±1%, ThickFilm, 0603	Vishay Dale	CRCW060350R0FKEA
R38, R42		RES, 3.0 Ohm, 1W, ±1%, Thick-Film, 2010	Vishay	CRCW20103R00FKEFHP
R39, R58		RES, 10 Ohm, ¼ W, ±1%, Thick-Film, 1206	Venkel	CR1206-4W-10R0F
R40		RES, 20 Ohm, ¼ W, ±1%, Thick-Film, 1206	Venkel	CR1206-4W-20R0FT
R41, R44, R60		RES, 100 Ohm, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-1000F
R43		RES, 4.02 Ohm, 1/4W, ±1%, ThickFilm, 1206	Venkel	CR1206-4W-4R02F
R46		RES, 0.05 Ohm, 2 W, ±1%, Metal, 2816	VishayDale	WSL2816R0500FEH
R48, R49, R50		RES, 0 Ohm, 4 A, ThickFilm, 1210	Venkel	CR1210-4W-000
R51, R57, R62, R75, R77		RES, 0 Ohm, 2 A, ThickFilm, 1206	Venkel	CR1206-4W-000
R53		RES, 10K, 1/10 W, ±1%, Thick-Film, 0603	Venkel	CR0603-10W-1002F
R54		RES, 1K, 1/10 W, ±1%, Thick-Film, 0603	Venkel	CR0603-10W-1001F
R55, R56		RES, 3K, ¼ W, ±1%, ThickFilm, 1206	Panasonic	ERJ-8ENF3001V
R59		RES, 10.0 Ohm, 2 W, ±0.5%, ThickFilm, 2512	Venkel	CR2512-2W-10R0D

Part Reference	NI	Description	Manufacturer	Manufacturer Part Number
R61		RES, 12 Ohm, ¼ W, ±5%, Thick-Film, 1206	Venkel	CR1206-4W-120J
R63, R64, R65, R66, R67, R68, R69, R70, R71, R72		RES, 200K, ¼ W, ±1%, Thick-Film, 1206	Venkel	RC1206FR-07200KL
R73		RES, 5m	Ohmite	RW1S0BAR005JE
R74		RES, 5.1 Ohm, ¼ W, ±1%, Thick-Film, 1206	Yageo	RC1206FR-075R1L
R76		RES, 165K, 1/16 W, ±1%, Thick-Film, 0603	Venkel	CR0603-16W-1653F
SO1, SO2, SO3, SO4, SO5, SO6		HDW, STANDOFF, 1/4 IN. HEX, 4-40x3/4 IN., NYLON	Keystone Electronics	1902D
S1		SWITCH, PB, NO, MOMENTARY, TACTILE, LIGHT TOUCH 130GF, 6 MM, PTH	PANASONIC CORP	EVQ-PAD04M
TPV10, TPV11, TPV12		TESTPOINT Via	N/A	N/A
TP1, TP2, TP4, TP5, TP6, TP7, TP8, TP9		TESTPOINT, BLACK, PTH	Kobiconn	151-203-RC
TP3, TP16, TP17, TP18, TP19		TESTPOINT, MINIATURE, SMD	Keystone	5019
TP10, TP11, TP12, TP13, TP14, TP15, TP20, TP21		TESTPOINT, WHITE, PTH	Kobiconn	151-201-RC
T2		TRANSFORMER, POWER, FLYBACK, 5 kV ISOLATED, 20 uH PRIMARY, 3 windings N1 = 17, N2 = 11, N3 = 3, SMT	Mentech	TTER09-1175SG
U2		IC, 4 AMP ISODRIVER WITH INTEGRATED DC/DC CONVERTER, 13 V UVLO, SO24W		Si8284DD-IS
C35, C45	NI	CAP, 10 µF, 1000 V, ±5%, Poly-Film, PTH	Vishay	MKP1848S61010JY5B
HS1	NI	HEATSINK, TO-247, 50 MM WIDE, PTH	Ohmite	CR101-50-AE
HW1	NI	HEATSINK CAM CLIP, TH (TO-247)	Ohmite	CLA-TO-21E
J15	NI	CONN, JACK BNC VERT 10 mohm current viewing resistor	T&M Research	SDN-414-01
Q1-1, Q8-1	NI	TRANSISTOR, MOSFET, N-CHNL, 1200 V, 115 A, 16 mohm, SiC, Switching, TO-247	CREE	C3M0016120D
Q1-2, Q8-2	NI	TRANSISTOR, MOSFET, N-CHNL, 1200 V, 115 A, 16 mohm, SiC, Switching, TO-247	CREE	C3M0016120K
R10	NI	RES, 15 Ohm, ¼ W, ±5%, Thick-Film, 1206	Venkel	CR1206-4W-150J
R11	NI	RES, 10 Ohm, ¼ W, ±1%, Thick-Film, 1206	Venkel	CR1206-4W-10R0F
R12, R52	NI	RES, 0 Ohm, 2 A, ThickFilm, 1206	Venkel	CR1206-4W-000

Part Reference	NI	Description	Manufacturer	Manufacturer Part Number
R19	NI	RES, 0 Ohm, 2 A, ThickFilm, 0805	Venkel	CR0805-10W-000
R36	NI	RES, 0 Ohm, 1 A, ThickFilm, 0603	Venkel	CR0603-16W-000
T3	NI	TRANSFORMER, POWER, FLY-BACK, 5 kV ISOLATED, 25 uH PRIMARY, 2 windings N = 2, N = 1.21, SMT	UMEC	UTB02253s

7. Ordering Guide

Table 7.1. Si8284v2-EVB Ordering Guide

Ordering Part Number (OPN)	Description
Si8284v2-KIT	Si8284 Isolated gate driver evaluation board kit

8. Revision History

Revision 0.1

April, 2021

- Initial release.

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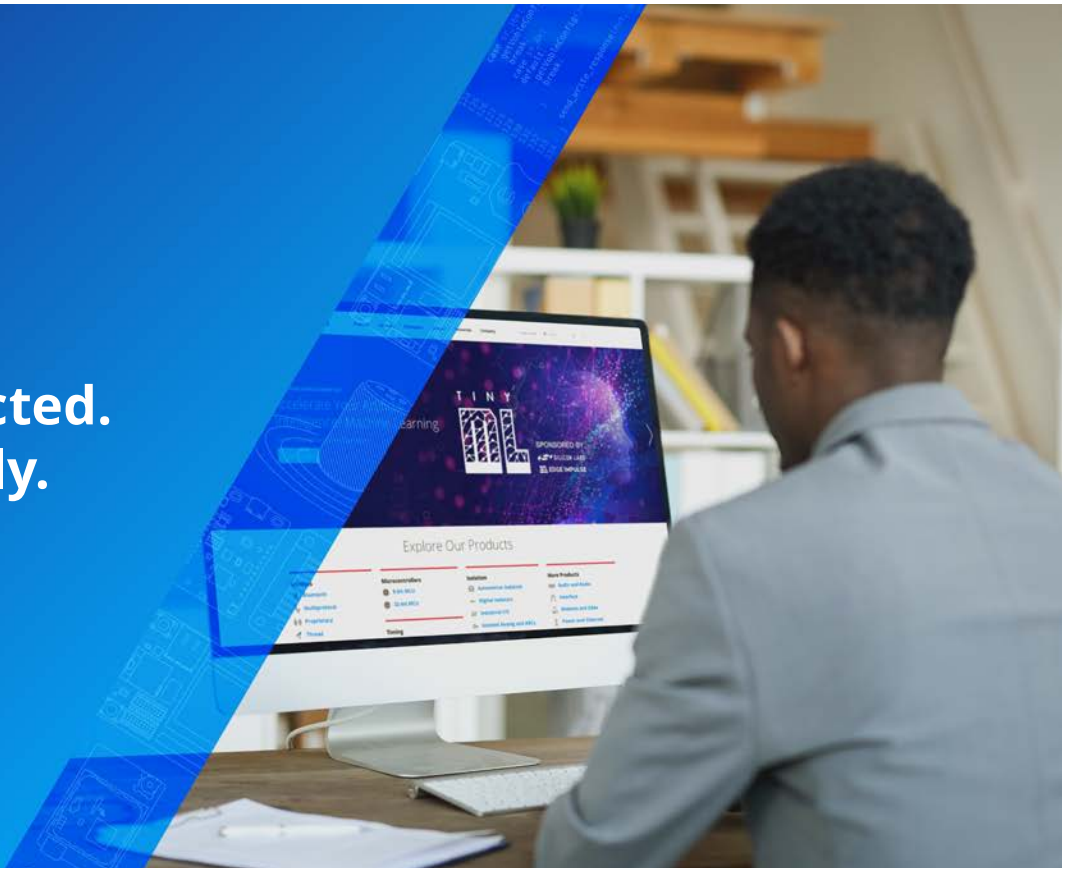

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