Low-Power Single and Dual-Channel Digital Isolators

Features

- High-speed operation
  - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage: 2.70–5.5 V
- Ultra low power (typical)
  5 V Operation:
  - < 2.1 mA per channel at 1 Mbps
  - < 6 mA per channel at 100 Mbps
  2.70 V Operation:
  - < 1.8 mA per channel at 1 Mbps
  - < 4 mA per channel at 100 Mbps
- High electromagnetic immunity
- Up to 2500 V_{RMS} isolation
- 60-year life at rated working voltage
- Precise timing (typical)
  - <10 ns worst case
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 6 ns minimum pulse width
- Transient Immunity 25 kV/µs
- Wide temperature range
  - –40 to 125 °C at 150 Mbps
- RoHS-compliant packages
  - SOIC-8 narrow body

Ordering Information:
See page 25.

Applications

- Industrial automation systems
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages when compared to legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges throughout their service life. For ease of design, only VDD bypass capacitors are required.

Data rates up to 150 Mbps are supported, and all devices achieve worst-case propagation delays of less than 10 ns. All products are safety certified by UL, CSA, and VDE and support withstand voltages of up to 2.5 kVrms. These devices are available in an 8-pin narrow-body SOIC package.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125	°C
Supply Voltage	V_{DD1}		2.70	—	5.5	V
	V_{DD2}		2.70	—	5.5	V

***Note:** The maximum ambient temperature is dependent upon data frequency, output loading, the number of operating channels, and supply voltage.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	°C
Operating Temperature	T_A	–40	—	125	°C
Supply Voltage (Revision C)[3]	V_{DD1}, V_{DD2}	–0.5	—	5.75	V
Supply Voltage (Revision D)[3]	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.
3. See "5. Ordering Guide" on page 25 for more information.

Table 3. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
DC Supply Current (All inputs 0 V or at Supply)						
Si8410Ax, Bx						
V_{DD1}		All inputs 0 DC	—	0.8	1.2	
V_{DD2}		All inputs 0 DC	—	0.8	1.2	mA
V_{DD1}		All inputs 1 DC	—	1.8	2.7	
V_{DD2}		All inputs 1 DC	—	0.8	1.2	
Si8420Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.0	1.5	
V_{DD2}		All inputs 0 DC	—	1.3	2.0	mA
V_{DD1}		All inputs 1 DC	—	3.0	4.5	
V_{DD2}		All inputs 1 DC	—	1.4	2.1	
Si8421Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.3	2.0	
V_{DD2}		All inputs 0 DC	—	1.3	2.0	mA
V_{DD1}		All inputs 1 DC	—	2.3	3.5	
V_{DD2}		All inputs 1 DC	—	2.3	3.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8410Ax, Bx						
V_{DD1}			—	1.3	2.0	mA
V_{DD2}			—	0.9	1.4	
Si8420Ax, Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.6	2.4	
Si8421Ax, Bx						
V_{DD1}			—	1.9	2.9	mA
V_{DD2}			—	1.9	2.9	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	1.3	2.0	mA
V_{DD2}			—	1.2	1.8	
Si8420Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	2.1	3.2	
Si8421Bx						
V_{DD1}			—	2.2	3.3	mA
V_{DD2}			—	2.2	3.3	
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	1.4	2.1	mA
V_{DD2}			—	4.6	5.8	
Si8420Bx						
V_{DD1}			—	2.2	3.3	mA
V_{DD2}			—	9.2	11.5	
Si8421Bx						
V_{DD1}			—	5.8	7.3	mA
V_{DD2}			—	5.8	7.3	
Timing Characteristics						
Si8410Ax, Si8420Ax, Si8421Ax						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8410Bx, Si8420Bx, Si8421Bx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	3.8	5.0	ns
Output Fall Time	t_f	C_L = 15 pF	—	2.8	3.7	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

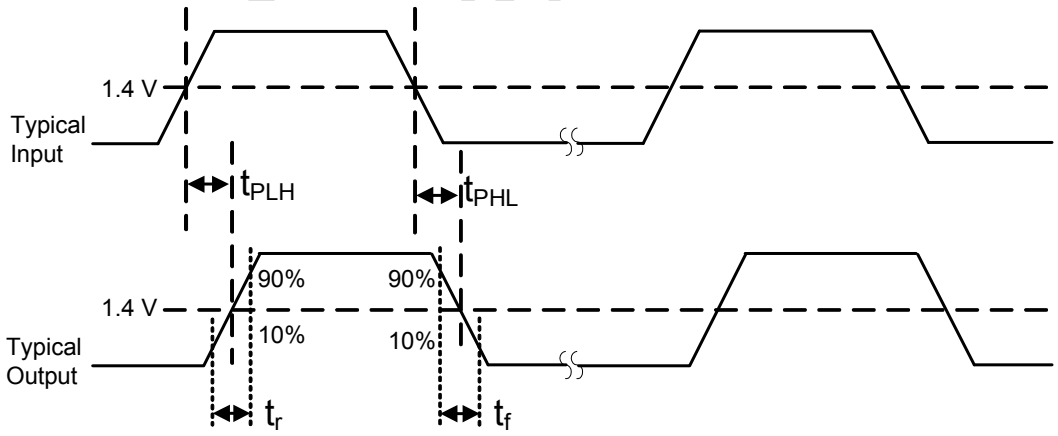


Figure 1. Propagation Delay Timing

Table 4. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8410Ax, Bx						
V_{DD1}		All inputs 0 DC	—	0.8	1.2	mA
V_{DD2}		All inputs 0 DC	—	0.8	1.2	
V_{DD1}		All inputs 1 DC	—	1.8	2.7	
V_{DD2}		All inputs 1 DC	—	0.8	1.2	
Si8420Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.0	1.5	mA
V_{DD2}		All inputs 0 DC	—	1.3	2.0	
V_{DD1}		All inputs 1 DC	—	3.0	4.5	
V_{DD2}		All inputs 1 DC	—	1.4	2.1	
Si8421Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.3	2.0	mA
V_{DD2}		All inputs 0 DC	—	1.3	2.0	
V_{DD1}		All inputs 1 DC	—	2.3	3.5	
V_{DD2}		All inputs 1 DC	—	2.3	3.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8410Ax, Bx						
V_{DD1}			—	1.3	2.0	mA
V_{DD2}			—	0.9	1.4	
Si8420Ax, Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.6	2.4	
Si8421Ax, Bx						
V_{DD1}			—	1.9	2.9	mA
V_{DD2}			—	1.9	2.9	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8410Bx V_{DD1} V_{DD2}			 — —	 1.3 1.2	 2.0 1.8	mA
Si8420Bx V_{DD1} V_{DD2}			 — —	 2.0 2.1	 3.0 3.2	mA
Si8421Bx V_{DD1} V_{DD2}			 — —	 2.2 2.2	 3.3 3.3	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8410Bx V_{DD1} V_{DD2}			 — —	 1.3 3.3	 2.0 4.9	mA
Si8420Bx V_{DD1} V_{DD2}			 — —	 2.0 6.5	 3.0 8.1	mA
Si8421Bx V_{DD1} V_{DD2}			 — —	 4.4 4.4	 5.5 5.5	mA
Timing Characteristics						
Si8410Ax, Si8420Ax, Si8421Ax						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8410Bx, Si8420Bx, Si8421Bx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	4.3	6.1	ns
Output Fall Time	t_f	C_L = 15 pF	—	3.0	4.3	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1]

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	85	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8410Ax, Bx						
V_{DD1}		All inputs 0 DC	—	0.8	1.2	mA
V_{DD2}		All inputs 0 DC	—	0.8	1.2	
V_{DD1}		All inputs 1 DC	—	1.8	2.7	
V_{DD2}		All inputs 1 DC	—	0.8	1.2	
Si8420Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.0	1.5	mA
V_{DD2}		All inputs 0 DC	—	1.3	2.0	
V_{DD1}		All inputs 1 DC	—	3.0	4.5	
V_{DD2}		All inputs 1 DC	—	1.4	2.1	
Si8421Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.3	2.0	mA
V_{DD2}		All inputs 0 DC	—	1.3	2.0	
V_{DD1}		All inputs 1 DC	—	2.3	3.5	
V_{DD2}		All inputs 1 DC	—	2.3	3.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8410Ax, Bx						
V_{DD1}			—	1.3	2.0	mA
V_{DD2}			—	0.9	1.4	
Si8420Ax, Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.6	2.4	
Si8421Ax, Bx						
V_{DD1}			—	1.9	2.9	mA
V_{DD2}			—	1.9	2.9	

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8410Bx V_{DD1} V_{DD2}			— —	1.3 1.2	2.0 1.8	mA
Si8420Bx V_{DD1} V_{DD2}			— —	2.0 2.1	3.0 3.2	mA
Si8421Bx V_{DD1} V_{DD2}			— —	2.2 2.2	3.3 3.3	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8410Bx V_{DD1} V_{DD2}			— —	1.3 2.7	2.0 4.0	mA
Si8420Bx V_{DD1} V_{DD2}			— —	2.0 5.2	3.0 6.5	mA
Si8421Bx V_{DD1} V_{DD2}			— —	3.7 3.7	4.6 4.6	mA
Timing Characteristics						
Si8410Ax, Si8420Ax, Si8421Ax						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

Notes:
1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8410Bx, Si8420Bx, Si8421Bx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	1.5	2.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	4.8	6.5	ns
Output Fall Time	t_f	C_L = 15 pF	—	3.2	4.6	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Start-up Time[4]	t_{SU}		—	15	40	µs

Notes:
1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 6. Regulatory Information*

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 300 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 130 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 560 V_{peak} for basic insulation working voltage.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for basic insulation.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see "5. Ordering Guide" on page 25.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
Nominal Air Gap (Clearance)[1]	L(IO1)		4.9	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		4.01	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V_{RMS}
Erosion Depth	ED		0.040	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.0	pF
Input Capacitance[3]	C_I		4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values as detailed in "6. Package Outline: 8-Pin Narrow Body SOIC" on page 26. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-8 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 package.
2. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–4 are shorted together to form the first terminal and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Condition	Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Case Temperature	T_S		—	—	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 140 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	160	mA
Device Power Dissipation[2]	P_D		—	—	150	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 2.
2. The Si841x/2x is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 °C, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	140	—	°C/W

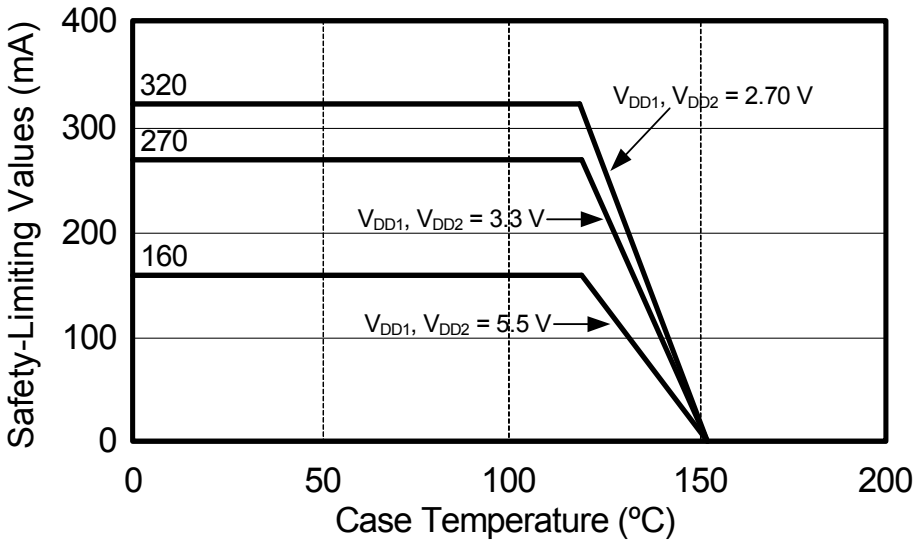


Figure 2. (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Functional Description

2.1. Theory of Operation

The operation of an Si84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si84xx channel is shown in Figure 3.

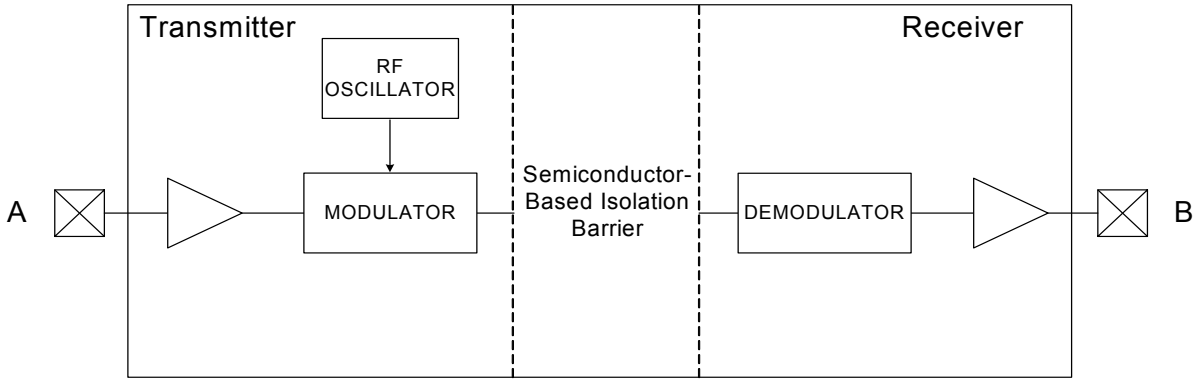


Figure 3. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 4 for more details.

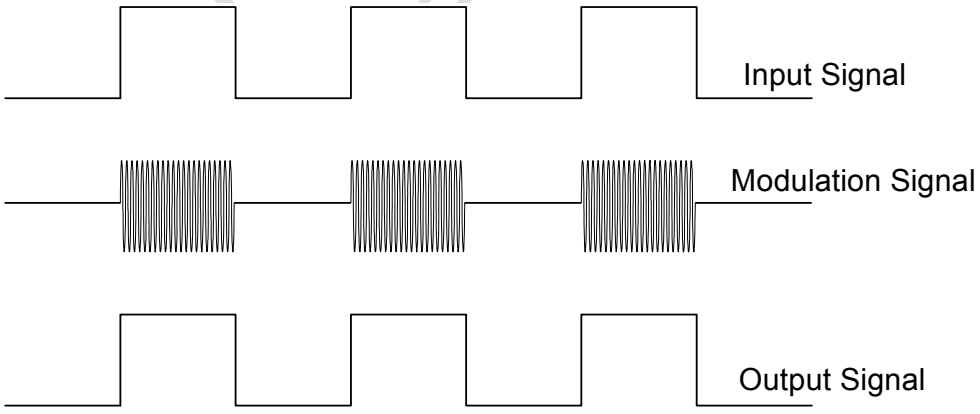


Figure 4. Modulation Scheme

2.2. Eye Diagram

Figure 5 illustrates an eye-diagram taken on an Si8410. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8410 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

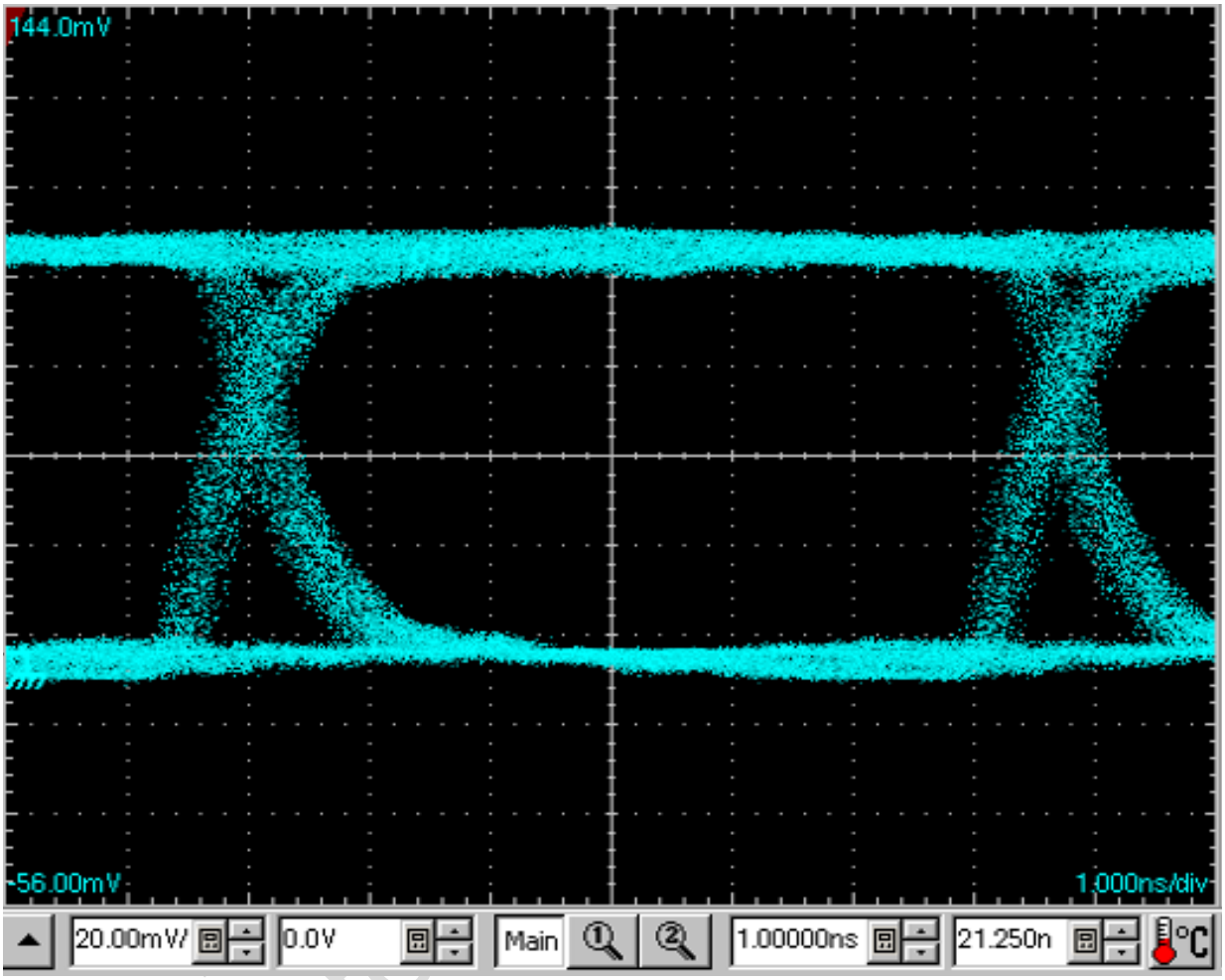


Figure 5. Eye Diagram

2.3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Table 12.

Table 12. Si84xx Logic Operation Table

V_I Input[1,4]	VDDI State[1,2,3]	VDDO State[1,2,3]	V_O Output[1,4]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	L	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. Powered (P) state is defined as 2.70 V < VDD < 5.5 V.
3. Unpowered (UP) state is defined as VDD = 0 V.
4. X = not applicable; H = Logic High; L = Logic Low.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.

2.4. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 13 and Table 7 on page 14 detail the working voltage and creepage/clearance capabilities of the Si84xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, etc.) requirements before starting any design that uses a digital isolator.

The following sections detail the recommended bypass and decoupling components necessary to ensure robust overall performance and reliability for systems using the Si84xx digital isolators.

2.4.1. Supply Bypass

Digital integrated circuit components typically require 0.1 µF (100 nF) bypass capacitors when used in electrically quiet environments. However, digital isolators are commonly used in hazardous environments with excessively noisy power supplies. To counteract these harsh conditions, it is recommended that an additional 1 µF bypass capacitor be added between VDD and GND on both sides of the package. The capacitors should be placed as close as possible to the package to minimize stray inductance. If the system is excessively noisy, it is recommended that the designer add 50 to 100 Ω resistors in series with the VDD supply voltage source and 50 to 300 Ω resistors in series with the digital inputs/outputs (see Figure 6). For more details, see "3. Errata and Design Migration Guidelines" on page 23.

All components upstream or downstream of the isolator should be properly decoupled as well. If these components are not properly decoupled, their supply noise can couple to the isolator inputs and outputs, potentially causing damage if spikes exceed the maximum ratings of the isolator (6 V). In this case, the 50 to 300 Ω resistors protect the isolator's inputs/outputs (note that permanent device damage may occur if the absolute maximum ratings are exceeded). Functional operation should be restricted to the conditions specified in Table 1, “Recommended Operating Conditions,” on page 4.

2.4.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

2.4.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The series termination resistor values should be scaled appropriately while keeping in mind the recommendations described in “2.4.1. Supply Bypass” above.

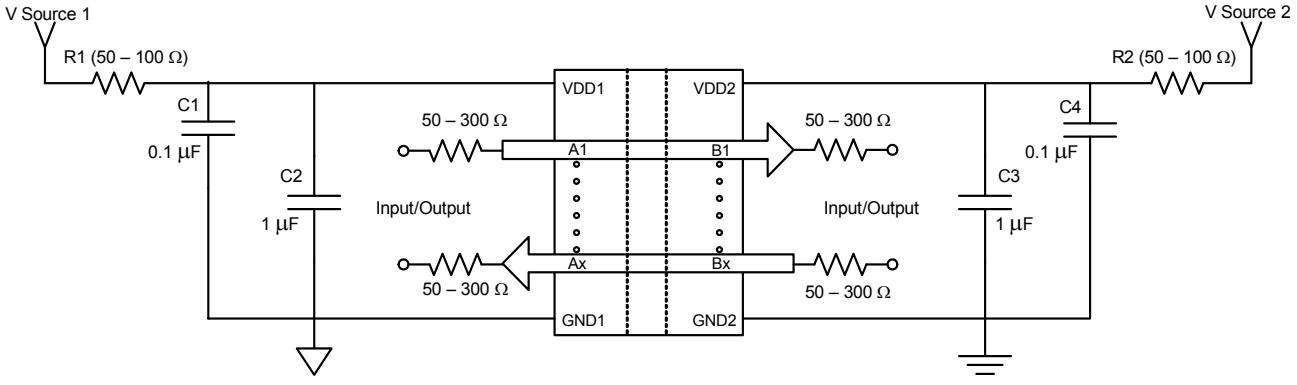


Figure 6. Recommended Bypass Components for the Si84xx Digital Isolator Family

2.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 3, 4, and 5 for actual specification limits.

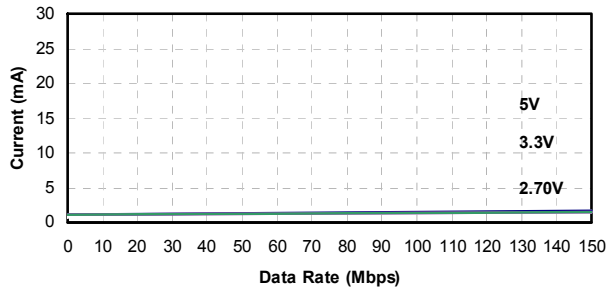


Figure 7. Si8410 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

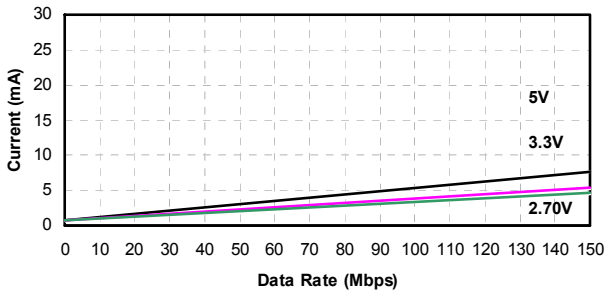


Figure 10. Si8410 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

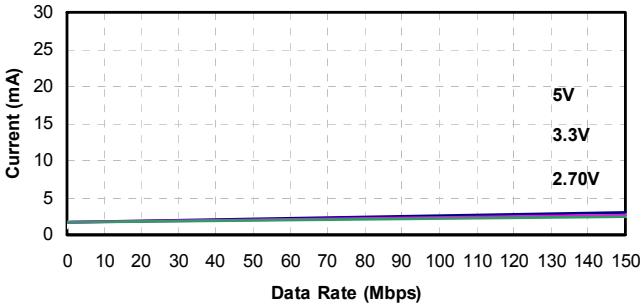


Figure 8. Si8420 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

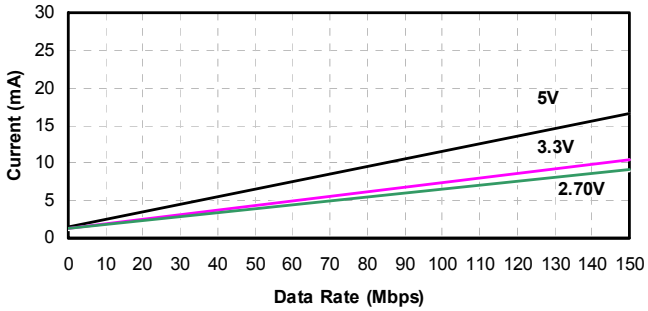


Figure 11. Si8420 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

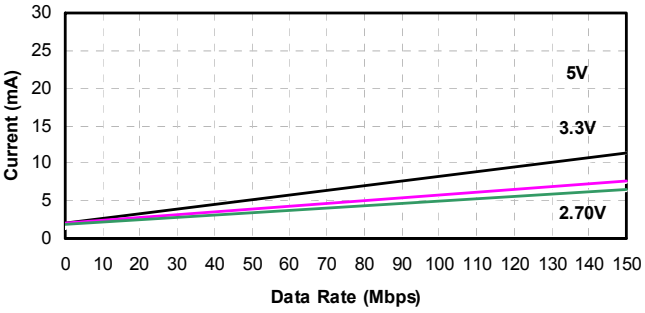


Figure 9. Si8421 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

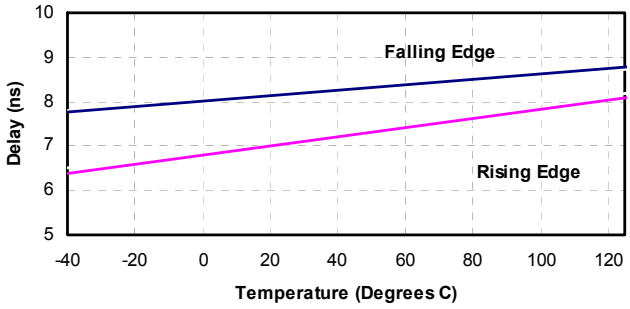


Figure 12. Propagation Delay vs. Temperature

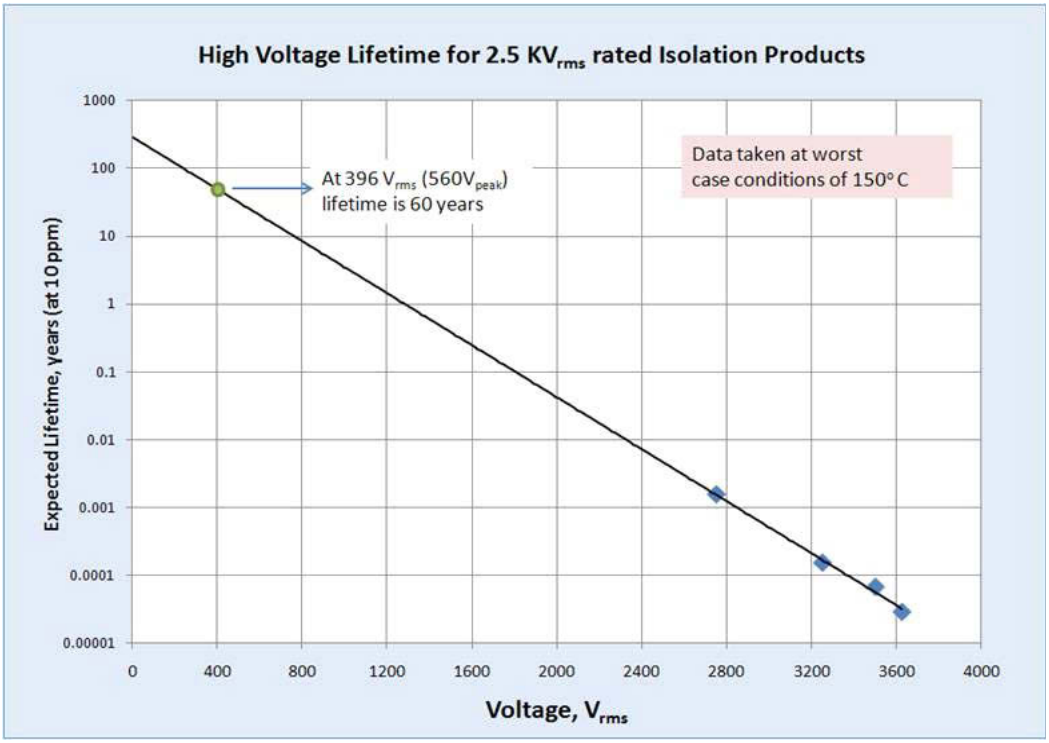


Figure 13. Si84xx Time-Dependent Dielectric Breakdown

3. Errata and Design Migration Guidelines

The following errata apply to Revision C devices only. See "5. Ordering Guide" on page 25 for more details. No errata exist for Revision D devices.

3.1. Power Supply Bypass Capacitors (Revision C and Revision D)

When using the Si84xx isolators with power supplies ≥ 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than 0.5 V/µs (which is > 9 µs for a ≥ 4.5 V supply). Although rise time is power supply dependent, ≥ 1 µF capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

3.1.1. Resolution

For recommendations on resolving this issue, see "2.4.1. Supply Bypass" on page 20. Additionally, refer to "5. Ordering Guide" on page 25 for current ordering information.

3.2. Latch Up Immunity (Revision C Only)

Si84xx latch up immunity generally exceeds ± 200 mA per pin. Exceptions: Certain pins provide < 100 mA of latch-up immunity. To increase latch-up immunity on these pins, 100 Ω of equivalent resistance must be included in series with *all* of the pins listed in Table 13. The 100 Ω equivalent resistance can be comprised of the source driver's output resistance and a series termination resistor. The Si8410 is not affected by the latch up immunity issue described above.

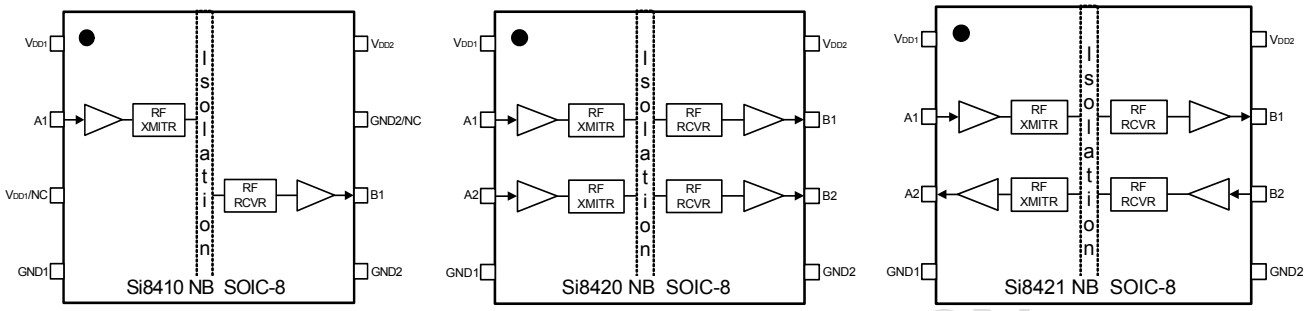
3.2.1. Resolution

This issue has been corrected with Revision D of the device. Refer to “5. Ordering Guide” for current ordering information.

Table 13. Affected Ordering Part Numbers (Revision C Only)

Affected Ordering Part Numbers*	Device Revision	Pin#	Name	Pin Type
SI8420SV-C-IS, SI8421SV-C-IS	C	3	A2	Input or Output
		7	B1	Output
***Note:** SV = Speed Grade/Isolation Rating (AA, AB, BA, BB).				

4. Pin Descriptions



Name	SOIC-8 Pin# Si8410	SOIC-8 Pin# Si8420/21	Type	Description
V_{DD1}/NC*	1,3	1	Supply	Side 1 power supply.
GND1	4	4	Ground	Side 1 ground.
A1	2	2	Digital I/O	Side 1 digital input or output.
A2	NA	3	Digital I/O	Side 1 digital input or output.
B1	6	7	Digital I/O	Side 2 digital input or output.
B2	NA	6	Digital I/O	Side 2 digital input or output.
V_{DD2}	8	8	Supply	Side 2 power supply.
GND2/NC*	5,7	5	Ground	Side 2 ground.
***Note:** No Connect. These pins are not internally connected. They can be left floating, tied to VDD or tied to GND.				

5. Ordering Guide

These devices are not recommended for new designs. Please see the Si861x datasheet for replacement options.

Table 14. Ordering Guide for Valid OPNs[1]

Ordering Part Number (OPN)	Alternative Part Number (APN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Package Type
Revision D Devices[2]						
Si8410AB-D-IS	Si8610AB-B-IS	1	0	1	2.5 kVrms	NB SOIC-8
Si8410BB-D-IS	Si8610BB-B-IS	1	0	150		
Si8420AB-D-IS	Si8620AB-B-IS	2	0	1		
Si8420BB-D-IS	Si8620BB-B-IS	2	0	150		
Si8421AB-D-IS	Si8621AB-B-IS	1	1	1		
Si8421BB-D-IS	Si8621BB-B-IS	1	1	150		
Revision C Devices[2]						
Si8410AB-C-IS	Si8610AB-B-IS	1	0	1	2.5 kVrms	NB SOIC-8
Si8410BB-C-IS	Si8610BB-B-IS	1	0	150		
Si8420AB-C-IS	Si8620AB-B-IS	2	0	1		
Si8420BB-C-IS	Si8620BB-B-IS	2	0	150		
Si8421AB-C-IS	Si8621AB-B-IS	1	1	1		
Si8421BB-C-IS	Si8621BB-B-IS	1	1	150		

Notes:
1. All packages are RoHS-compliant. Moisture sensitivity level is MSL2A with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.
2. Revision C and Revision D devices are supported for existing designs.

6. Package Outline: 8-Pin Narrow Body SOIC

Figure 14 illustrates the package details for the Si841x. Table 15 lists the values for the dimensions shown in the illustration.

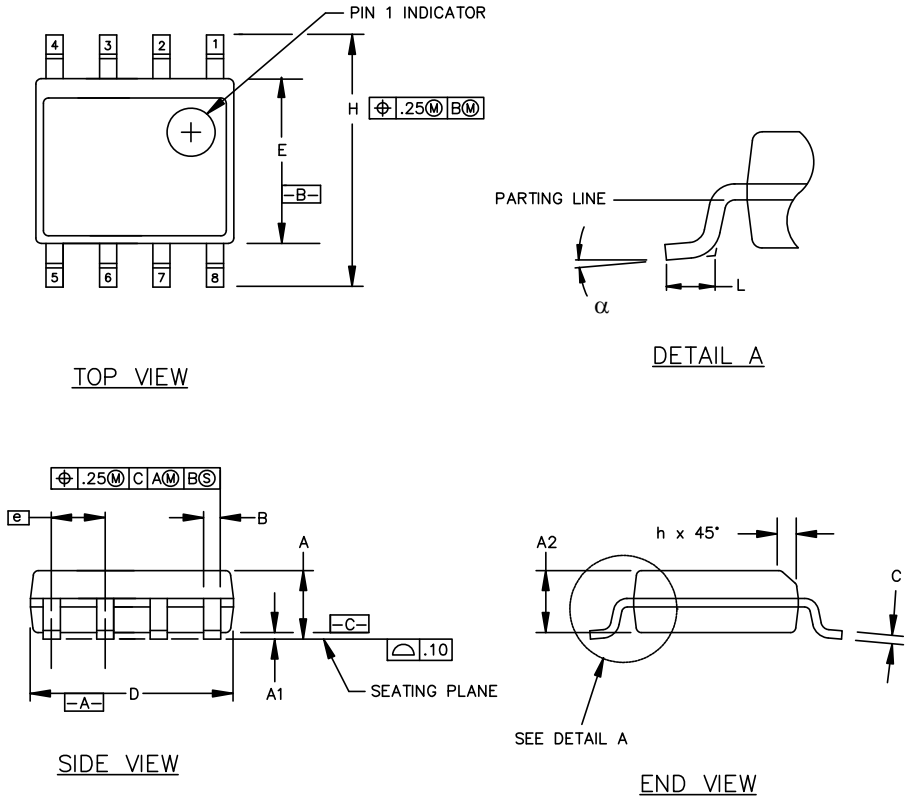


Figure 14. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 15. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

7. Land Pattern: 8-Pin Narrow Body SOIC

Figure 15 illustrates the recommended land pattern details for the Si841x in an 8-pin narrow-body SOIC. Table 16 lists the values for the dimensions shown in the illustration.

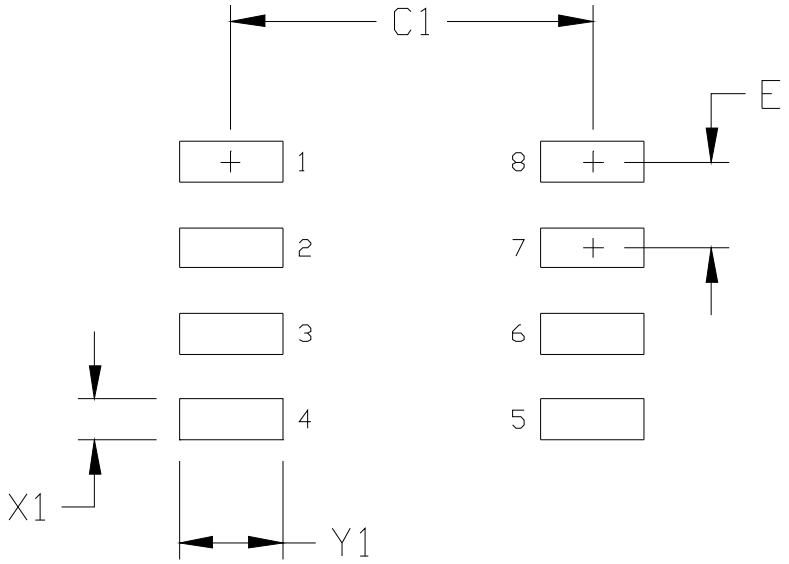


Figure 15. PCB Land Pattern: 8-Pin Narrow Body SOIC

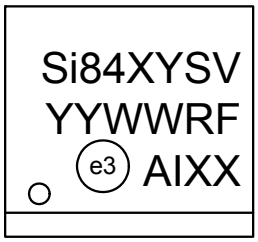
Table 16. PCM Land Pattern Dimensions (8-Pin Narrow Body SOIC)

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Top Marking: 8-Pin Narrow Body SOIC

8.1. 8-Pin Narrow Body SOIC Top Marking



8.2. Top Marking Explanation

Table 17. Top Marking Explanations

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (2, 1) Y = # of reverse channels (1, 0) S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by Assembly Contractor. Corresponds to the year and workweek of the mold date.
	R = Product (OPN) Revision F = Wafer Fab	
Line 3 Marking:	Circle = 1.1 mm Diameter Left-Justified	“e3” Pb-Free Symbol First Two Characters of the Manufacturing Code
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last Four Characters of the Manufacturing Code

Document Change List

Revision 0.11 to Revision 0.21

- Rev 0.21 is the first revision of this document that applies to the new series of ultra low power isolators featuring pinout and functional compatibility with previous isolator products.
- Updated “1. Electrical Specifications”.
- Updated “5. Ordering Guide”.
- Added “8. Top Marking: 8-Pin Narrow Body SOIC”.

Revision 0.21 to Revision 0.22

- Updated all specs to reflect latest silicon.

Revision 0.22 to Revision 0.23

- Updated all specs to reflect latest silicon.
- Added "3. Errata and Design Migration Guidelines" on page 23.

Revision 0.23 to Revision 1.0

- Updated document to reflect availability of Revision D silicon.
- Updated Tables 3,4, and 5.
  - Updated all supply currents and channel-channel skew.
- Updated Table 2.
  - Updated absolute maximum supply voltage.
- Updated Table 7.
  - Updated clearance and creepage dimensions.
- Updated "3. Errata and Design Migration Guidelines" on page 23.
- Updated "5. Ordering Guide" on page 25.

Revision 1.0 to Revision 1.1

- Updated Tables 3, 4, and 5.
  - Updated notes in tables to reflect output impedance of 85 Ω.
  - Updated rise and fall time specifications.
  - Updated CMTI value.

Revision 1.1 to Revision 1.2

- Updated document throughout to include MSL improvements to MSL2A.
- Updated "5. Ordering Guide" on page 25.
  - Updated Note 1 in ordering guide table to reflect improvement and compliance to MSL2A moisture sensitivity level.

Revision 1.2 to Revision 1.3

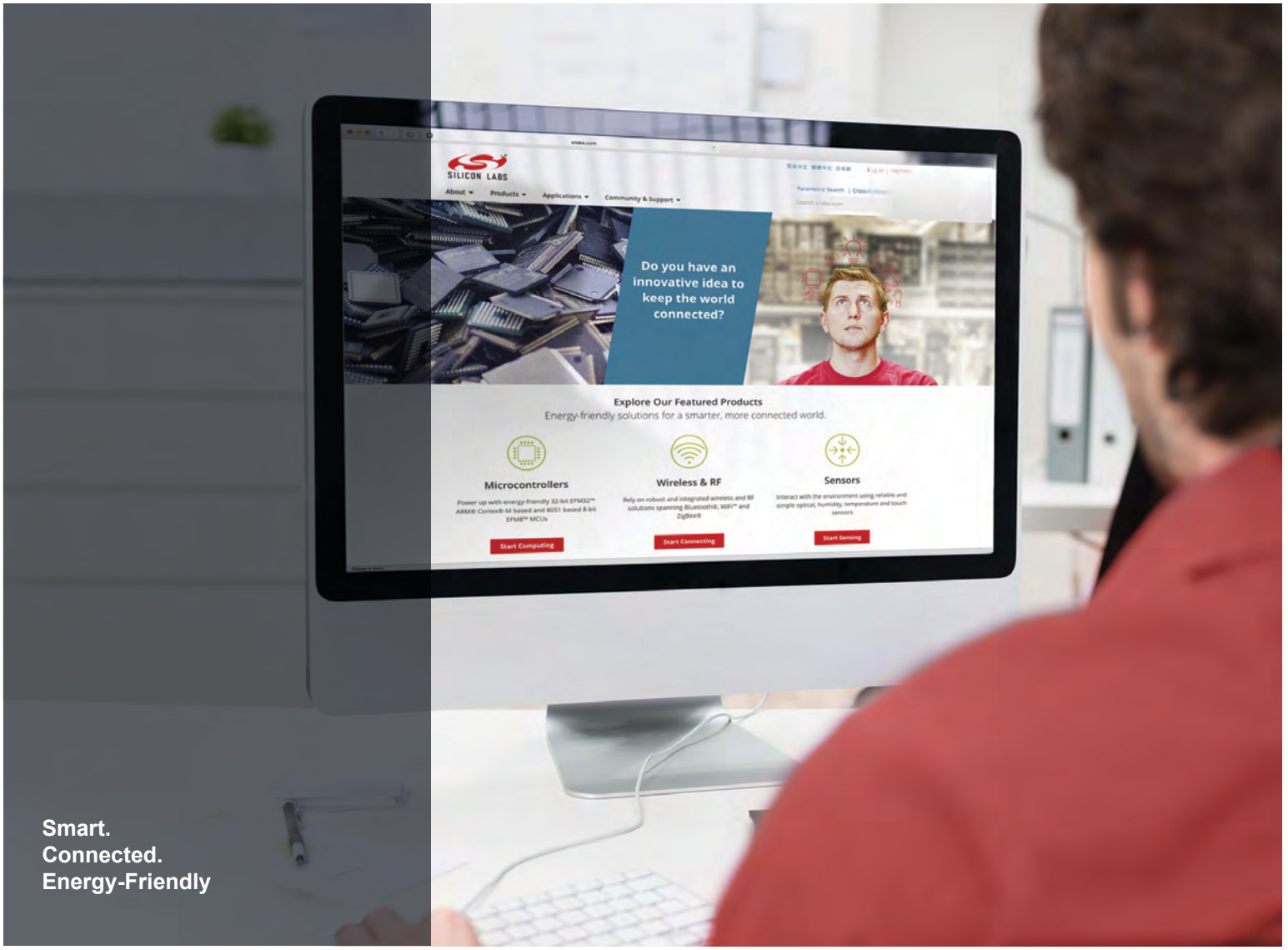
- Updated " Features" on page 1.
- Moved Tables 1 and 2 to page 4.
- Updated Tables 6, 7, 8, and 9.
- Updated Table 12 footnotes.
- Added Figure 13, “Si84xx Time-Dependent Dielectric Breakdown,” on page 22.

Revision 1.3 to Revision 1.4

- Updated "2.4.1. Supply Bypass" on page 20.
- Added Figure 6, “Recommended Bypass Components for the Si84xx Digital Isolator Family,” on page 20.
- Updated "3.1. Power Supply Bypass Capacitors (Revision C and Revision D)" on page 23.

Revision 1.4 to Revision 1.5

- Updated "5. Ordering Guide" on page 25 to include new title note and “ Alternative Part Number (APN)” column.



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