SL28EB717

Not Recommended for New Designs

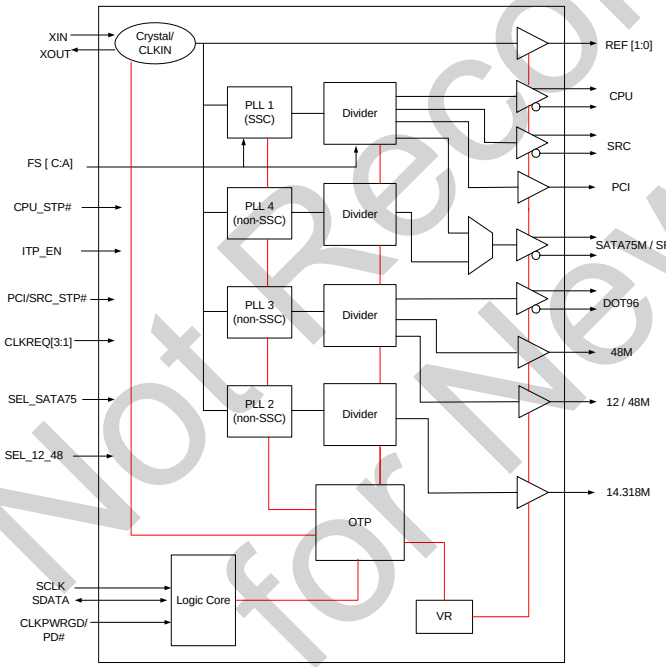
EProClock® Generator for Intel Tunnel Creek & Top Cliff

Features

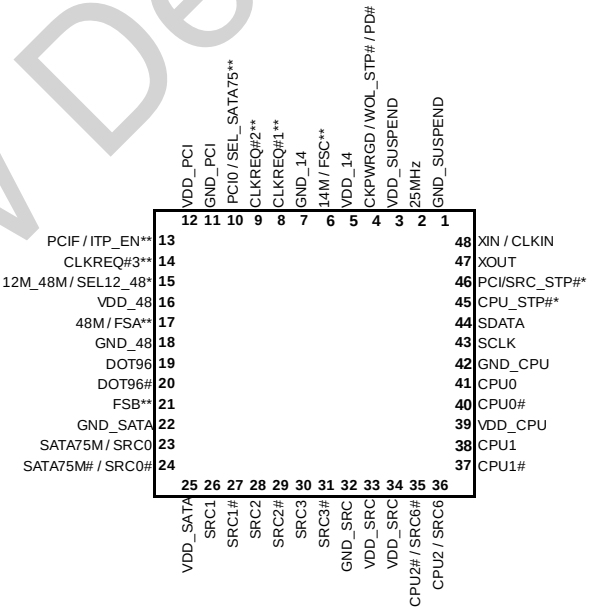
- Compliant Intel CK505 Clock spec
- Low power push-pull type differential output buffers
- Integrated resistors on differential clocks
- Wireless friendly 3-bits slew rate control on single-ended clocks.
- Differential CPU clocks with selectable frequency
- 100MHz Differential SRC clocks
- 75MHz Differential SATA clocks
- 96MHz Differential DOT clock
- 48MHz USB clock
- Selectable 12 or 48MHz output
- 14.318MHz output
- Buffered Reference Clock 25MHz
- 25MHz Crystal Input or Clock input
- Support Wake-On-LAN (WOL)
- EProClock® Programmable Technology
- I²C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 48-pin QFN package

CPU	SRC	SATA75	DOT96	48M	48M/12M	33M	25M	14.318M
x2/x3	x3/5	x0/x1	x 1	x1/2	x1	x2	x1	x1

Block Diagram



Pin Configuration



* Internal 100K-ohm pull-up resistor

** Internal 100K-ohm pull down resistor

400 West Cesar Chavez, Austin, TX 78701 1+(512) 416-8500 1+(512) 416-9669 www.silabs.com

32-QFN Pin Definitions

Pin No.	Name	Type	Description
1	GND_SUSPEND	GND	Ground for REF clock and WOL support
2	25MHz	O	25MHz reference output clock
3	VDD_SUSPEND	PWR	3.3V Power Supply for REF clock and power to support WOL
4	CKPWRGD/WOL_STP#/PD#	I	3.3V LVTTL input. This pin is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled / Asynchronous active low input pin that stops all outputs except free running 25MHz when WOL_EN = "1" (*Byte 1 bit 1*) This pin becomes a real-time active low input for asserting power down (PD#) when WOL_EN = "0" (*Byte 1 bit 1*).
5	VDD_14	PWR	3.3V Power supply for 14.318MHz clock
6	14.318M / FSC**	I/O, PD	Fixed 14.318MHz clock output/3.3V-tolerant input for CPU frequency selection *(internal 100K-ohm pull-down)* Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.
7	GND_14	GND	Ground for 14.318MHz clock
8	CLKREQ#1**	I, PD	3.3V clock request input *(internal 100K-ohm pull-down)*
9	CLKREQ#2**	I, PD	3.3V clock request input *(internal 100K-ohm pull-down)*
10	PCI0 / SEL_SATA75**	I/O, SE PD	33MHz clock output/3.3V LVTTL input to enable 75MHz SATA *(internal 100K-ohm pull-down)* 0 = SATA75/SRC0 = 100MHz, 1 = SATA75/SRC0 = 75MHz
11	GND_PCI	GND	Ground for PCI clocks
12	VDD_PCI	PWR	3.3V Power supply for PCI clocks
13	PCIF / ITP_EN**	I/O, SE, PD	33 MHz free running clock output/3.3V LVTTL input to enable SRC6 or CPU2_ITP (sampled on the CKPWRGD assertion) 0= SRC6, 1= CPU2
14	CLKREQ#3**	I, PD	3.3V clock request input *(internal 100K-ohm pull-down)*
15	12_48M / SEL12_48*	I/O, SE PU	12 MHz/ 48MHz Clock output/3.3V-tolerance input for 12MHz or 48MHz selection (Sampled at CKPWRGD assertion) *(internal 100K-ohm pull-up)* 0 = 48M, 1 = 12M
16	VDD_48	PWR	3.3V Power supply for 48MHz clocks
17	48M / FSA**	I/O PD	Fixed 48 MHz clock output/3.3V-tolerant input for CPU frequency selection *(internal 100K-ohm pull-down)* Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.
18	GND_48	GND	Ground for 48MHz clocks
19	DOT96	O, DIF	Fixed true 96MHz clock output
20	DOT96#	O, DIF	Fixed complement 96MHz clock output
21	FSB**	I, PD	3.3V-tolerant input for CPU frequency selection *(internal 100K-ohm pull-down)* Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.
22	GND_SATA	GND	Ground for SATA clock
23	SATA75M / SRC0	O, DIF	75MHz or 100MHz True differential serial reference clock
24	SATA75M# / SRC0#	O, DIF	75MHz or 100MHz Complement differential serial reference clock
25	VDD_SATA	PWR	3.3V Power supply for SATA clock
26	SRC1	O, DIF	100MHz True differential serial reference clock
27	SRC1#	O, DIF	100MHz Complement differential serial reference clock
28	SRC2	O, DIF	100MHz True differential serial reference clock
29	SRC2#	O, DIF	100MHz Complement differential serial reference clock
30	SRC3	O, DIF	100MHz True differential serial reference clock
31	SRC3#	O, DIF	100MHz Complement differential serial reference clock

Pin No.	Name	Type	Description
32	GND_SRC	GND	Ground for SRC clocks
33	VDD_SRC	PWR	3.3V Power supply for SRC clocks
34	VDD_SRC	PWR	3.3V Power supply for SRC clocks
35	SRC6# / CPU2#_ITP	O, DIF	Selectable complementary differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC6 ITP_EN = 1 @ CK_PWRGD assertion = CPU2
36	SRC6 / CPU2_ITP,	O, DIF	Selectable True differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC6 ITP_EN = 1 @ CK_PWRGD assertion = CPU2
37	CPU1#	O, DIF	Complement differential CPU clock output
38	CPU1	O, DIF	True differential CPU clock output
39	VDD_CPU	PWR	3.3V Power supply for CPU clocks
40	CPU0#	O, DIF	Complement differential CPU clock output
41	CPU0	O, DIF	True differential CPU clock output
42	GND_CPU	GND	Ground for clocks
43	SCLK	I	SMBus compatible SCLOCK
44	SDATA	I/O	SMBus compatible SDATA
45	CPU_STP#*	I, PU	3.3V-tolerant input for stopping CPU outputs *(internal 100K-ohm pull-up)*
46	PCI/SRC_STP#*	I, PU	3.3V-tolerant input for stopping PCI and SRC outputs *(internal 100K-ohm pull-up)*
47	XOUT	O	25.00MHz Crystal output, *Float XOUT if using only CLKIN (Clock input)*
48	XIN / CLKIN	I	25.00MHz Crystal input or 3.3V, 25MHz Clock Input

EProClock® Programmable Technology

EProClock® is the world's first non-volatile programmable clock. The EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

EProClock® technology can be configured through SMBus or hard coded.

Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate

Frequency Select Pin (FS)

SEL_SATA	FSC	FSB	FSA	CPU	SRC	SATA75/SRC0	PCI
0	0	0	0	100.00	100.00	100.00	33.33
0	0	0	1	100.00	100.00	100.00	33.33
0	0	1	0	83.33	100.00	100.00	33.33
0	0	1	1	83.33	100.00	100.00	33.33
0	1	0	0	133.33	100.00	100.00	33.33
0	1	0	1	133.33	100.00	100.00	33.33
0	1	1	0	166.67	100.00	100.00	33.33
0	1	1	1	166.67	100.00	100.00	33.33
1	0	0	0	100.00	100.00	75.00	33.33
1	0	0	1	100.00	100.00	75.00	33.33

Frequency Select Pin (FS)

1	0	1	0	83.33	100.00	75.00	33.33
1	0	1	1	83.33	100.00	75.00	33.33
1	1	0	0	133.33	100.00	75.00	33.33
1	1	0	1	133.33	100.00	75.00	33.33
1	1	1	0	166.67	100.00	75.00	33.33
1	1	1	1	166.67	100.00	75.00	33.33

Frequency Select Pin FS

Apply the appropriate logic levels to FS inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that VTT voltage is stable then FS input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid HIGH, all other FS, and CKPWRGD transitions are ignored except in test mode.

Wake-On-LAN (WOL) Support

When power is applied to the VDD_SUSPEND pin, the 25MHz reference clock output will be enabled under all conditions, unless the WOL_EN bit, Byte 1 bit 1, is set to “0”. When the WOL_EN bit Byte 1 bit 1, is set to “0”, the WOL_STP# pin will function as a PD# pin. By default, the WOL_EN bit is enabled and set to a “1”. The clock device will support “out-of-the-box” WOL or after a power outage by enabling the 25MHz reference clock output when the clock device powers up for the very first time with only power applied to the VDD_SUSPEND pin and all other VDD pins power have not been applied.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start

Table 2. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	Spread Enable	Enable spread for CPU/SRC/PCI outputs 0=Disable, 1= -0.5%
4	HW	SEL_SATA	See Table 1 for SATA/SRC selection.
3	0	RESERVED	RESERVED
2	HW	FSC	See Table 1 for CPU Frequency selection Table
1	HW	FSB	
0	HW	FSA	

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	DOT96_OE	Output enable for DOT96 0 = Output Disabled, 1 = Output Enabled
6	1	SATA75/SRC0_OE	Output enable for SATA75/SRC0 0 = Output Disabled, 1 = Output Enabled
5	1	CPU2/SRC6_OE	Output enable for CPU2/SRC6 0 = Output Disabled, 1 = Output Enabled
4	1	SRC2	Output enable for SRC2 0 = Output Disabled, 1 = Output Enabled
3	1	SRC1	Output enable for SRC1 0 = Output Disabled, 1 = Output Enabled
2	1	RESERVED	RESERVED
1	1	WOL_EN	Wake-On-LAN Enable bit 25MHz free running during VDD Suspend (S-states). If this bit is set to 0, the XTAL OSC will also be powered down in the Suspend States)
0	0	RESERVED	RESERVED

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	48M_OE	Output enable for 48M 0 = Output Disabled, 1 = Output Enabled
6	0	RESERVED	RESERVED
5	1	14M_OE	Output enable for 14M 0 = Output Disabled, 1 = Output Enabled
4	1	25M_OE	Output enable for 25M 0 = Output Disabled, 1 = Output Enabled
3	1	12_48M_OE	Output enable for 12_48M 0 = Output Disabled, 1 = Output Enabled
2	1	PCI0_OE	Output enable for PCI0 0 = Output Disabled, 1 = Output Enabled
1	1	PCIF_OE	Output enable for PCIF 0 = Output Disabled, 1 = Output Enabled
0	0	RESERVED	RESERVED

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	CPU1_OE	Output enable for CPU1 0 = Output Disabled, 1 = Output Enabled
6	1	CPU0_OE	Output enable for CPU0 0 = Output Disabled, 1 = Output Enabled
5	0	CLKREQ#_3	Clock request for SRC2 0=Not controlled, 1= Controlled
4	0	CLKREQ#_3	Clock request for SRC6 (does not apply to CPU clock) 0=Not controlled, 1= Controlled
3	0	CLKREQ#_2	Clock request for SRC2 0=Not controlled, 1= Controlled
2	0	CLKREQ#_2	Clock request for SATA75M/SRC0 0=Not controlled, 1= Controlled

Byte 3: Control Register 3

1	0	CLKREQ#_1	Clock request for SRC1 0=Not controlled, 1= Controlled
0	0	CLKREQ#_1	Clock request for SATA75M/SRC0 0=Not controlled, 1= Controlled

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	CPU1	CPU1 Free Run Control 0= Free Running, 1= Stoppable
5	HW	12_48M	Selectable 12_48M status 0= 48M, 1=12M
4	0	CPU2	CPU2 Free Run Control 0= Free Running, 1= Stoppable
3	HW	ITP_EN	SelectableCPUe_ITP/ SRC6 status 0= SRC6, 1=CPU2
2	0	RESERVED	RESERVED
1	0	CPU0	CPU0 Free Run Control 0= Free Running, 1= Stoppable
0	0	RESERVED	RESERVED

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	1	SATA75/SRC0	SATA75/SRC0 Free Run Control 0= Free Running, 1= Stoppable
3	0	SRC6	SRC6 Free Run Control 0= Free Running, 1= Stoppable
2	0	SRC2	SRC2 Free Run Control 0= Free Running, 1= Stoppable
1	0	SRC1	SRC1 Free Run Control 0= Free Running, 1= Stoppable
0	0	RESERVED	RESERVED

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	CPU_AMP	CPU amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV
6	1	CPU_AMP	
5	0	SRC_AMP	SRC amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV
4	1	SRC_AMP	
3	0	DOT96_AMP	DOT96 amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV
2	1	DOT96_AMP	
1	0	SATA_AMP	SATA75/SRC0 amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV
0	1	SATA_AMP	

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	0	Rev Code Bit 2	Revision Code Bit 2
5	0	Rev Code Bit 1	Revision Code Bit 1
4	1	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	BC7	Byte count register for block read operation. The default value for Byte count is 15 In order to read beyond Byte 15, the user should change the byte count limit.to or beyond the byte that is desired to be read.
6	0	BC6	
5	0	BC5	
4	0	BC4	
3	1	BC3	
2	1	BC2	
1	1	BC1	
0	1	BC0	

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	SRC3	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	SRC3	SRC3 Free Run Control 0= Free Running, 1= Stoppable
1	0	PCI0	PCI0 Free Run Control 0= Free Running, 1= Stoppable
0	1	PCIF	PCIF Free Run Control 0= Free Running, 1= Stoppable

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	1	14M_Bit2	Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111'
6	0	14M_Bit1	
5	1	14M_Bit0	
4	1	25M_Bit2	
3	0	25M_Bit1	
2	1	25M_Bit0	
1	1	12_48M_Bit2	
0	1	12_48M_Bit0	

Mode	Bit2	Bit1	Bit0	Buffer Strength
	0	0	0	Strong
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Default	1	0	1	
	1	1	0	
Wireless Friendly	1	1	1	Weak

Byte 12: Control Register 12

Bit	@Pup	Name	Description
7	1	48M_Bit2	Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111'
6	0	48M_Bit1	
5	1	48M_Bit0	
4	1	PCI0_Bit2	
3	0	PCI0_Bit1	
2	1	PCI0_Bit0	
1	0	RESERVED	
0	0	12_48M_Bit1	

Mode	Bit2	Bit1	Bit0	Buffer Strength
	0	0	0	Strong
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Default	1	0	1	
	1	1	0	
Wireless Friendly	1	1	1	Weak

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	1	PCIF_Bit2	Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111'
6	0	PCIF_Bit1	
5	1	PCIF_Bit0	
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	Wireless Friendly mode	Wireless Friendly Mode 0 = Disabled, Default all single-ended clocks slew rate config bits to '101' 1 = Enabled, Default all single-ended clocks slew rate config bits to '111'

Mode	Bit2	Bit1	Bit0	Buffer Strength
	0	0	0	Strong
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Default	1	0	1	
	1	1	0	
Wireless Friendly	1	1	1	Weak

Byte 14: Control Register 14

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	OTP_4	OTP_ID Idenification for programmed device
3	0	OTP_3	
2	0	OTP_2	
1	0	OTP_1	
0	0	OTP_0	

Table 4. Output Driver Status during CPU_STP# & PCIS_STP#

		CPU_STP# Asserted	PCI_STP# Asserted	CLKREQ# Asserted	SMBus OE Disabled
Single-ended Clocks	Stoppable	Running	Driven Low	Running	Driven low
	Non stoppable	Running	Running	Running	
Differential Clocks	Stoppable	Clock driven high	Clock driven high	Clock driven low	Clock driven low
		Clock# driven low	Clock# driven low	Clock# driven low	
	Non stoppable	Running	Running	Running	

Table 5. Output Driver Status

	All Single-ended Clocks		All Differential Clocks	
	w/o Strap	w/ Strap	Clock	Clock#
PD# = 0 (Power down)	Low	Hi-z	Low	Low

PD# (Power down) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD# (Power down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held LOW. When PD mode is desired as the initial power on state, PD must be asserted HIGH in less than 10 μs after asserting CKPWRGD.

PD# Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from power down are driven high in less than 300 μs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. *Figure 2* is an example showing the relationship of clocks coming up.

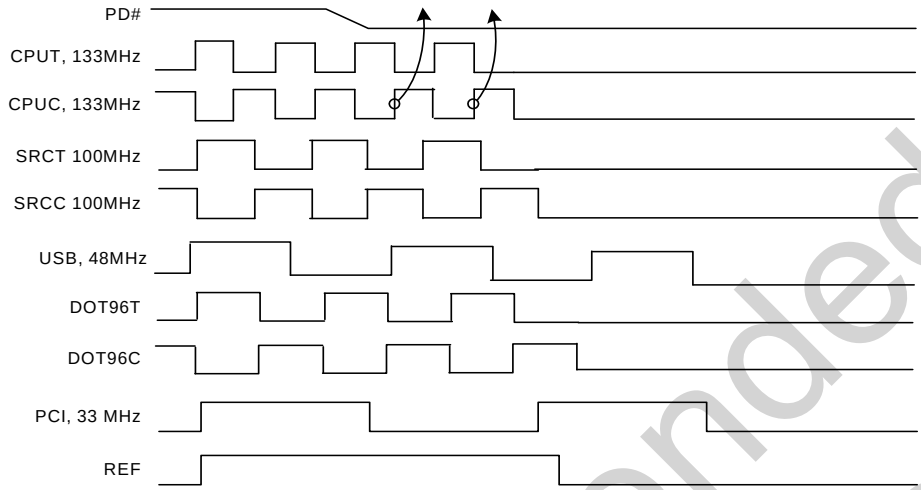


Figure 1. Power down Assertion Timing Waveform

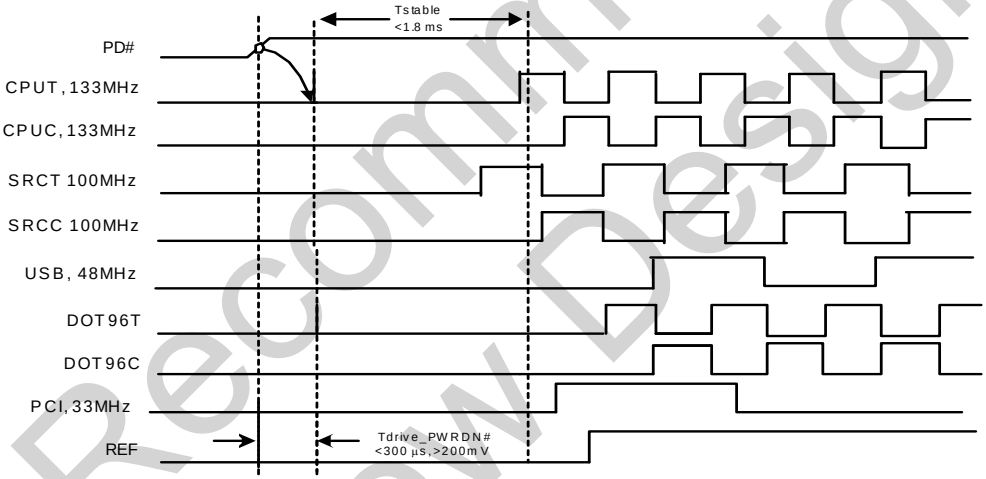


Figure 2. Power down Deassertion Timing Waveform

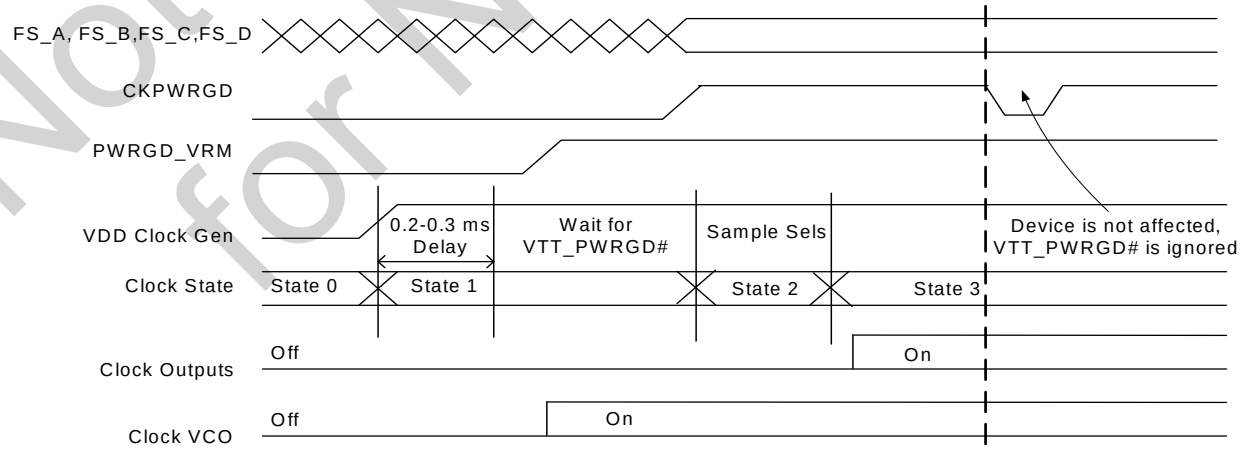


Figure 3. CKPWRGD Timing Diagram

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable are stopped within two to six CPU clock periods after sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

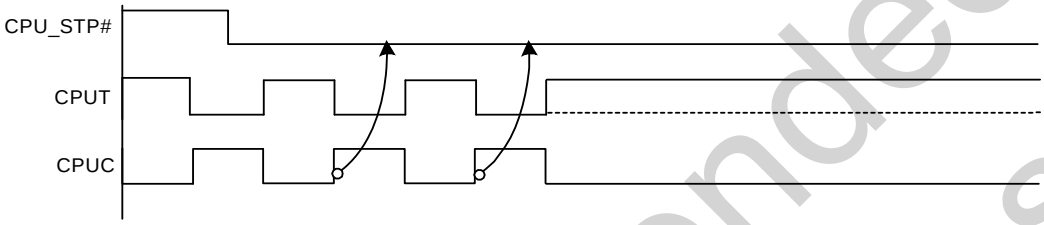


Figure 4. CPU_STP# Assertion Waveform

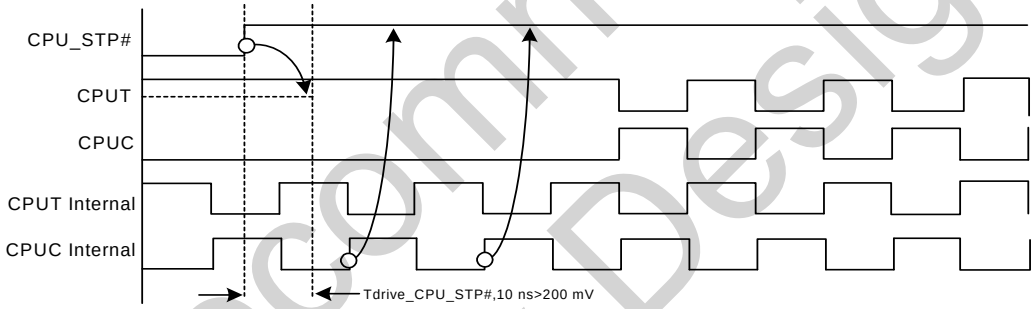


Figure 5. CPU_STP# Deassertion Waveform

PCI/SRC_STP# Assertion

The PCI/SRC_STP# signal is an active LOW input used for synchronously stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI/SRC_STP# going LOW is 10 ns (t_{SU}). (See *Figure 6*.) The PCIF and SRC clocks are affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running. For SRC clocks assertion description, please refer to CPU_STP# description.

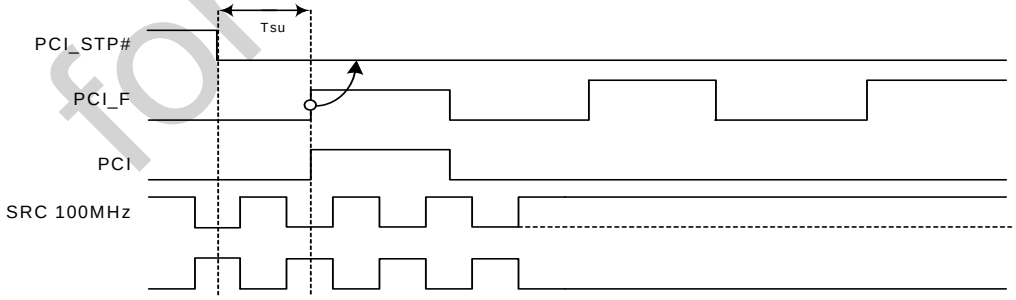


Figure 6. PCI_STP# Assertion Waveform

PCI/SRC_STP# Deassertion

The deassertion of the PCI/SRC_STP# signal causes all PCI and stoppable PCIF to resume running in a synchronous manner within two PCI clock periods, after PCI/SRC_STP# transitions to a HIGH level. Simlarly, PCI/SRC_STP# deassertion will cause stoppable SRC clocks to resume running. For SRC clocks deassertion description, please refer to CPU_STP# description.

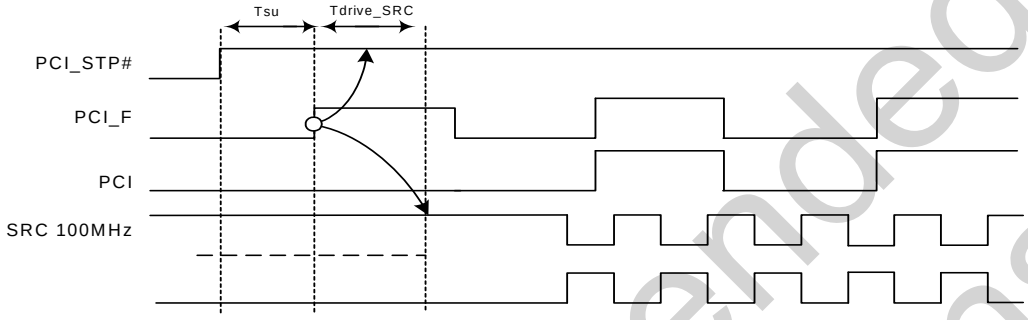


Figure 7. PCI_STP# Deassertion Waveform

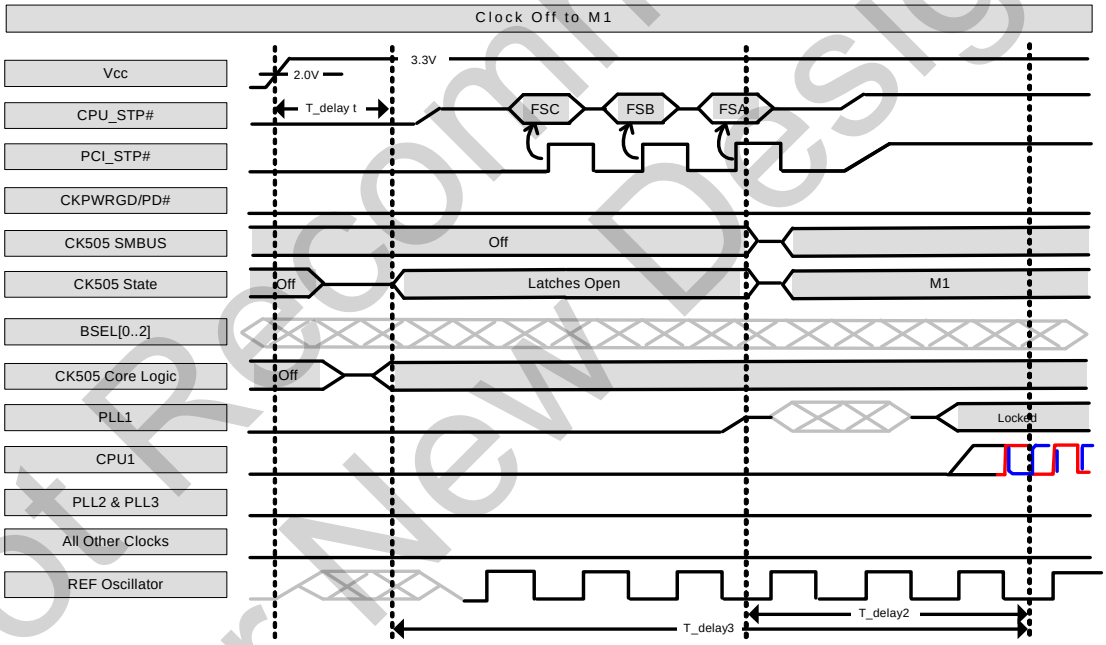


Figure 8. BSEL Serial Latching

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD\_3.3V}$	Main Supply Voltage	Functional	–	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	–40	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22 - A114)	2000	–	V
UL-94	Flammability Rating	UL (Class)	V–0		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage (SE)		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage (SE)		V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IH_FS}	FS Input High Voltage		0.7	VDD+0.3	V
V_{IL_FS}	FS Input Low Voltage		V_{SS} – 0.3	0.35	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
IDD_PD	Power Down Current		–	1	mA
$I_{DD\_3.3V}$	Dynamic Supply Current	All outputs enabled. SE clocks with 5” traces. Differential clocks with 5” traces. Loading per CK505 spec.	–	100	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
L_{ACC}	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
Clock Input					
T_{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T_R/T_F	CLKIN Rise and Fall Times	Measured between $0.2V_{DD}$ and $0.8V_{DD}$	0.5	4.0	V/ns
T_{CCJ}	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T_{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V_{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
V_{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
I_{IH}	Input HighCurrent	XIN / CLKIN pin, VIN = VDD	–	35	uA
I_{IL}	Input LowCurrent	XIN / CLKIN pin, 0 < VIN <0.8	–35	–	uA
CPU at 0.7V					
T_{DC}	CPU Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	83.33 MHz CPU Period	Measured at 0V differential at 0.1s	11.99880	12.00120	ns
$T_{PERIODSS}$	83.33 MHz CPU Period, SSC	Measured at 0V differential at 0.1s	12.028872	12.03128	ns
$T_{PERIODAbs}$	83.33 MHz CPU Absolute Period	Measured at 0V differential at 1clock	11.18969	12.16344	ns
$T_{PERIODSSAbs}$	83.33 MHz CPU Absolute Period, SSC	Measured at 0V differential at 1 clock	11.89687	12.16344	ns
T_{PERIOD}	100 MHz CPU Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz CPU Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz CPU Absolute Period	Measured at 0V differential at 1clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz CPU Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns
T_{PERIOD}	133 MHz CPU Period	Measured at 0V differential at 0.1s	7.49925	7.50075	ns
$T_{PERIODSS}$	133 MHz CPU Period, SSC	Measured at 0V differential at 0.1s	7.51804	7.51955	ns
$T_{PERIODAbs}$	133 MHz CPU Absolute period	Measured at 0V differential at 1 clock	7.41425	7.58575	ns
$T_{PERIODSSAbs}$	133 MHz CPU Absolute period, SSC	Measured at 0V differential at1 clock	7.41430	7.62340	ns
T_{PERIOD}	166 MHz CPU Period	Measured at 0V differential at 0.1s	5.99940	6.00060	ns
$T_{PERIODSS}$	166 MHz CPU Period, SSC	Measured at 0V differential at 0.1s	6.01444	6.01564	ns
$T_{PERIODAbs}$	166 MHz CPU Absolute period	Measured at 0V differential at 1 clock	5.91440	6.08560	ns
$T_{PERIODSSAbs}$	166 MHz CPU Absolute period, SSC	Measured at 0V differential at 1 clock	5.91444	6.11572	ns
T_{CCJ}	CPU Cycle to Cycle Jitter	Measured at 0V differential	–	85	ps
$T_{CCJ\ (CPU2)}$	CPU Cycle to Cycle Jitter for CPU 2	Measured at 0V differential	–	125	ps
Skew	CPU0 to CPU1 skew	Measured at 0V differential	–	100	ps
L_{ACC}	Long-term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	CPU Rising/Falling Slew rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
SRC at 0.7V					
T_{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{SKEW(window)}$	Any SRC Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	–	3.0	ns
T_{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	SRC Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
DOT96 at 0.7V					
T_{DC}	DOT96 Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	DOT96 Period	Measured at 0V differential at 0.1s	10.4156	10.4177	ns
$T_{PERIODAbs}$	DOT96 Absolute Period	Measured at 0V differential at 0.1s	10.1656	10.6677	ns
T_{CCJ}	DOT96 Cycle to Cycle Jitter	Measured at 0V differential at 1 clock	–	250	ps
L_{ACC}	DOT96 Long Term Accuracy	Measured at 0V differential at 1 clock	–	100	ppm
T_R / T_F	DOT96 Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
SATA75M at 0.7V					
T_{DC}	SATA75M Duty Cycle	Measured at 0V differential	45	55	%
T_{CCJ}	SATA75M Cycle to Cycle Jitter	Measured at 0V differential at 1 clock	–	125	ps
L_{ACC}	SATA75M Long Term Accuracy	Measured at 0V differential at 1 clock	–	100	ppm
T_R / T_F	SATA75M Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
PCI/PCIF at 3.3V					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99700	30.00300	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	30.08421	30.23459	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49700	30.50300	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	29.56617	30.58421	ns
T_{HIGH}	Spread Enabled PCIF and PCI high time	Measurement at 2V	12.27095	16.27995	ns
T_{LOW}	Spread Enabled PCIF and PCI low time	Measurement at 0.8V	11.87095	16.07995	ns
T_{HIGH}	Spread Disabled PCIF and PCI high time	Measurement at 2.V	12.27365	16.27665	ns
T_{LOW}	Spread Disabled PCIF and PCI low time	Measurement at 0.8V	11.87365	16.07665	ns
T_R / T_F	PCIF/PCI Rising/Falling Slew Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	1000	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	300	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measurement at 1.5V	–	100	ppm

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
48M, 12_48M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	48MHz Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	48MHz Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	48MHz High time	Measurement at 2V	8.216563	11.15198	ns
T_{LOW}	48MHz Low time	Measurement at 0.8V	7.816563	10.95198	ns
T_R / T_F (48M)	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_R / T_F (12_48M)	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	300	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	100	ppm
25M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	39.996	40.004	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	39.32360	40.67640	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	300	ps
L_{ACC}	Long Term Accuracy	Measured at 1.5V	–	100	ppm
14.318M, at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	69.82033	69.86224	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	68.83429	70.84826	ns
T_{HIGH}	High time	Measurement at 2V	29.97543	38.46654	ns
T_{LOW}	Low time	Measurement at 0.8V	29.57543	38.26654	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	100	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up

For Single Ended Clocks

The following diagram shows the test load configurations for the single-ended output signals.

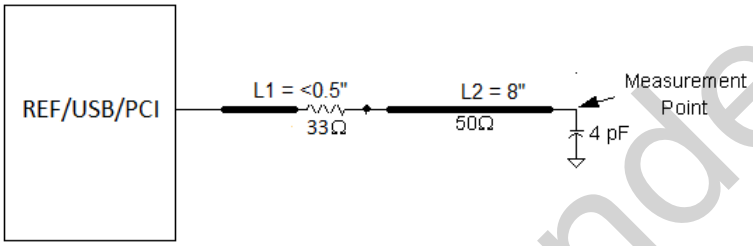


Figure 9. Single-ended clocks Single Load Configuration

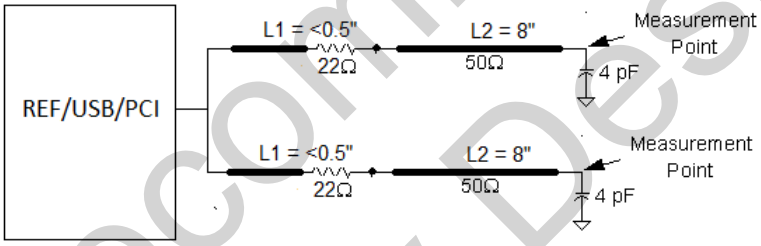


Figure 10. Single-ended clocks Double Load Configuration

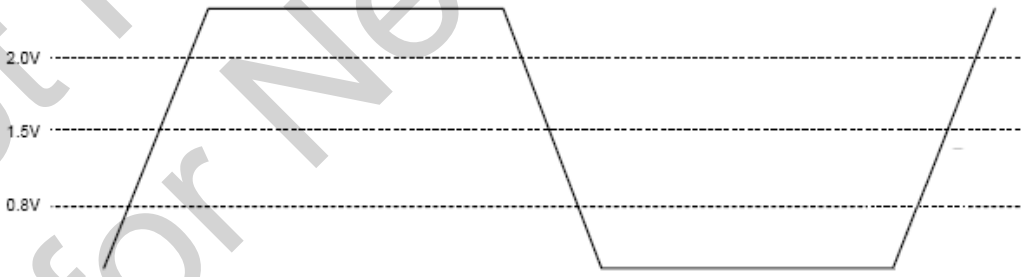


Figure 11. Single-ended Output Signals (for AC Parameters Measurement)

For Differential Clock Signals

This diagram shows the test load configuration for the differential clock signals

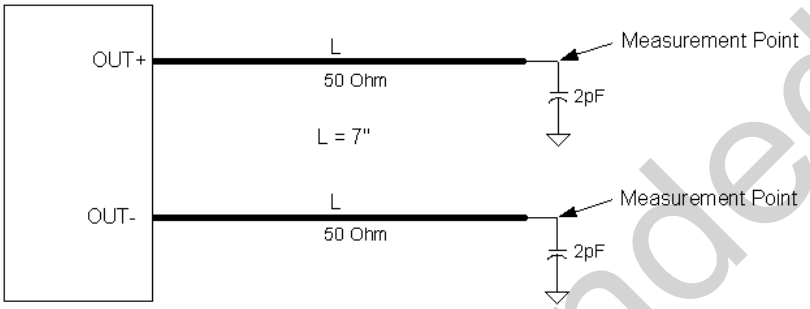


Figure 12. 0.7V Differential Load Configuration

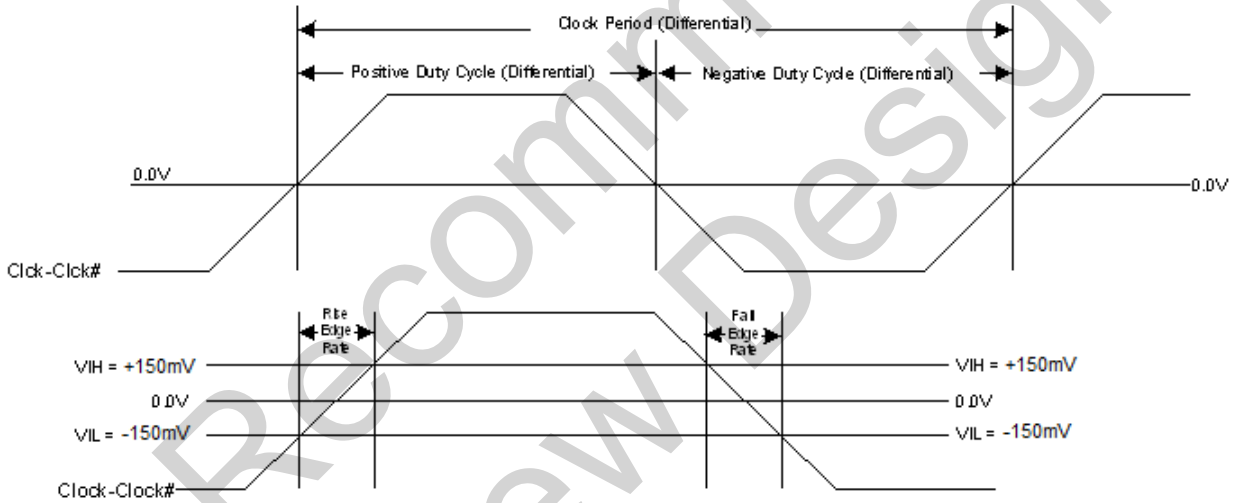


Figure 13. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

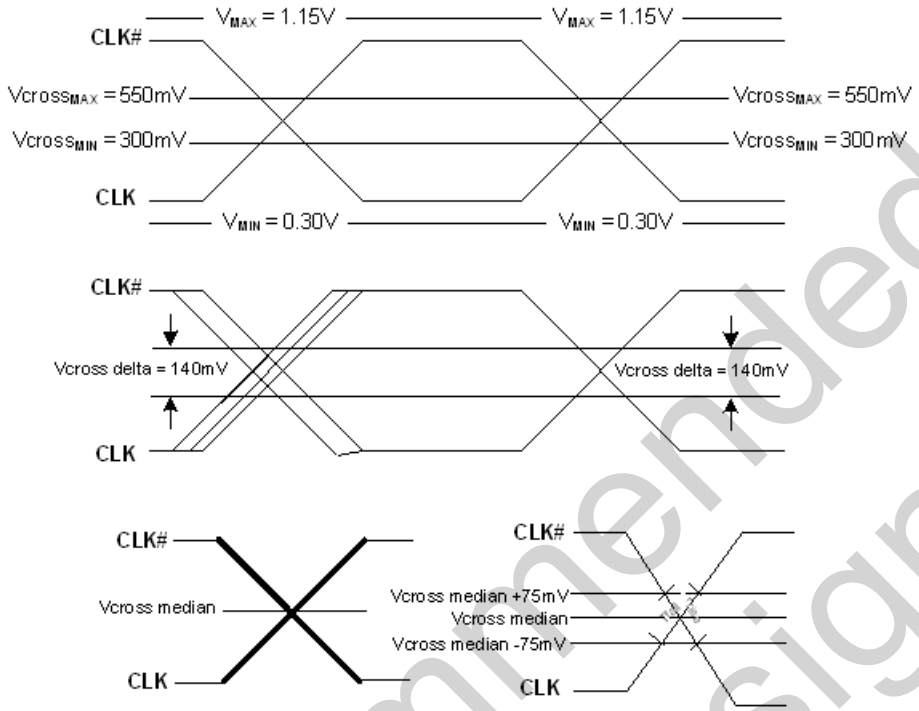


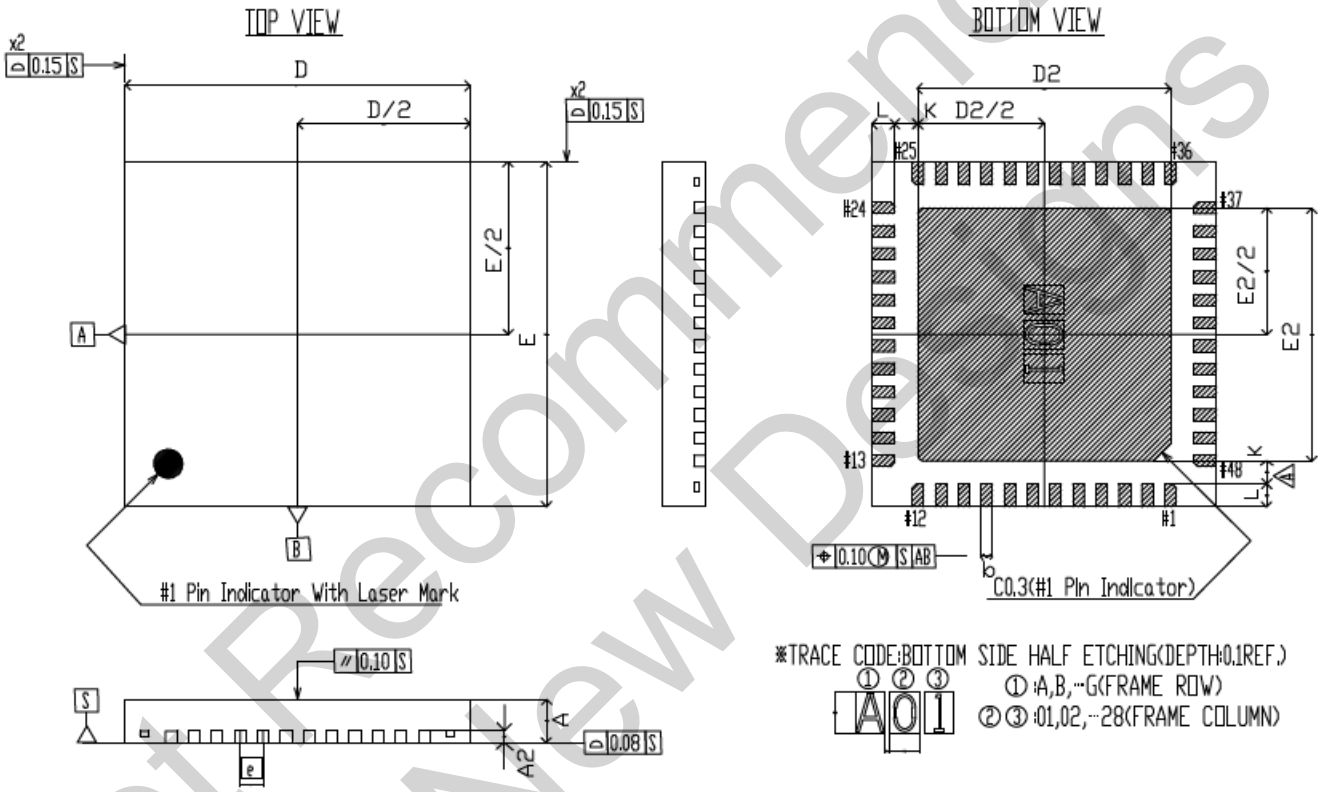
Figure 14. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
SL28EB717ALI	48-pin QFN	Industrial, -40° to 85°C
SL28EB717ALIT	48-pin QFN – Tape and Reel	Industrial, -40° to 85°C

Package Diagrams

48-Lead QFN 6 x 6mm



※TRACE CODE:BOTTOM SIDE HALF ETCHING(DEPTH:0.1REF.)
① ② ③ A01
①:A,B,···G(FRAME ROW)
②③:01,02,···28(FRAME COLUMN)

SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	4.25	4.40	4.55
E	5.90	6.00	6.10
E2	4.25	4.40	4.55
e		0.40 BSC.	
k	0.36	—	—
L	0.30	0.40	0.50

NOTES)
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED
3.THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8㎛.
4.PROTRUSIONS AT PKG.OUTLINE SHALL NOT EXCEED 0.10.

Document History Page

Document Title: SL28EB717 PC EProClock® Generator for Intel Tunnel Creek & Top Cliff DOC#: SP-AP-0755 (Rev. AA)				
REV.	**ECR#**	**Issue Date**	**Orig. of Change**	**Description of Change**
0.3		11/30/09	JMA	Initial Release
0.4		12/15/09	JMA	Updated Table in Feature section to add PCI clocks Updated pin naming in pin diagram Added PCI_STP# state in Table 4 Updated Figure 3 to show trace length Edited ordering information
AA	1431	01/04/09	JMA	1. Added WOL Support and description 2. Changed VDD_REF pin to VDD_SUSPEND pin 3. Changed PD# pin to WOL_STP# pin 4. Updated Table 4 to show CLKREQ# status 5. Showed Byte 8bit [7:0] to be byte count 6. Added note to Byte 3 bit 4 to indicate bit will not affect CPU clock 7. Added SRC0 to Byte 3 [bit 2 & bit 0] to indicate bit will disable SATA75 and SRC0 8.Updated 12M_48M slew rate to be 2V/ns max 9. Updated Test condition circuit for single-ended clocks from triple loads to double load 10. Updated all differential clocks to be 8V/ns max instead of 4V/ns max
AA	1638	06/23/10	JMA	1. Added CLKIN feature 2. Added Period Spec for CPU, SRC, and DOT96 3. Added Cycle-to-cycle jitter spec for CPU2/SRC5 (ITP clock) 4. Removed REF wording from 14.318MHz 5. Reduced IDD to 130mA from 200mA 6. Reduced PCI clocks cycle-to-cycle jitter to 300ps from 500ps 7. Reduced 25MHzclock cycle-to-cycle jitter to 300ps from 500ps 8. Reduced 48/12MHz clocks cycle-to-cycle jitter to 300ps from 350ps 9. Reduced 14.318MHz clock cycle-to-cycle jitter to 500ps from 1000ps 10. Reduced SATA75 clock cycle-to-cycle jitter to 125ps from 250ps 11. Removed skew for 14MHz 12. Updated CPU2 Cycle-to-cycle jitter to be 125ps from 85ps 13. Updated Package information 14. Added PD# label to pin configuration on page 1 15. Updated MIL-STD to JEDEC 16. Removed Prliminary wording 17. Added period spec for 83.33, 133, and 166MHz 18. Updated block diagram 19. Updated MSL Level from 1 to 2
AA		11/10/10	JMA	Updated Rev. ID Byte 7
AA		11/17/10	TRP	1. Updated revision to AA 2. Renamed byte 12 as ‘Control Register’ from ‘Byte count’

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