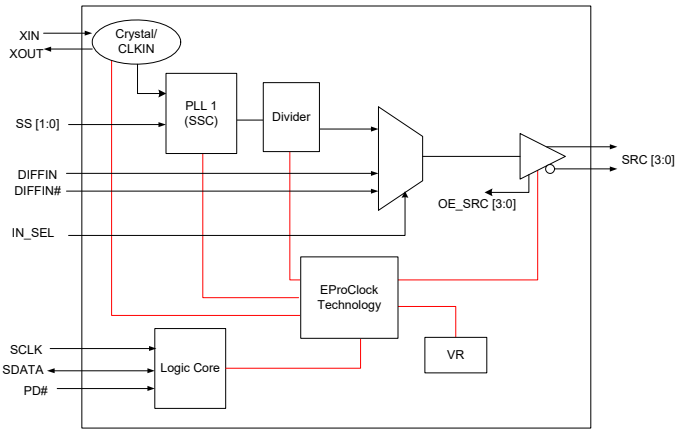
PCI-Express Gen 2 & Gen 3 Clock Generator & Fan-out Buffer with EProClock® Technology

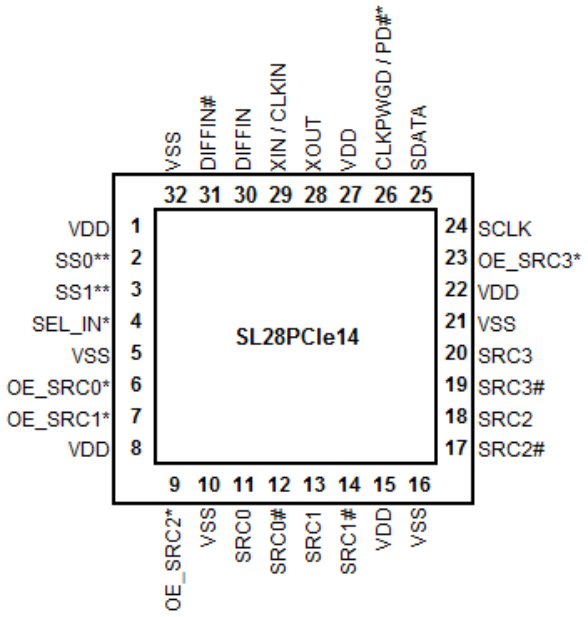
Features

- PCI-Express Gen 2 & Gen 3 Compliant
- Low power push-pull type differential output buffers
- Integrated resistors on differential clocks
- HW Selectable Buffered Input or crystal synthesizer mode
- Dedicated Output Enable pin for all clocks
- HW Selectable Frequency and Spread Control
- Four PCI-Express Gen2 & Gen 3 Clocks
- 25MHz Crystal Input or Clock input
- EProClock® Programmable Technology
- I²C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 32-pin QFN package

Block Diagram



Pin Configuration



* Internal 100K-ohm pull-upresistor

** Internal 100K-ohm pull-down resistor

32-QFN Pin Definitions

Pin No.	Name	Type	Description
1	VDD	PWR	3.3V Power Supply
2	SS0**	I, PD	Freqency/Spread Control. Default SS[1:0] =00. *(internal 100K-ohm pull-down)* SS1 / SS0 / Frequency / Spread / Note 0 / 0 / 100M / OFF / Default 0 / 1 / 100M / -0.5% / 1 / 0 / 100M / -/+0.25 / 1 / 1 / 100M / -0.75% / MID / 0 / 125MHz / OFF / MID / 1 / 200MHz / OFF /
3	SS1**	I, PD	
4	IN_SEL*	I, PU	3.3V input to select between crystal input or external differential buffer input mode. 0 = Synthesizer mode, 1=Fan-out Buffer mode *(internal 100K-ohm pull-up; switching is not glitchless)*
5	VSS	GND	Ground
6	OE_SRC0*	I,PU	3.3V input to enabled SRC0 clock. *(internal 100K-ohm pull-up)*
7	OE_SRC1*	I,PU	3.3V input to enabled SRC1 clock. *(internal 100K-ohm pull-up)*
8	VDD	PWR	3.3V Power Supply
9	OE_SRC2*	I,PU	3.3V input to enabled SRC2 clock. *(internal 100K-ohm pull-up)*
10	VSS	GND	Ground
11	SRC0	O, DIF	100MHz True differential serial reference clock
12	SRC0#	O, DIF	100MHz Complement differential serial reference clock
13	SRC1	O, DIF	100MHz True differential serial reference clock
14	SRC1#	O, DIF	100MHz Complement differential serial reference clock
15	VDD	PWR	3.3V Power Supply
16	VSS	GND	Ground
17	SRC2#	O, DIF	100MHz Complement differential serial reference clock
18	SRC2	O, DIF	100MHz True differential serial reference clock
19	SRC3#	O, DIF	100MHz Complement differential serial reference clock
20	SRC3	O, DIF	100MHz True differential serial reference clock
21	VSS	GND	Ground
22	VDD	PWR	3.3V Power Supply
23	OE_SRC3*	I,PU	3.3V input to enabled SRC3 clock. *(internal 100K-ohm pull-up)*
24	SCLK	I	SMBus compatible SCLOCK
25	SDATA	I/O	SMBus compatible SDATA
26	CKPWRGD/PD#*	I,PU	3.3V LVTTL input. This pin is a level sensitive strobe used to latch the SS[1:0]. After CKPWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW)
27	VDD	PWR	3.3V Power Supply
28	XOUT	O	25.00MHz Crystal output, *Float XOUT if using only CLKIN (Clock input)*
29	XIN / CLKIN	I	25.00MHz Crystal input or 3.3V, 25MHz Clock Input
30	DIFFIN	I	True differential serial reference clock input
31	DIFFIN#	I	Complement differential serial reference clock
32	VSS	GND	Ground

EProClock® Programmable Technology

EProClock® is the world's first non-volatile programmable clock. The EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

EProClock® technology can be configured through SMBus or hard coded.

Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate

Frequency/Spread Select Pin (SS[1:0])

SS1	SS0	Frequency (MHz)	Spread (%)	Note
0	0	100.00	OFF	Default Value for SS [1:0] =00
0	1	100.00	- 0.5	
1	0	100.00	+/- 0.25	
1	1	100.00	- 0.75	
MID	0	125	OFF	
MID	1	200	OFF	

Frequency/Spread Select Pin SS[1:0]

Apply the appropriate logic levels to SS [1:0] inputs before CKPWRGD assertion to achieve clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that the voltage is stable then SS [1:0] input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid HIGH, all other SS[1:0], and CKPWRGD transitions are ignored.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits

Table 2. Block Read and Block Write Protocol (Continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Type	Name	Description
7	0	R/W	RESERVED	RESERVED
6	0	R/W	RESERVED	RESERVED
5	0	R/W	RESERVED	RESERVED
4	0	R/W	RESERVED	RESERVED
3	0	R/W	RESERVED	RESERVED
2	0	R/W	RESERVED	RESERVED
1	0	R/W	RESERVED	RESERVED
0	0	R/W	RESERVED	RESERVED

Byte 1: Control Register 1

Bit	@Pup	Type	Name	Description
7	0	R/W	RESERVED	RESERVED
6	0	R/W	RESERVED	RESERVED
5	0	R/W	RESERVED	RESERVED
4	0	R/W	RESERVED	RESERVED
3	0	R/W	RESERVED	RESERVED
2	1	R/W	SRC0_OE	Output enable for SRC0 0 = Output Disabled, 1 = Output Enabled
1	0	R/W	RESERVED	RESERVED
0	1	R/W	SRC1_OE	Output enable for SRC1 0 = Output Disabled, 1 = Output Enabled

Byte 2: Control Register 2

Bit	@Pup	Type	Name	Description
7	1	R/W	SRC2_OE	Output enable for SRC2 0 = Output Disabled, 1 = Output Enabled
6	1	R/W	SRC3_OE	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
5	0	R/W	RESERVED	RESERVED
4	0	R/W	RESERVED	RESERVED
3	0	R/W	RESERVED	RESERVED
2	0	R/W	RESERVED	RESERVED
1	0	R/W	RESERVED	RESERVED
0	0	R/W	RESERVED	RESERVED

Byte 3: Control Register 3

Bit	@Pup	Type	Name	Description
7	0	R	Rev Code Bit 3	Revision Code Bit 3
6	0	R	Rev Code Bit 2	Revision Code Bit 2
5	0	R	Rev Code Bit 1	Revision Code Bit 1
4	0	R	Rev Code Bit 0	Revision Code Bit 0
3	1	R	Vendor ID bit 3	Vendor ID Bit 3
2	0	R	Vendor ID bit 2	Vendor ID Bit 2
1	0	R	Vendor ID bit 1	Vendor ID Bit 1
0	0	R	Vendor ID bit 0	Vendor ID Bit 0

Byte 4: Control Register 4

Bit	@Pup	Type	Name	Description
7	0	R/W	BC7	Byte count register for block read operation. The default value for Byte count is 7. In order to read beyond Byte 7, the user should change the byte count limit.to or beyond the byte that is desired to be read.
6	0	R/W	BC6	
5	0	R/W	BC5	
4	0	R/W	BC4	
3	0	R/W	BC3	
2	1	R/W	BC2	
1	1	R/W	BC1	
0	1	R/W	BC0	

Byte 5: Control Register 5

Bit	@Pup	Type	Name	Description
7	1	R/W	RESERVED	RESERVED
6	1	R/W	SRC_AMP2	SRC amplitude adjustment 000= 300mV, 001=400mV, 010=500mV, 011= 600mV 100= 700mV, 101=800mV, 110=900mV, 111= 1000mV
5	0	R/W	SRC_AMP1	
4	1	R/W	SRC_AMP0	
3	1	R/W	RESERVED	RESERVED
2	0	R/W	RESERVED	RESERVED
1	0	R/W	RESERVED	RESERVED
0	0	R/W	RESERVED	RESERVED

OE[3:0] Assertion

All differential outputs that were stopped are to resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2 and 6 clocks of the internal reference clock with all differential outputs resuming simultaneously. All stopped differential outputs must be driven HIGH within 10 ns of OE deassertion to a voltage greater than 200 mV.

OE[3:0] Deassertion

The impact of deasserting the OE pins is that all SRC outputs that are set in the control registers to stoppable via deassertion of OE are to be stopped after their next transition. The final state of all stopped SRC clocks is Low/Low.

PD# (Power down) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD# (Power down) Assertion

When PD# has been sampled LOW by the internal reference clock all differential clocks will be stopped in a glitch-free mannter to the LOW-LOW state within their next two consecutive rising edges.

PD# Deassertion

The power up latency will be less than 2ms for crystal input reference and less than 8ms for differential input reference clock. This is the delay from the power supply reaching the minimum value specified in the datasheet, until the time that the part is ready to sample any latched inputs on the first rising edge of CLKPWRGD.

After the first rising edge on the CKPWRGD this pin becmoes PD#. After a valid rising edge on CKPWRGD/PD# pin, a time of not more than 1.8ms is allowed for the clock device's internal PLL's to power up and lock. After this time, all outputs are enabled in a glitch-free manner within a few clock cycles of each clock.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD\_3.3V}$	Main Supply Voltage	Functional	–	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Industrial Temperature, Operating Ambient	Functional	–40	85	°C
T_A	Commercial Temperature, Operating Ambient	Functional	0	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22 - A114)	2000	–	V
UL-94	Flammability Rating	UL (Class)	V–0		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage (SE)		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage (SE)		V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
$V_{IH\_SS[1:0]\_HIGH}$	SS Input High Voltage		0.7	VDD+0.3	V
$V_{IH\_SS[1:0]\_MID}$	SS Input MIDVoltage		0.7	1.5	V
$V_{IL\_SS[1:0]\_LOW}$	SS Input Low Voltage		V_{SS} – 0.3	0.35	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, 0 < V_{IN} < V_{DD}	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, 0 < V_{IN} < V_{DD}	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
$IDD_{\_PD}$	Power Down Current		–	1	mA
$I_{DD\_3.3V}$	Dynamic Supply Current in synthesizer mode	Differential clocks with 5” traces and 2pF load, frequency at 100MHz.	–	50	mA
$I_{DD\_3.3V}$	Dynamic Supply Current in fanout mode	Differential clocks with 5” traces and 2pF load, frequency at 100MHz.	–	30	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
L_{ACC}	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
Clock Input					
T_{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T_R/T_F	CLKIN Rise and Fall Times	Measured between $0.2V_{DD}$ and $0.8V_{DD}$	0.5	4.0	V/ns
T_{CCJ}	CLKIN Cycle to Cycle Jitter (Sythesizer)	Measured at VDD/2	–	250	ps
T_{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V_{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
V_{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
I_{IH}	Input HighCurrent	XIN / CLKIN pin, VIN = VDD	–	35	uA
I_{IL}	Input LowCurrent	XIN / CLKIN pin, 0 < VIN <0.8	–35	–	uA
SRC at 0.7V					
T_{DC}	Duty Cycle	Measured at 0V differential	45	55	%
RMS_{GEN1}	Output PCIe* Gen1 REFCLK phase jitter	BER = 1E-12 (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)	0	108	ps
RMS_{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.0	ps
RMS_{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.1	ps
RMS_{GEN3}	Output phase jitter impact – PCIe* Gen3	Includes PLL BW 2 - 4 MHz, CDR = 10MHz)	0	1.0	ps
T_{CCJ}	Cycle to Cycle Jitter	Measured at 0V differential	–	85	ps
T_{CCJ}	Additive Cycle to Cycle Jitter	In buffer mode. Measured at 0V differential	–	50	ps
L_{ACC}	Long-term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	Rising/Falling Slew rate	Measured differentially from ±150 mV	2.5	8	V/ns
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up

For Differential Clock Signals

This diagram shows the test load configuration for the differential clock signals

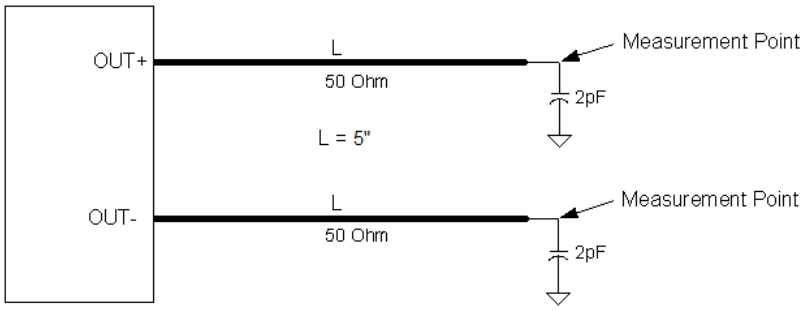


Figure 1. 0.7V Differential Load Configuration

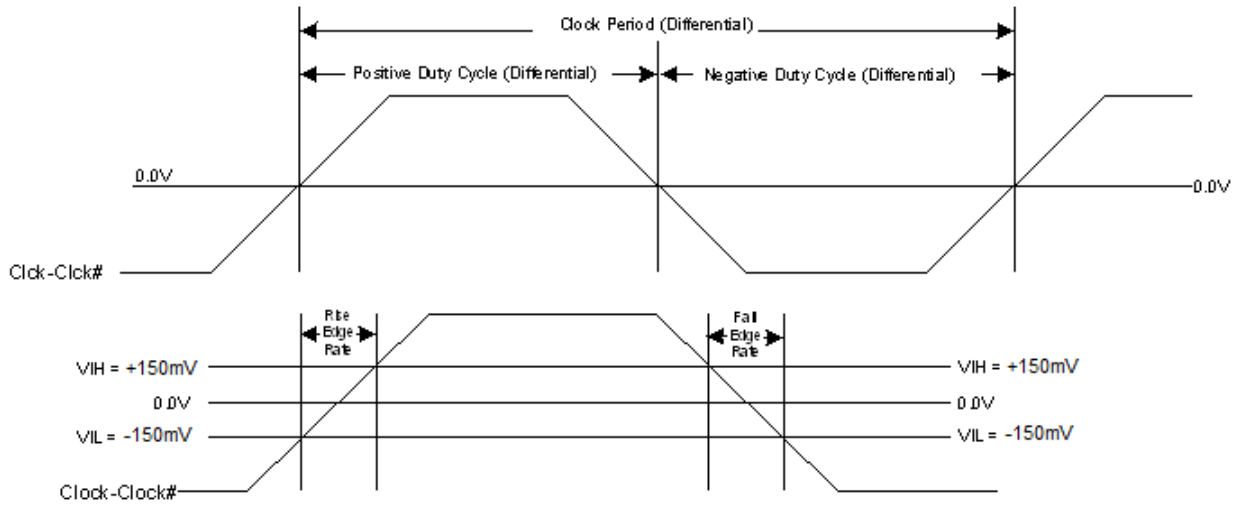


Figure 2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

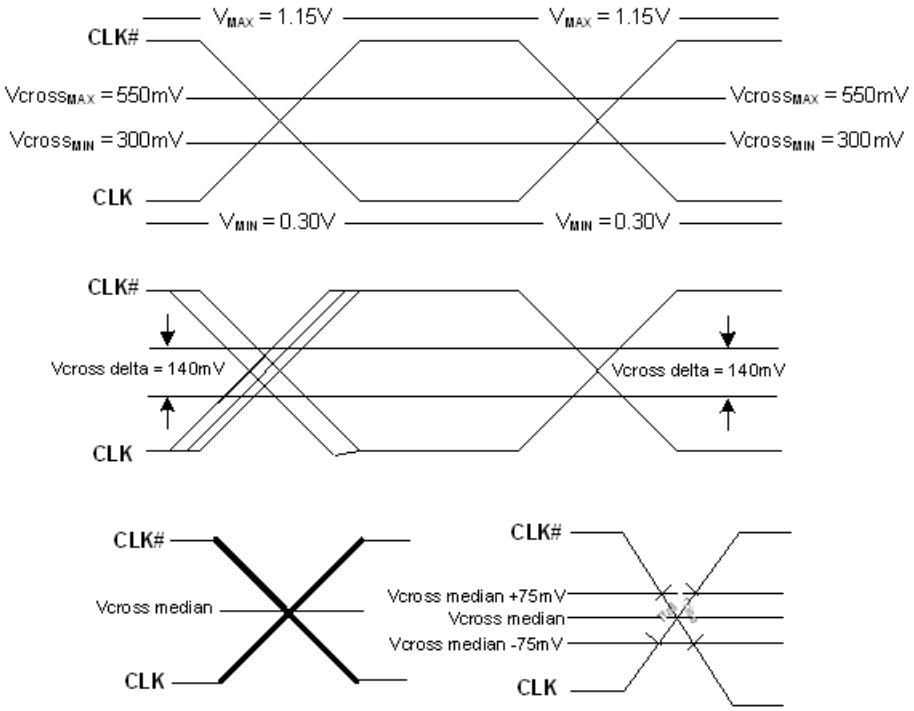


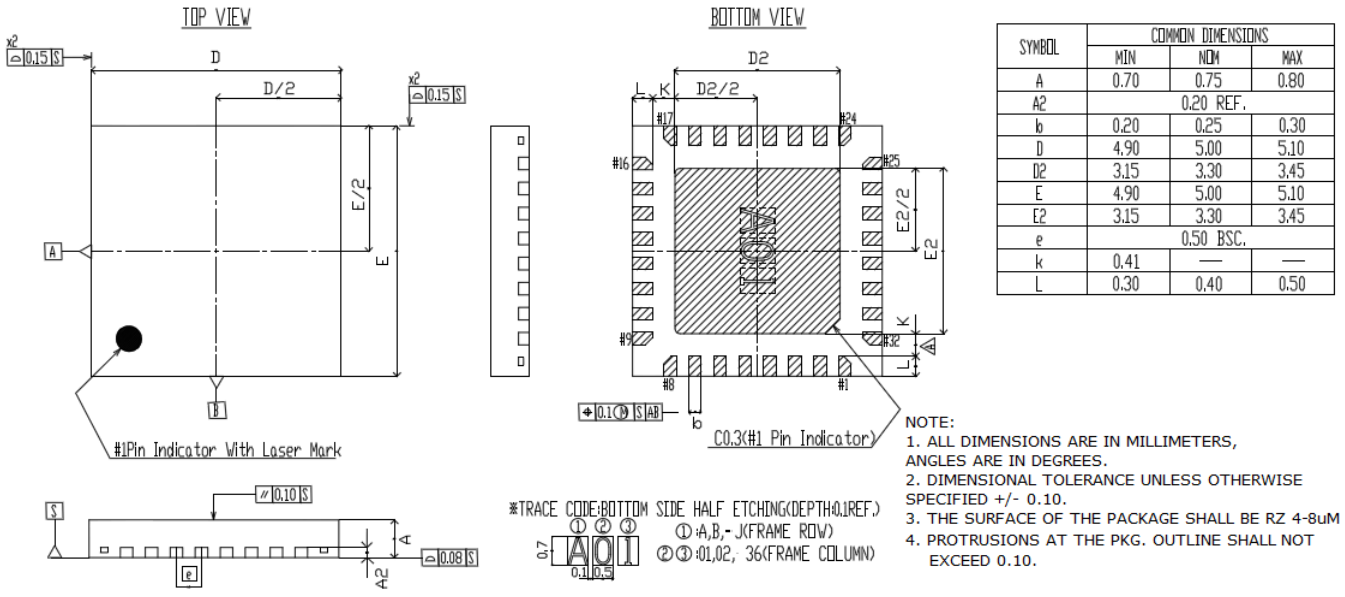
Figure 3. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
SL28PCIe14ALC	32-pin QFN	Commercial, 0° to 85°C
SL28PCIe14ALCT	32-pin QFN – Tape and Reel	Commercial, 0° to 85°C
SL28PCIe14ALI	32-pin QFN	Industrial, -40° to 85°C
SL28PCIe14ALIT	32-pin QFN – Tape and Reel	Industrial, -40° to 85°C

Package Diagrams

32-Lead QFN 5x 5mm



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.30	3.45
E	4.90	5.00	5.10
E2	3.15	3.30	3.45
e		0.50 BSC.	
k	0.41	—	—
L	0.30	0.40	0.50

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
2. DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED +/- 0.10.
3. THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8uM
4. PROTRUSIONS AT THE PKG. OUTLINE SHALL NOT EXCEED 0.10.

Document History Page

Document Title: SL28PCIe14 PC Low-Power Clock Generator for Intel® Ultra Mobile Platform DOC #: SP-AP-0078 (Rev. 1.0)				
REV.	**ECR#**	**Issue Date**	**Orig. of Change**	**Description of Change**
AA	1695	02/09/11	JMA	Initial Release

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