# TS7003

## A 300ksps, Single-supply, 12-Bit Serial-output ADC

## FEATURES

- Pin-Compatible, Single-channel Higher-Speed Upgrade to MAX1286
- Single-Supply Operation: +2.7V to +3.6V
- DNL & INL: ±1LSB (max)
- 300ksps Sampling Rate
- Low Conversion-Mode Supply Current: 0.95mA @ 300ksps
- Low Supply Current in Shutdown: 0.2µA
- Internal 10-MHzTrack-and-Hold
- Internal ±0.6%, 30ppm/ºC +2.5V Reference
- SPI/QSPI/MICROWIRE 3-Wire Serial-Interface
- 8-Pin, 3mm x 3mm TDFN-EP Package

## APPLICATIONS

Process Control and Factory Automation
Data and Low-frequency Signal Acquisition
Portable Data Logging
Pen Digitizers & Tablet Computers
Medical Instrumentation
Battery-powered Instruments

## DESCRIPTION

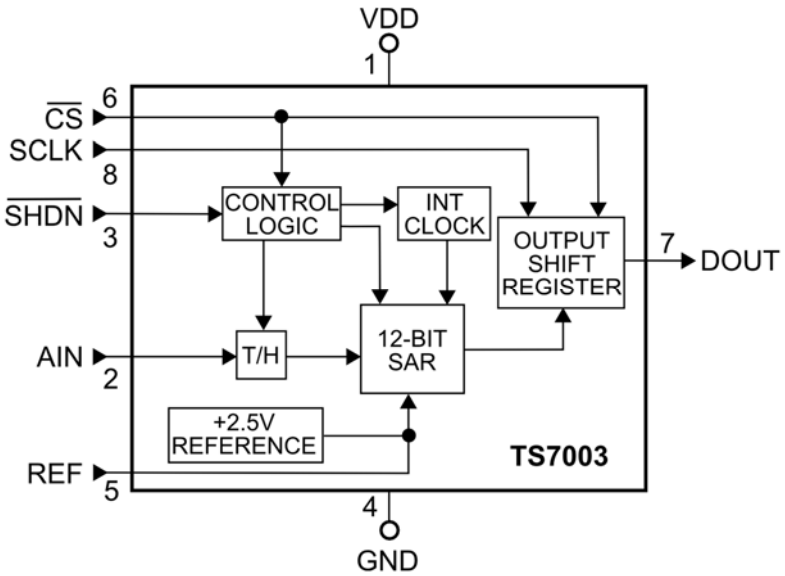
The TS7003 – a single-supply, single-channel, 12-bit analog-to-digital converter (ADC) - is a successive-approximation ADC that combines a high-bandwidth track-and-hold (T/H), a high-speed serial digital interface, an internal +2.5V reference, and low conversion-mode power consumption. The TS7003 operates from a single +2.7V to+3.6V supply and draws less than 1mA at 300ksps.

Connecting directly to any SPI™/QSPI™/ MICROWIRE™ microcontrollers and other interface-compatible computing devices, the TS7003's 3-wire serial interface is easy to use and doesn't require separate, external logic. An external serial-interface clock controls the TS7003's conversion process and its output shift register operation.

In PCB-space-conscious, low-power remote-sensor and data-acquisition applications, the TS7003 is an excellent choice for its low-power, ease-of-use, and small-package-footprint attributes.

As a pin-compatible and higher-speed upgrade to the MAX1286, the TS7003 is fully specified over the -40°C to +85°C temperature range and is available in a low-profile, 8-pin 3x3mm TDFN package with an exposed back-side paddle.

## FUNCTIONAL BLOCK DIAGRAM



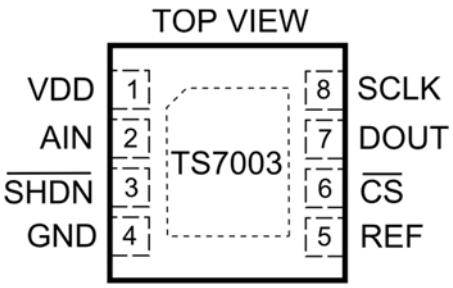
## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND ..... -0.3V to +6V
AIN to GND ..... -0.3V to ($V_{DD}$ + 0.3V)
REF to GND ..... -0.3V to ($V_{DD}$ + 0.3V)
Digital Inputs to GND ..... -0.3V to +6V
DOUT to GND ..... -0.3V to ($V_{DD}$ + 0.3V)
DOUT Current ..... ±25mA
Continuous Power Dissipation ($T_A$ = +70°C):
8-Pin TFDN33-EP (Derate 12.5mW/°C above +70°C) .1000mW

Operating Temperature Ranges:
TS7003I ..... -40°C to +85°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C
Soldering Temperature (Reflow) ..... +260°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

## PACKAGE/ORDERING INFORMATION




3mm x 3mm x 0.75mm DFN-EP 8L
TD833 Package

| ORDER NUMBER | PART MARKING | CARRIER | QUANTITY |
|---|---|---|---|
| TS7003ITD833 | 7003I | Tape & Reel | ----- |
| TS7003ITD833T | | Tape & Reel | 3000 |

**Lead-free Program:** Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

# ELECTRICAL SPECIFICATIONS

$V_{DD}$ = +2.7V to +3.6V; $f_{SCLK}$ = 4.8MHz, 50% duty cycle, 16 clocks/conversion cycle, 300ksps; 4.7µF capacitor at REF; $T_A$ = -40ºC to +85ºC, unless otherwise noted. Typical values apply at $T_A$ = +25°C.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC ACCURACY** (See Note 1) | | | | | | |
| Resolution | | | 12 | | | Bits |
| Relative Accuracy | INL | See Note 2 | | | ±1.0 | LSB |
| Differential Nonlinearity | DNL | No missing codes over temperature | | | ±1.0 | LSB |
| Offset Error | ZE | | | | ±6.0 | LSB |
| Gain Error | GE | See Note 3 | | | ±6.0 | LSB |
| Gain-Error Temperature Coefficient | TCGE | | | ±1.6 | | ppm/°C |
| **DYNAMIC SPECIFICATIONS** ($f_{IN}$ = 75kHz sine wave, 2.5$V_{PP}$, $f_{SAMPLE}$ = 300ksps, $f_{SCLK}$ = 4.8MHz) | | | | | | |
| Signal-to-Noise Plus Distortion Ratio | SINAD | | | 70 | | dB |
| Total Harmonic Distortion | THD | Including the 5th harmonic | | -80 | | dB |
| Spurious-Free Dynamic Range | SFDR | | | 80 | | dB |
| Intermodulation Distortion | IMD | $f_A$ = 73kHz, $f_B$ = 77kHz | | 76 | | dB |
| Full-Power Bandwidth | FPBW | -3dB point | | 10 | | MHz |
| Full-Linear Bandwidth | FLBW | SINAD > 68dB | | 300 | | kHz |
| **CONVERSION RATE** | | | | | | |
| Conversion Time | $t_{CONV}$ | See Note 4 | 3.3 | | | µs |
| Track/Hold Acquisition Time | $t_{ACQ}$ | | | | 625 | ns |
| Aperture Delay | $t_{AD}$ | | | 10 | | ns |
| Aperture Jitter | $t_{AJ}$ | | | < 50 | | ps |
| Serial Clock Frequency | $t_{SCLK}$ | | 0.5 | | 4.8 | MHz |
| Duty Cycle | | | 40 | | 60 | % |
| **ANALOG INPUT (AIN)** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 0 | | VREF | V |
| Input Capacitance | $C_{INA}$ | | | 10 | | pF |
| **INTERNAL REFERENCE** | | | | | | |
| REF Output Voltage | VREF | | 2.485 | 2.50 | 2.515 | V |
| REF Short-Circuit Current | | $T_A$ = +25°C | | 15 | | mA |
| REF Output Tempco | TCVREF | | | 30 | | ppm/°C |
| Load Regulation | | See Note 5; 0 to 0.75mA output load | | 3 | 5 | mV/mA |
| Capacitive Bypass at REF | | | 4.7 | | 10 | µF |
| **DIGITAL INPUTS (SCLK, $\overline{CS}$, $\overline{SHDN}$)** | | | | | | |
| Input High Voltage | $V_{INH}$ | | 2.4 | | | V |
| Input Low Voltage | $V_{INL}$ | | | | 0.8 | V |
| Input Hysteresis | $V_{HYST}$ | | | 0.2 | | V |
| Input Leakage | $I_{IN}$ | $V_{INL}$ = 0V or $V_{INH}$ = $V_{DD}$ | | | ±1 | µA |
| Input Capacitance | $C_{IND}$ | | | 15 | | pF |
| **DIGITAL OUTPUT (DOUT)** | | | | | | |
| Output Voltage Low | $V_{OL}$ | $I_{SINK}$ = 5mA | 0.4 | | | V |
| Output Voltage High | $V_{OH}$ | $I_{SOURCE}$ = 0.5mA | $V_{DD}$ - 0.5 | | | V |
| Three-State Leakage Current | $I_L$ | $V_{\overline{CS}}$ = +3V | | ±10 | | µA |
| Three-State Output Capacitance | $C_{OUT}$ | $V_{\overline{CS}}$ = +3V | | 15 | | pF |
| **POWER SUPPLY** | | | | | | |
| Positive Supply Voltage | $V_{DD}$ | See Note 6 | 2.7 | | 3.6 | V |
| Positive Supply Current | $I_{DD}$ | See Note 7; $V_{DD}$ = +3.6V | | 0.95 | 1.25 | mA |
| Shutdown Supply Current | $I_{\overline{SHDN}}$ | SCLK = $V_{DD}$, $\overline{SHDN}$ = GND | | 0.2 | 2 | µA |
| Power-Supply Rejection | PSR | $V_{DD}$ = +2.7V to 3.6V, midscale input | | ±0.5 | ±2.5 | mV |

## TIMING SPECIFICATIONS

$V_{DD}$ = +2.7V to +3.6V, $T_A$ = -40ºC to +85ºC, unless otherwise noted.

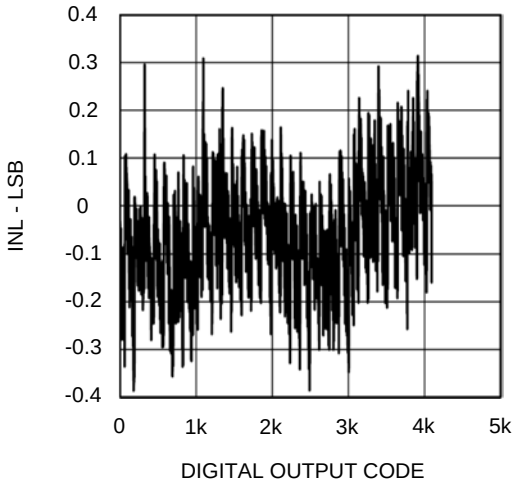
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCLK Period | $t_{CP}$ | | 208 | | | ns |
| SCLK Pulse-Width High | $t_{CH}$ | | 83 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 83 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup | $t_{CSS}$ | | 45 | | | ns |
| SCLK Rise to $\overline{CS}$ Rise Hold | $t_{CSH}$ | | 0 | | | ns |
| SCLK Rise to $\overline{CS}$ Fall Ignore | $t_{CSO}$ | | 45 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Ignore | $t_{CS1}$ | | 45 | | | ns |
| SCLK Rise to DOUT Hold | $t_{DOH}$ | $C_{LOAD}$ = 20pF | 13 | | | ns |
| SCLK Rise to DOUT Valid | $t_{DOV}$ | $C_{LOAD}$ = 20pF | | | 100 | ns |
| $\overline{CS}$ Rise to DOUT Disable | $t_{DOD}$ | $C_{LOAD}$ = 20pF; Refer to Figure 2 | 13 | | 85 | ns |
| $\overline{CS}$ Fall to DOUT Enable | $t_{DOE}$ | $C_{LOAD}$ = 20pF; Refer to Figure 1 | | | 85 | ns |
| $\overline{CS}$ Pulse-Width High | $t_{CSW}$ | | 100 | | | ns |

**Note 1:** Tested at $V_{DD} = V_{DD(MIN)}$.
**Note 2:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
**Note 3:** Internal reference, offset, and reference errors nulled.
**Note 4:** Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
**Note 5:** External load should not change during conversion for specified accuracy. Guaranteed specification limit of 2mV/mA because of production test limitations.
**Note 6:** Electrical characteristics are guaranteed from $V_{DD(MIN)}$ to $V_{DD(MAX)}$. For operations beyond this range, see Typical Operating Characteristics.
**Note 7:** TS7003 tested with 20pF on DOUT and $f_{SCLK}$ = 4.8MHz, 0 to 3V. DOUT = full scale.

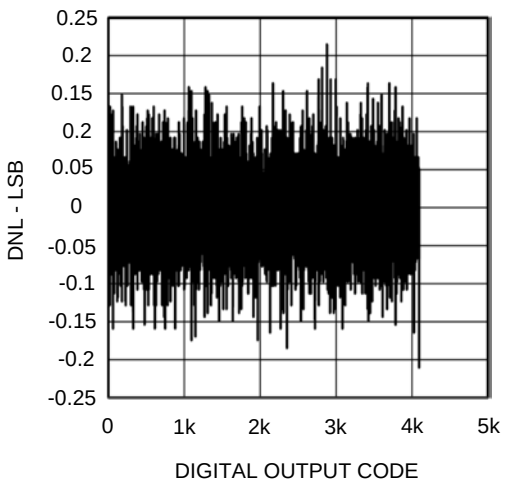
# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD}$ = +3V; $f_{SCLK}$ = 4.8MHz; $C_{LOAD}$ = 20pF; 4.7µF capacitor at REF; $T_A$ = 25ºC, unless otherwise noted.

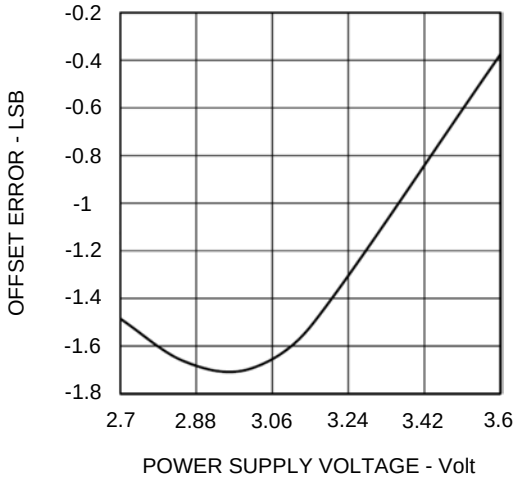
**Integral Nonlinearity**



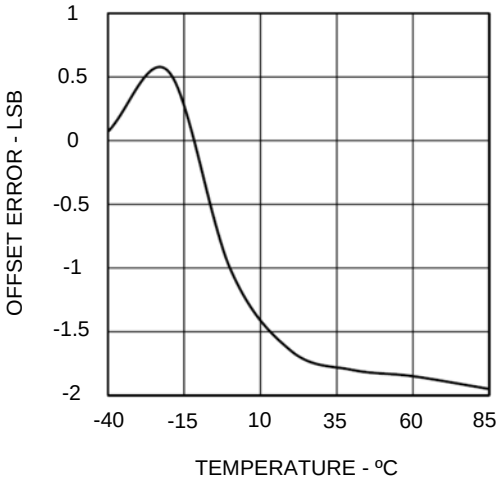

**Differential Nonlinearity**



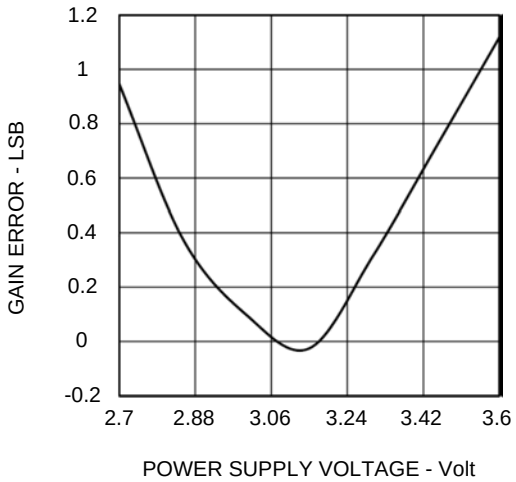

**Offset Error vs Supply Voltage**



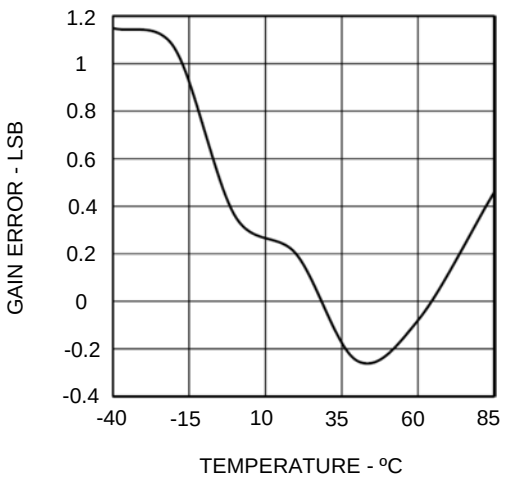

**Offset Error vs Temperature**




**Gain Error vs Supply Voltage**



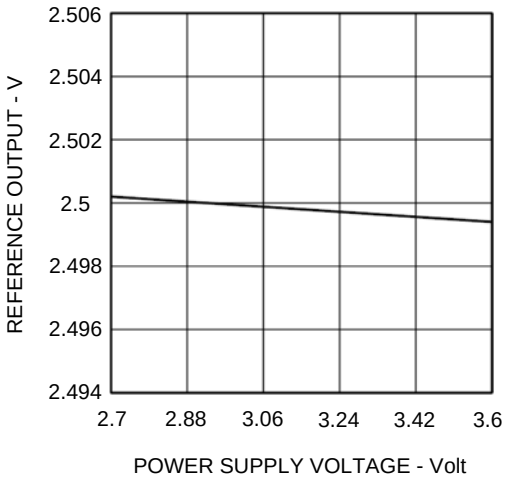

**Gain Error vs Temperature**



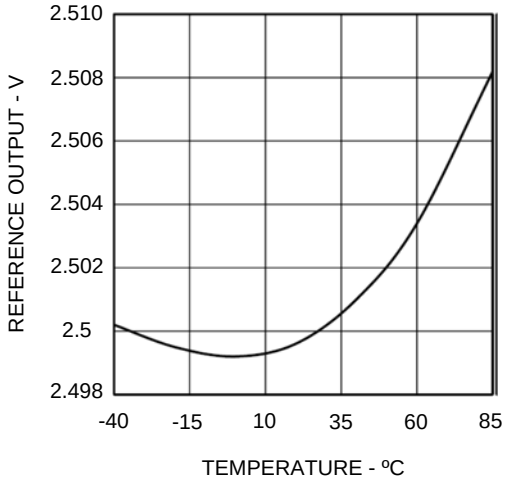
# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD}$ = +3V; $f_{SCLK}$ = 4.8MHz; $C_{LOAD}$ = 20pF; 4.7µF capacitor at REF; $T_A$ = 25ºC, unless otherwise noted.

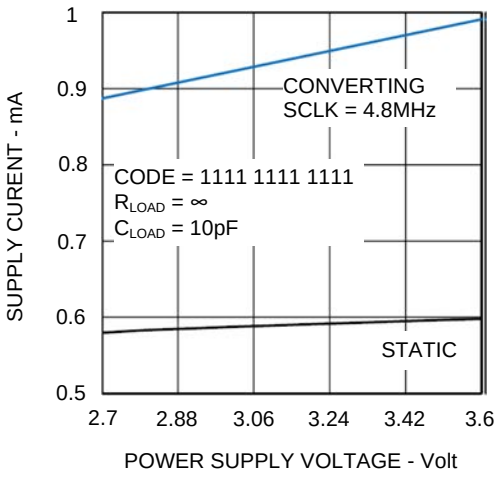
**Internal Reference Output vs Supply Voltage**



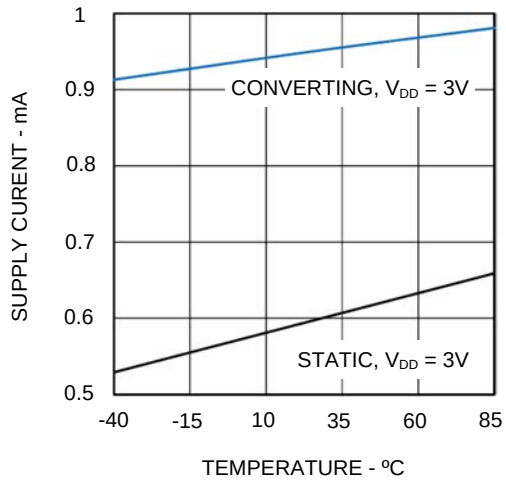

**Internal Reference Output vs Temperature**




**Power Supply Current vs Power Supply Voltage**




**Power Supply Current vs Temperature**



## PIN FUNCTIONS

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | VDD | Power Supply Voltage, +2.7V to +3.6V. |
| 2 | AIN | Analog Signal Input; Unipolar, 0 to VREF input range. |
| 3 | $\overline{\text{SHDN}}$ | Active-Low Shutdown Input. Toggling $\overline{\text{SHDN}}$ high-to-low powers down the TS7003 and reduces the supply current to 0.2µA (typ). |
| 4 | GND | Analog and Digital Ground. Connect the TS7003's GND pin at one and only one point to the system analog ground plane. |
| 5 | REF | Reference Voltage for Analog-to-Digital Conversion – an internal 2.5V reference output. Bypass with a good-quality 4.7µF capacitor. |
| 6 | $\overline{\text{CS}}$ | Active-Low Chip Select. The $\overline{\text{CS}}$ signal initiates the conversion process on its falling edge. When the CS input is logic high, DOUT is high impedance. |
| 7 | DOUT | Serial-Data Output. DOUT toggles state on SCLK's rising edge and is high impedance when CS is logic high. |
| 8 | SCLK | Serial-Clock Input. The SCLK signal controls the conversion process and transfers output data at rates up to 4.8MHz. |

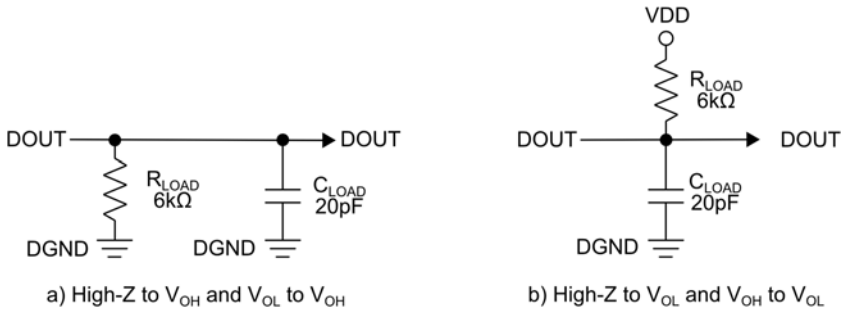



**Figure 1:** Output Loading Circuits for DOUT Enable Time ($t_{DOE}$).

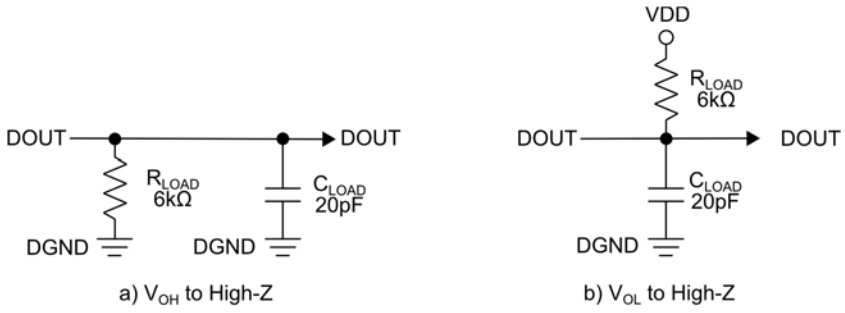



**Figure 2:** Output Loading Circuits for DOUT Disable Time ($t_{DOD}$).

# DESCRIPTION OF OPERATION

### Converter Operation

The TS7003 uses an input track-and-hold (T/H) and a successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 12-bit output. No external-hold capacitor is needed for the track/hold circuit. Figure 3 illustrates the TS7003 in its simplest configuration. The TS7003 converts input

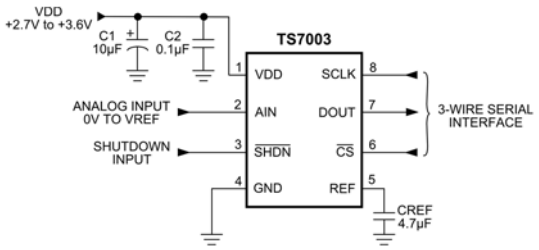



**Figure 3:** TS7003 Typical Application Circuit.

signals within the 0V to $V_{REF}$ range in 3.3µs including the track-and-hold's acquisition time. The serial interface requires only three digital lines (SCLK, $\overline{CS}$, and DOUT) and provides an easy interface to microprocessors (µPs) and microcontrollers (µCs).

The TS7003 has two operating modes: normal and shutdown. Toggling (or driving) the $\overline{SHDN}$ pin low shuts down the ADCs and reduces supply current below 1 µA when $V_{DD} \leq 3.6V$. Open-circuiting or toggling (or driving) the $\overline{SHDN}$ pin high or places the ADCs into operational mode. Toggling the $\overline{CS}$ pin to logic low initiates a conversion where the conversion result is available at DOUT in unipolar serial format. The serial data stream consists of three leading zeros followed by the data bits with the MSB first. All transitions on the DOUT pin occur within 20ns after the low-to-high transition of SCLK. Serial interface timing details of the TS7003 are illustrated in Figures 8 and 9.

### Analog Input

Figure 4 illustrates the sampling architecture of the

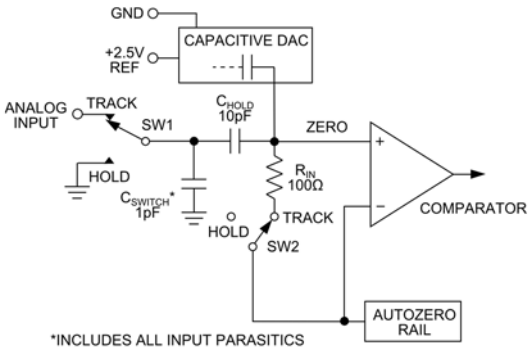



**Figure 4:** TS7003 Equivalent Input Circuit Details.

analog-to-digital converter's comparator. The full-scale input voltage is set by the TS7003's internal 2.5-V reference.

### Track-and-Hold Operation

During track mode, the analog signal is acquired and stored on the internal hold capacitor. During hold mode, the track/hold switches SW1 and SW2 are opened thereby maintaining a constant input level to the converter's SAR subcircuit.

During the acquisition phase with SW1 and SW2 on TRACK, the input capacitor, $C_{HOLD}$, is charged to the analog input (AIN). Toggling the $\overline{CS}$ pin low causes the acquisition process to stop. At this instant, track/hold switches SW1 and SW2 are moved to HOLD position and the input side of $C_{HOLD}$ is then switched to GND. Unbalancing Node ZERO at the comparator's input, the retained charge on $C_{HOLD}$ represents a sample of the input signal applied to the converter.

In hold mode and to restore Node ZERO to 0V within the limits of the converter's 12- bit resolution, the output of the capacitive digital-to-analog converter (the CDAC) is adjusted during the remainder of the conversion cycle. In other words, the stored charge on $C_{HOLD}$ is transferred to the binary-weighted CDAC where it is converted into a digital representation of the analog input signal. At end of the conversion

process, the input side of $C_{HOLD}$ is switched back to AIN so as to be charged to the input signal again.

An ADC's acquisition time is function of how fast its input capacitance can be charged. If an input signal's driving-point source impedance is high, the acquisition time is lengthened and more time must be allowed between conversions. The acquisition time ($t_{ACQ}$) is the maximum time the ADC requires to acquire the signal and is also the minimum time needed for the signal to be acquired. The TS7003's acquisition time is calculated from the following expression:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 10pF$$

where $R_{IN}$ = 100Ω (the TS7003's internal track/hold switch resistance), $R_S$ = the input signal's source impedance, and $t_{ACQ}$ is never less than 625ns.

Because of the input structure of the TS7003, sources with output impedances of 1kΩ or less do not affect significantly the AC performance of the TS7003. The TS7003 can still be used in applications where the source impedance is higher so long as a 0.01µF capacitor is connected between the analog input and GND. Limiting the ADC's input signal bandwidth, the use of an external, input capacitor forms an RC filter with the input's source impedance.

### Input Bandwidth Considerations

Since the TS7003's input track-and-hold circuit exhibits a 10 MHz small-signal bandwidth, it is possible to measure periodic signals and to digitize high-speed transient events with signal bandwidths higher than the TS7003's sampling rate by using undersampling techniques. To avoid the aliasing of high-frequency signals into the frequency band of interest, the use of external anti-alias filter circuits (discrete or integrated) is recommended. The time constant of the external anti-alias filter should be set so as not to interfere with the desired signal bandwidth.

### Analog Input Protection

The TS7003 incorporates internal protection diodes that clamp the analog input between $V_{DD}$ and GND. These internal protection diodes allow the AIN pin to swing from GND - 0.3V to $V_{DD}$ + 0.3V without causing damage to the TS7003. However, for accurate conversions near full scale, the input signal must not exceed $V_{DD}$ by more than 50mV or be lower than GND by 50mV.

**If the analog inputs can exceed 50mV beyond the supplies, then the current in the forward-biased protection diodes should be limited to less than 2mA since large fault currents can affect conversion results.**

### Internal Reference Considerations

The TS7003 has an internal voltage reference that is factory-trimmed to 2.5V. The internal reference output is connected to the REF pin and is also connected to the ADC's internal CDAC. The REF output can be used as a reference voltage source for other components external to the ADC and can source up to 750µA. To maintain conversion accuracy to within 1 LSB, a 4.7µF capacitor from the REF pin to GND is recommended. While larger-valued capacitors can be used to further reduce reference wide-band noise, larger capacitor values can increase the TS7003's wake-up time when exiting from shutdown mode (see the "Using $\overline{SHDN}$ to Reduce Operating Supply Current" section for more information). When in shutdown (that is, when $\overline{SHDN}$ = 0), the TS7003's internal 2.5-V reference is disabled.

## Serial Digital Interface

### Initialization after Power-Up and Starting a Conversion

If the $\overline{SHDN}$ pin is not driven low upon an initial, cold-start condition, it may take up to 2.5ms for a fully-discharged 4.7µF reference bypass capacitor to provide adequate charge for specified conversion accuracy. As a result, conversions should not be initiated during this reference capacitor charge-up delay. To initiate a conversion, the $\overline{CS}$ pin is toggled (or driven) low. At the $\overline{CS}$'s falling edge, the TS7003's internal track-and-hold is placed in hold mode and a conversion is initiated. Data can then be transferred out of the ADC using an external serial clock.

### Using the ADC's $\overline{SHDN}$ to Reduce Operating Supply Current

Power consumption can be reduced significantly by turning off the TS7003 in between conversions.

**Figure 5:** TS7003 Supply Current vs Conversion Rate

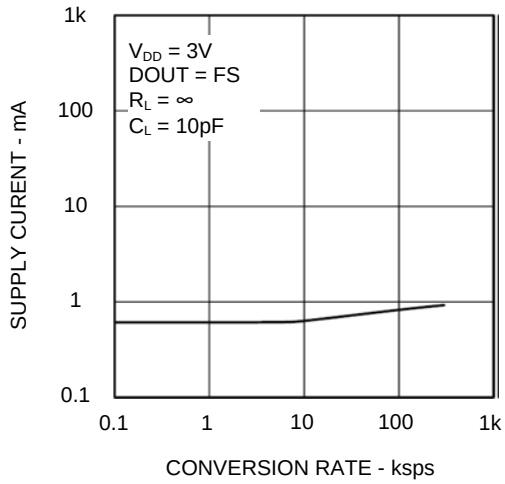



Figure 5 illustrates the TS7003's average supply current versus conversion rate. The wake-up delay time ($t_{WAKE}$) is the time from when the $\overline{SHDN}$ pin is deasserted to the time when a conversion may be initiated (Refer to Figure 6). This delay time depends on how long the ADC was in shutdown (Refer to Figure 7) because the external 4.7µF reference bypass capacitor is discharged slowly when $\overline{SHDN}$ = 0.

### Timing and Control Details

The $\overline{CS}$ and SCLK digital inputs control the TS7003's conversion-start and data-read operations. The ADC's serial-interface operations are illustrated in Figures 8 and 9.

A $\overline{CS}$ high-to-low transition initiates the conversion sequence - the input track-and-hold samples the input signal level, the ADC begins to convert, and the DOUT pin changes state from high impedance to logic low. The external SCLK signal is used to drive the conversion process and is also used to transfer the converted data out of the ADC as each bit of conversion is determined.

The SCLK signal transfers data after a low-to-high transition of the third (3rd) SCLK pulse. After each subsequent SCLK rising edge, transitions on the DOUT pin occur in 20ns. The third rising clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are twelve data bits and three leading zeros, at least fifteen rising clock edges are needed to transfer the entire data stream. Extra SCLK pulses occurring after the conversion result has been completely transferred out and, before to a new, low-to-high transition on $\overline{CS}$, produce a string trailing zeros at DOUT. In addition, the extra SCLK pulses have no effect on converter operation.

Minimum conversion cycle time can be accomplished by: (a) toggling the $\overline{CS}$ pin high after reading the conversion result's LSB; and (b), after the specified minimum time defined by $t_{CS}$ has elapsed, toggling the $\overline{CS}$ pin low again to initiate the next conversion.

### Output Data Coding and Transfer Function

Conversion results at the TS7003's DOUT pin are straight binary data. Figure 10 illustrates the nominal transfer function where code transitions occur halfway between successive integer LSB values. If $V_{REF}$ = +2.500V, then 1 LSB = 610µV or 2.500V/4096.

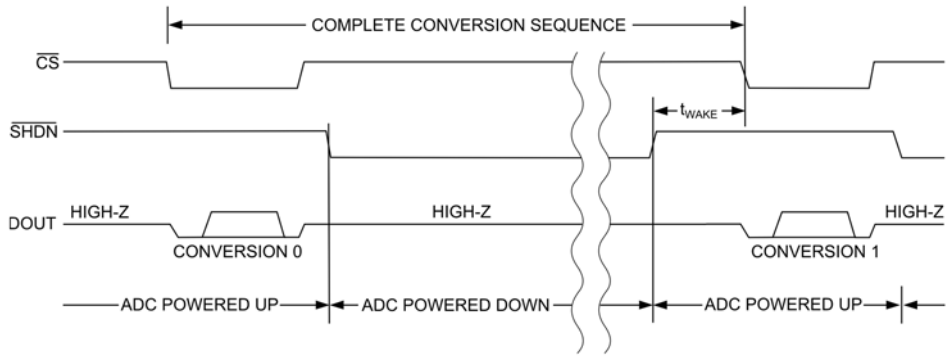
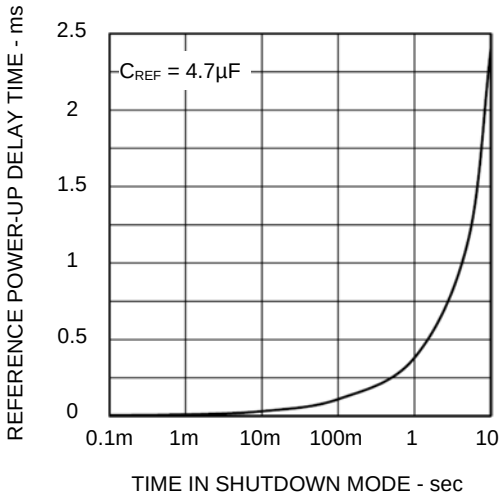



**Figure 6:** TS7003 Shutdown Operation.

**Figure 7:** TS7003 Reference Power-Up Delay vs Duration in Shutdown Mode




# APPLICATIONS INFORMATION

### Connection to Industry-Standard Serial Interfaces

The TS7003's serial interface is fully compatible with SPI/QSPI and MICROWIRE standard serial interfaces (Refer to Figure 11). For serial interface operation with these standards, the CPU's serial interface should be set to master mode so the CPU then generates the serial clock. Second, the CPU's serial clock should be configured to operate up to 4.8MHz. The process to configure the serial clock and data transfer operation is as follows:

1) Using a general-purpose I/O line from the CPU, the $\overline{CS}$ pin is driven low to start a conversion. DOUT transitions from high impedance to logic low. The SCLK polarity should be low to start the conversion process correctly.

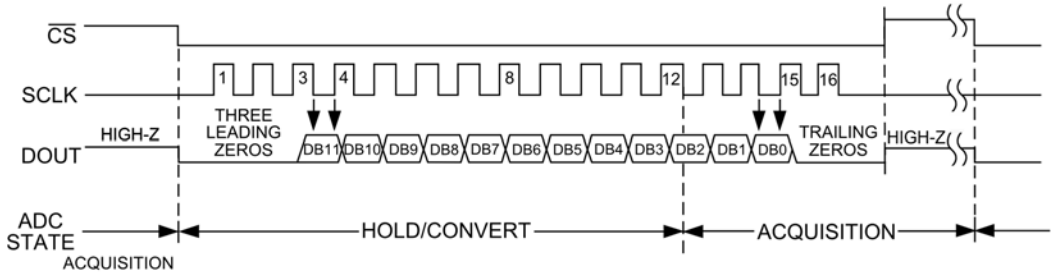



**Figure 8:** TS7003 Serial Interface Timing Sequence

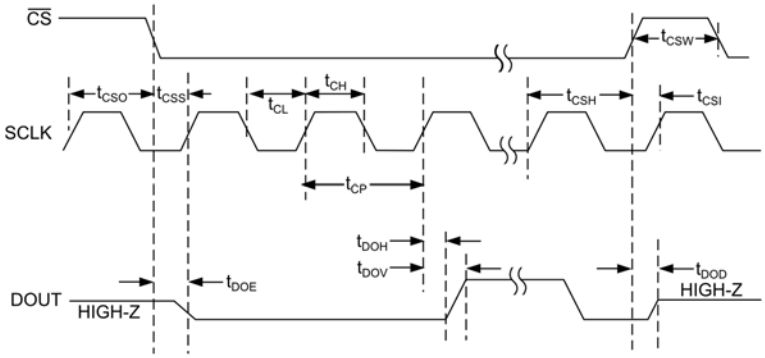



**Figure 9:** TS7003 Serial Interface Timing Specifications in Detail.

2) Next, SCLK is activated for a minimum of 15 SCLK cycles where the first two SCLKs produce zeros at the DOUT pin. Data at DOUT is formatted MSB first and DOUT transitions occur 20ns after the third (3rd) SCLK low-to-high transition. Once the low-to-high SCLK transition has occurred, data is valid at DOUT

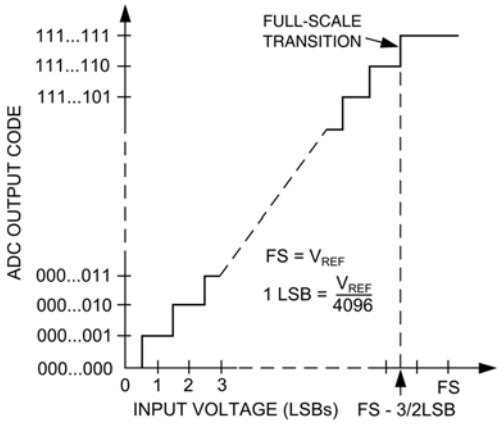



**Figure 10:** ADC Unipolar Transfer Function for Straight Binary Digital Data.

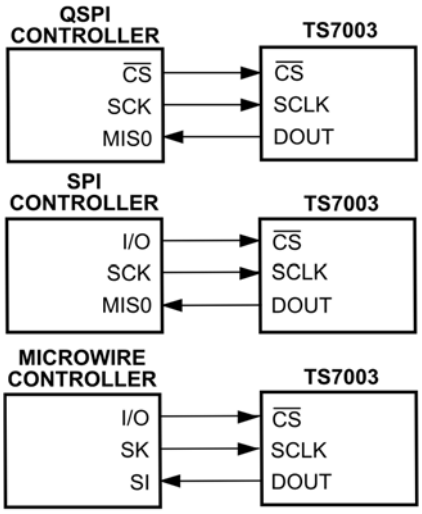



**Figure 11:** TS7003 Circuit Connections to Industry-Standard Serial Interfaces

according to the $t_{DOV}$ (SCLK Rise to DOUT Valid) timing specification. Valid output data can then be transferred into µP or µCs on SCLK low-to-high transitions.

3) At or after the 15th SCLK low-to-high transition, the $\overline{CS}$ pin can be toggled high to halt the transfer process. If the $\overline{CS}$ pin remains low and the SCLK is still active, trailing zeros are transferred out after the LSB.

4) Once the $\overline{CS}$ pin is held at logic high for at least $t_{CS}$, a new conversion cycle is started when the $\overline{CS}$ pin is toggled low. If a conversion is aborted by toggling the $\overline{CS}$ pin high before the current conversion has completed, a new conversion cycle can only be started after a the ADC has acquired the signal ($t_{ACQ}$).

The $\overline{CS}$ pin must be held low and SCLK active until all data bits are transferred out of the ADC. As shown in Figure 8, data can be transferred in two 8-bit bytes or continuously. The bytes contain the result of the conversion padded with three leading 0s in the first 8-bit byte and 1 trailing 0 in the second 8-bit byte.

**SPI and MICROWIRE Interface Details**

When using an SPI or MICROWIRE interface, setting [CPOL:CPHA] = [0:0] configures the microcontroller's serial clock and sampling edge for the TS7003. The conversion commences on a high-to-low transition of the $\overline{CS}$ pin. The DOUT pin transitions from a high-impedance state to a logic low, indicating a conversion is in progress. Two consecutive 1-byte data reads are required to transfer the full 12-bit result from the ADC. DOUT output data transitions occur on the SCLK's low-to-high transition and are transferred into the downstream microcontroller on the SCLK's low-to-high transition.

The first byte contains three leading 0s and then five bits of the conversion result. The second byte contains the remaining seven bits of the conversion result and one trailing zero. Refer to Figure 11 for the circuit connections and to Figure 12 for all timing details.

**QSPI Details**

Using a QSPI microcontroller, setting [CPOL:CPHA] = [0:1] configures the microcontroller's serial clock and sampling edge for the TS7003. Unlike the SPI, which requires two 1-byte reads to transfer all 12 bits of data from the ADC, the QSPI allows a minimum number of clock cycles necessary to transfer data from the ADC to the microcontroller. Thus, the TS7003 requires 15 SCLK clock cycles from the microcontroller to transfer the 12 bits of data with no trailing zeros. As shown in Figure 13, the conversion results contain two leading 0s followed by the MSB-first-formatted, 12-bit data stream.

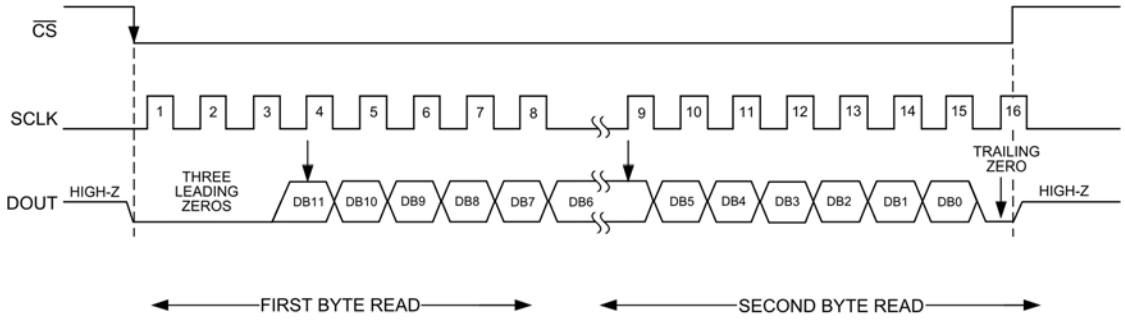



**Figure 12:** SPI/MICROWIRE-TS7003 Serial Interface Timing Details with [CPOL:CPHA] = [0:0].

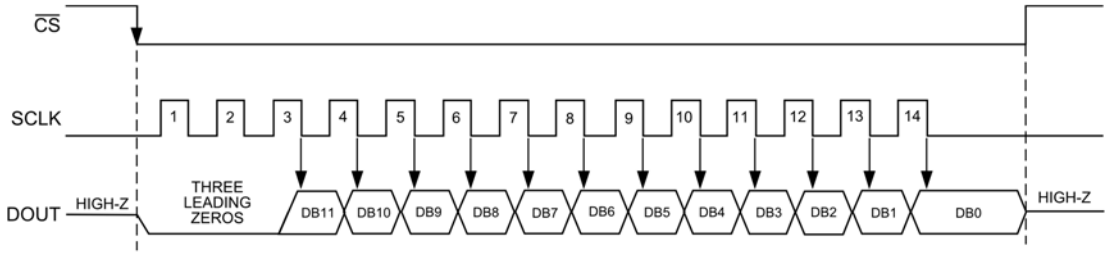



**Figure 13**: QSPI-TS7003 Serial Interface Timing Details with [CPOL:CPHA] = [0:1].

**PCB Layout, Ground Plane Management, and Capacitive Bypassing**

For best performance, printed circuit boards should always be used and wire-wrap boards are not recommended. Good PC board layout techniques ensure that digital and analog signal lines are kept separate from each other, analog and digital (especially clock) lines are not routed parallel to one another, and high-speed digital lines are not routed underneath the ADC package.

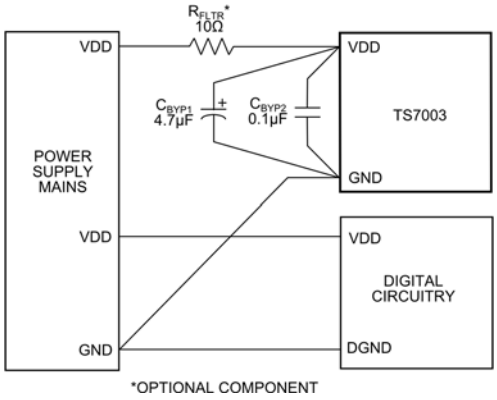



**Figure 14:** Recommended Power Supply Bypassing and Star Ground Configuration.

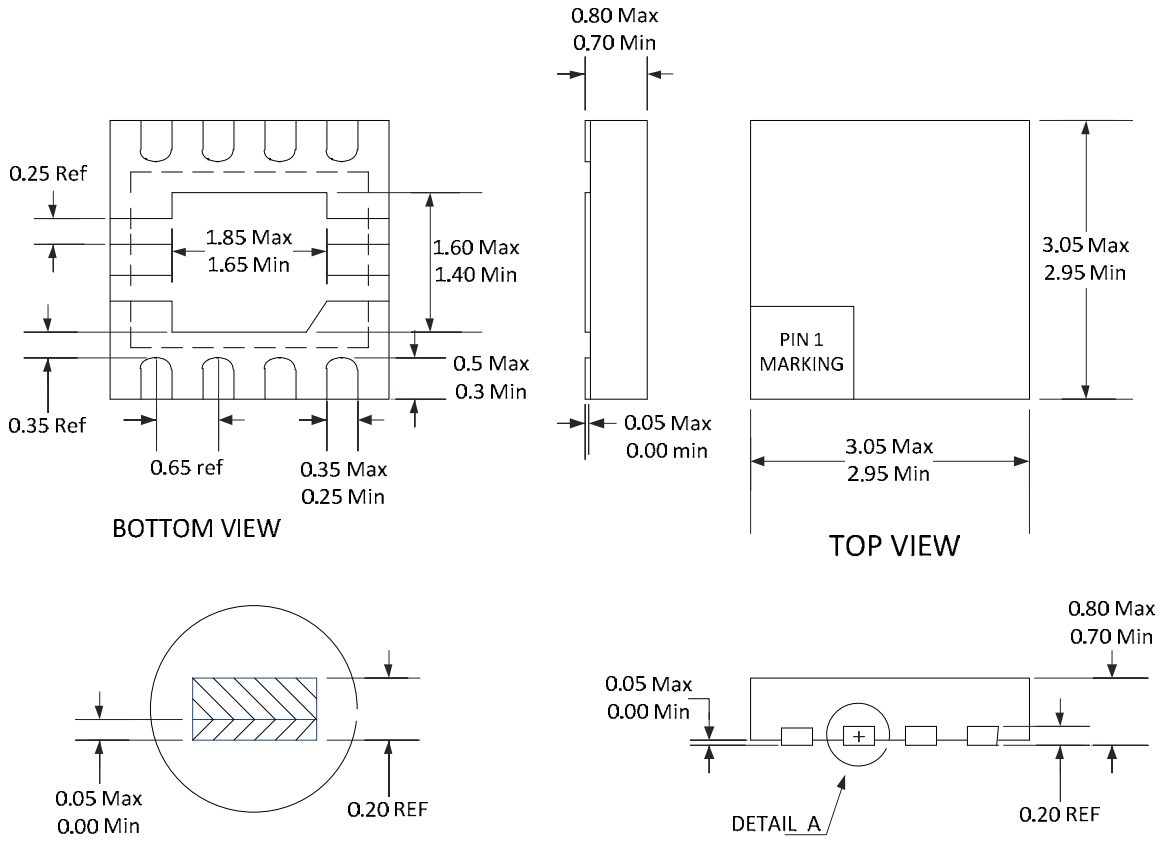
A recommended system ground connection is illustrated in Figure 14. A single-point analog ground (star ground point) should be created at the ADC's GND and separate from the logic ground. All analog grounds as well as the ADC's GND pin should be connected to the star ground. No other digital system ground should be connected to this ground. For lowest-noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

High-frequency noise on the $V_{DD}$ power supply may affect the ADC's high-speed comparator. Therefore, it is necessary to bypass the $V_{DD}$ supply pin to the star ground with 0.1µF and 1µF capacitors in parallel and placed close to the ADC's Pin 1. Component lead lengths should be very short for optimal supply-noise rejection. If the power supply is very noisy, an optional 10-Ω resistor can be used in conjunction with the bypass capacitors to form a low-pass filter as shown in Figure 14.

# PACKAGE OUTLINE DRAWING

## 8-Pin 3mm x 3mm TDFN-EP Package Outline Drawing

(N.B., Drawings are not to scale)




NOTE: CONTROLLING DIMENTIONS IN MILIMETERS
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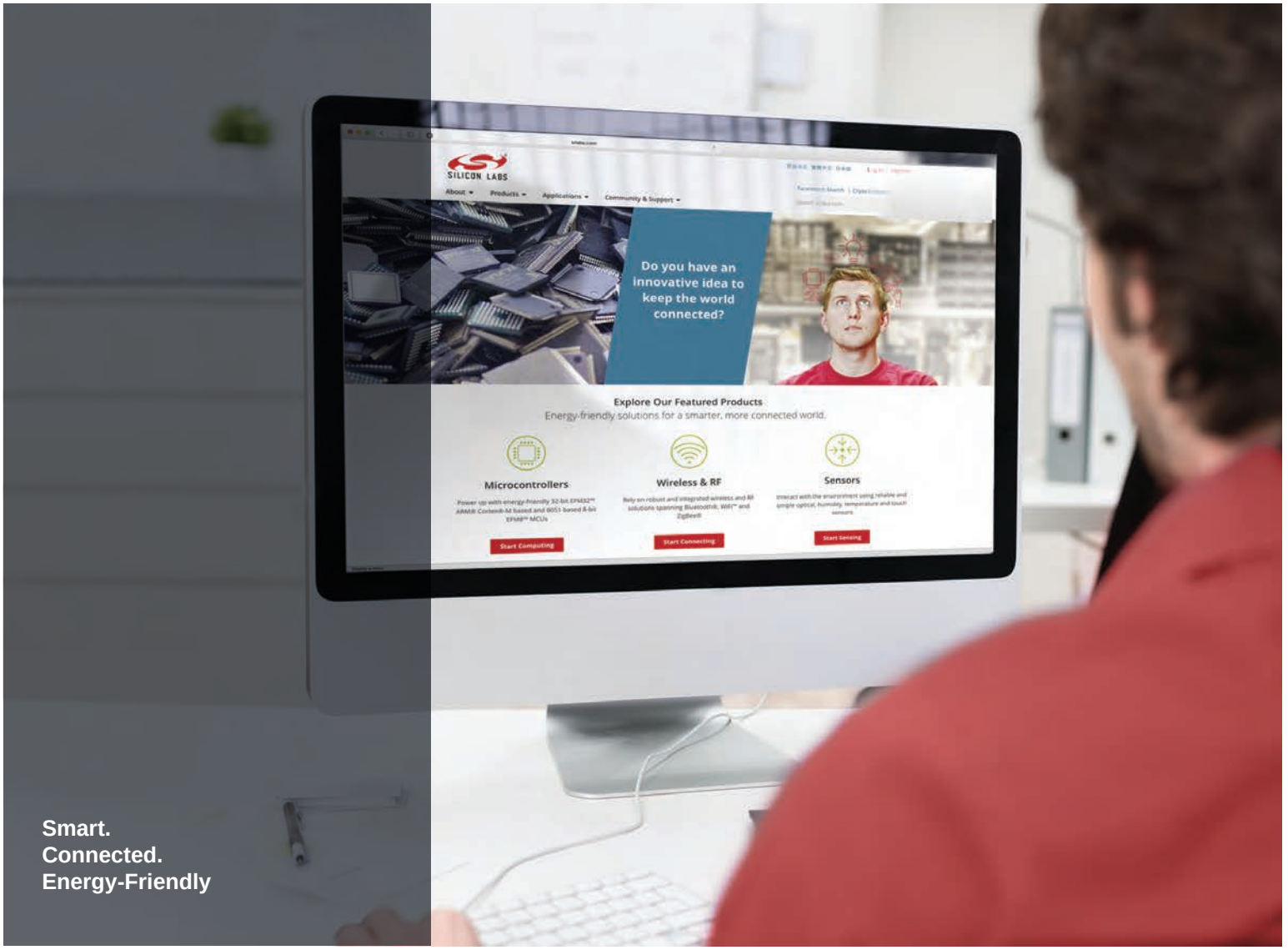


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