200V Half-Bridge Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 200 V max.
- **I_O+/-** 1 A/1.5 A
- **V_{OUT}** 10 V - 18 V
- **$t_{on/off}$ (typ.)** 150 ns/150 ns
- **Deadtime (typ.)** 110 ns

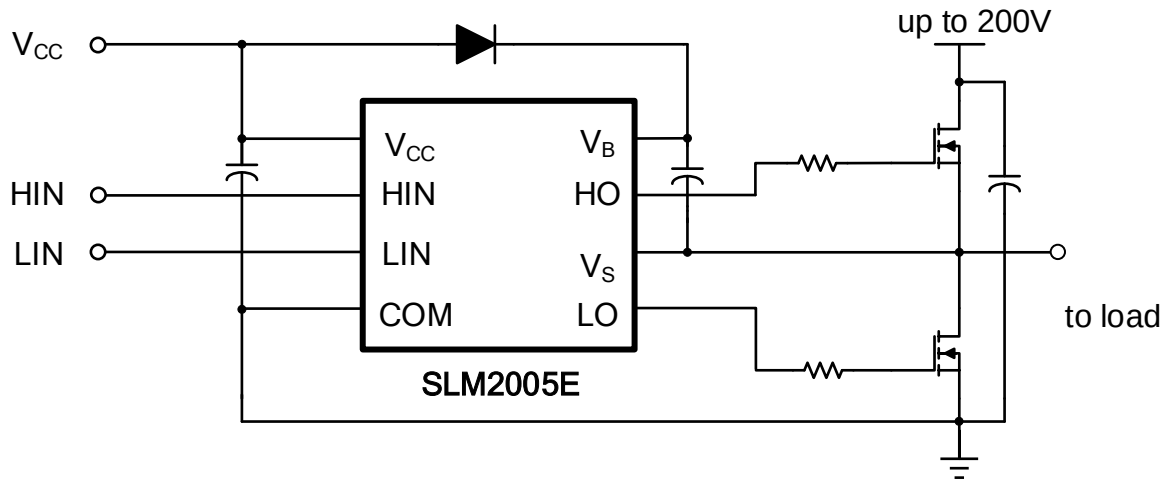
GENERAL DESCRIPTION

The SLM2005E is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 200 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 18 V
- Undervoltage lockout
- 3.3 V, 5 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High-side/Low-side output in phase with HIN/LIN input
- RoHS compliant
- SOP8 package

TYPICAL APPLICATION CIRCUIT



(Refer to Pin Configuration for correct configuration. This diagram shows electrical connections only.)

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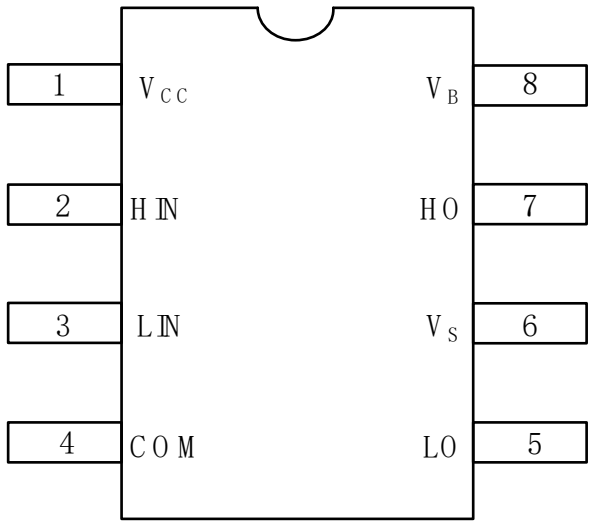
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP8	

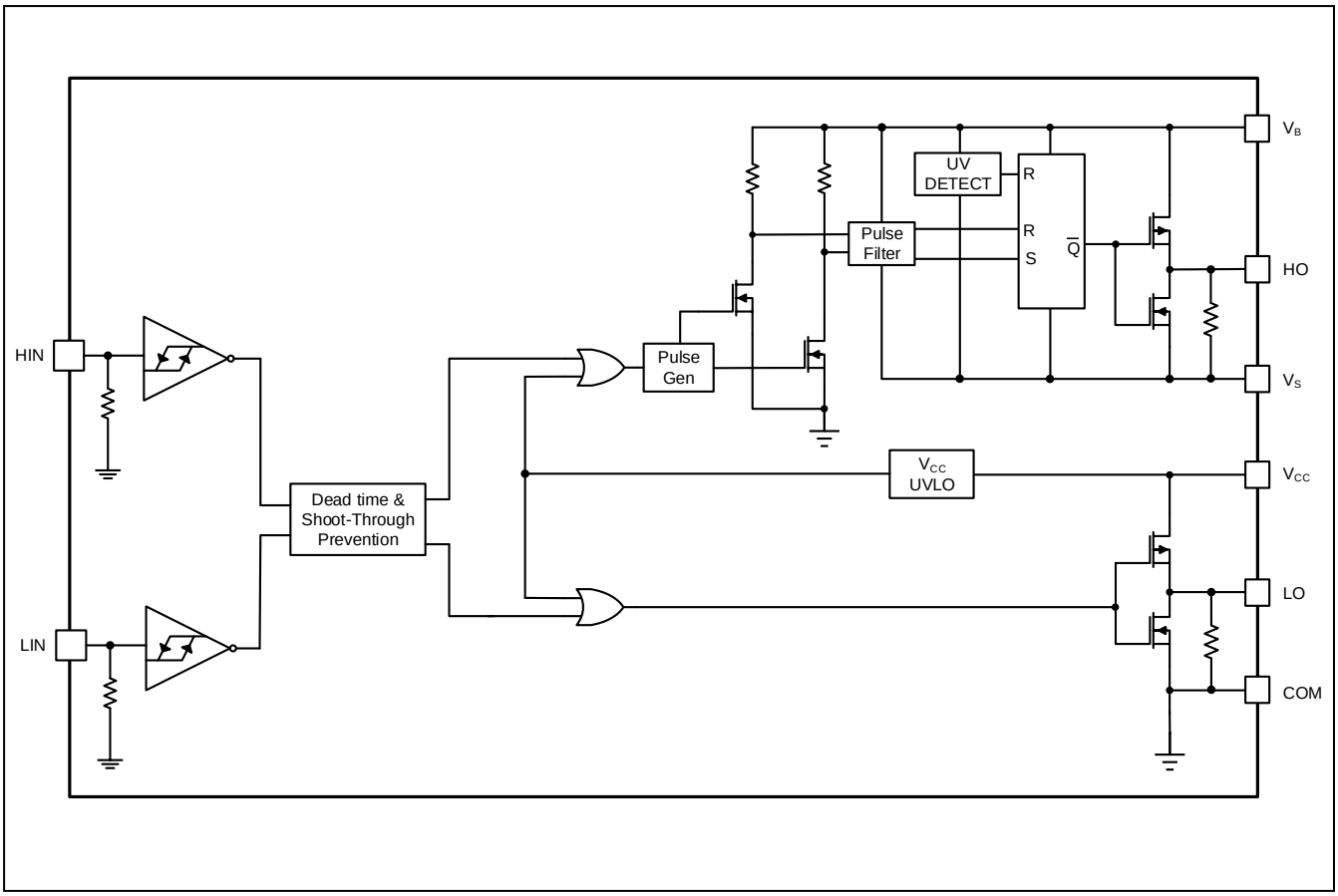
PIN DESCRIPTION

No.	Pin	Description
1	V_{CC}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

ORDERING INFORMATION

Order Part No.	Package	QTY
SLM2005ECA-DG	SOP8, Pb-Free	4000/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	-0.3	220	V
V_S	High-side floating supply offset voltage	V_B - 20	V_B + 0.3	
V_{HO}	High-side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	20	
V_{LO}	Low-side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	-0.3	10	
dV_S/dt	Allowable offset supply voltage transient	---	50	V/ns
P_D	Package power dissipation at $T_A \leqslant +25°C$	---	0.625	W
θ_{JA}	Thermal resistance, junction to ambient	---	200	°C/W
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	V_S + 10	V_S + 18	V
V_S	High-side floating supply offset voltage		200	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	18	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	0	10	
T_A	Ambient temperature	- 40	125	°C

Note: For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	150	260	ns
t_{off}	Turn-off propagation delay	V_S = 0 V	---	150	260	
t_r	Turn-on rise time		---	25	50	
t_f	Turn-off fall time		---	10	25	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		50	110	220	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

Note: See timing diagram in Figure 1, Figure 2, Figure 3 and Figure 4.

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” (HIN/LIN) input voltage	V_{CC} = 10 V to 18V	2.5	---	---	V
V_{IL}	Logic “0” (HIN/LIN) input voltage		---	---	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 20 mA	---	0.16	0.3	
V_{OL}	Low level output voltage, V_O		---	0.07	0.15	
I_{LK}	Offset supply leakage current	V_B = V_S = 200 V	---	---	50	µA
I_{QBS}	Quiescent V_{BS} supply current	V_o = 0 V	---	67	80	
I_{QCC}	Quiescent V_{CC} supply current		---	230	300	
I_{IN+}	Logic “1” input bias current on HIN/LIN	V_{IN} = 5 V	---	100	150	
I_{IN-}	Logic “0” input bias current on HIN/LIN	V_{IN} = 0 V	---	---	5	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		8	8.8	9.8	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		7.4	8.3	9	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold			4.8		

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold			4.3		V
I_{O+}	Output high short circuit pulsed current	V_O = 0 V, V_{IN} = V_{IH} PW ⩽ 10 μs		1		A
I_{O-}	Output low short circuit pulsed current	V_O = 15 V, V_{IN} = V_{IL} PW ⩽ 10 μs		1.5		

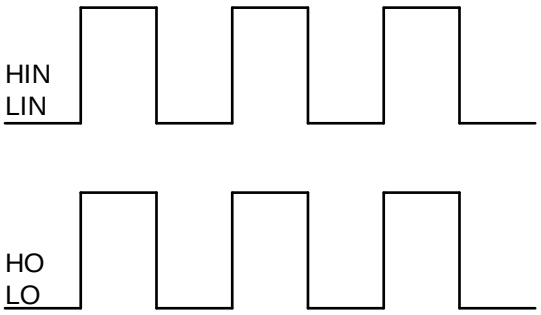


Figure 1. Input/Output Timing Diagram

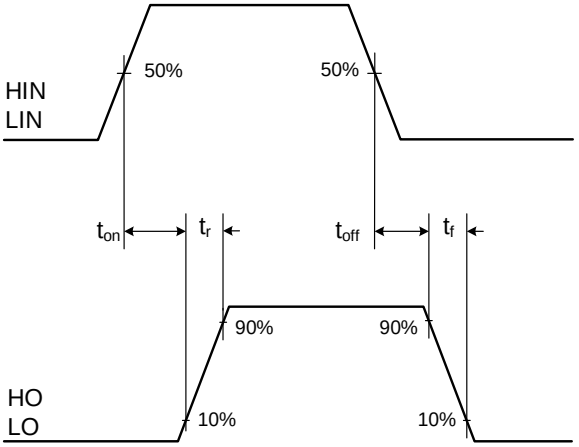


Figure 2. Switching Time Waveform

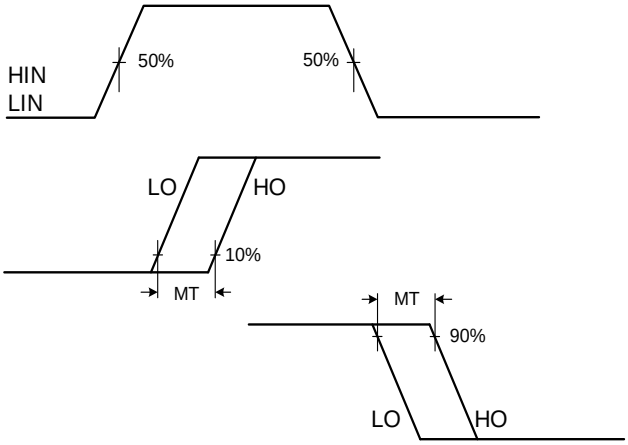


Figure 3. Delay Matching Waveform

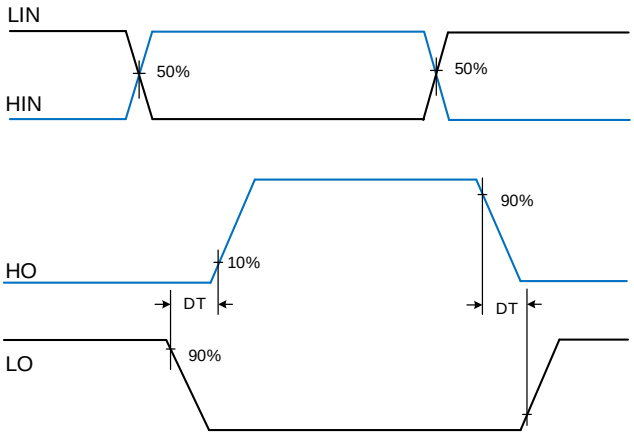
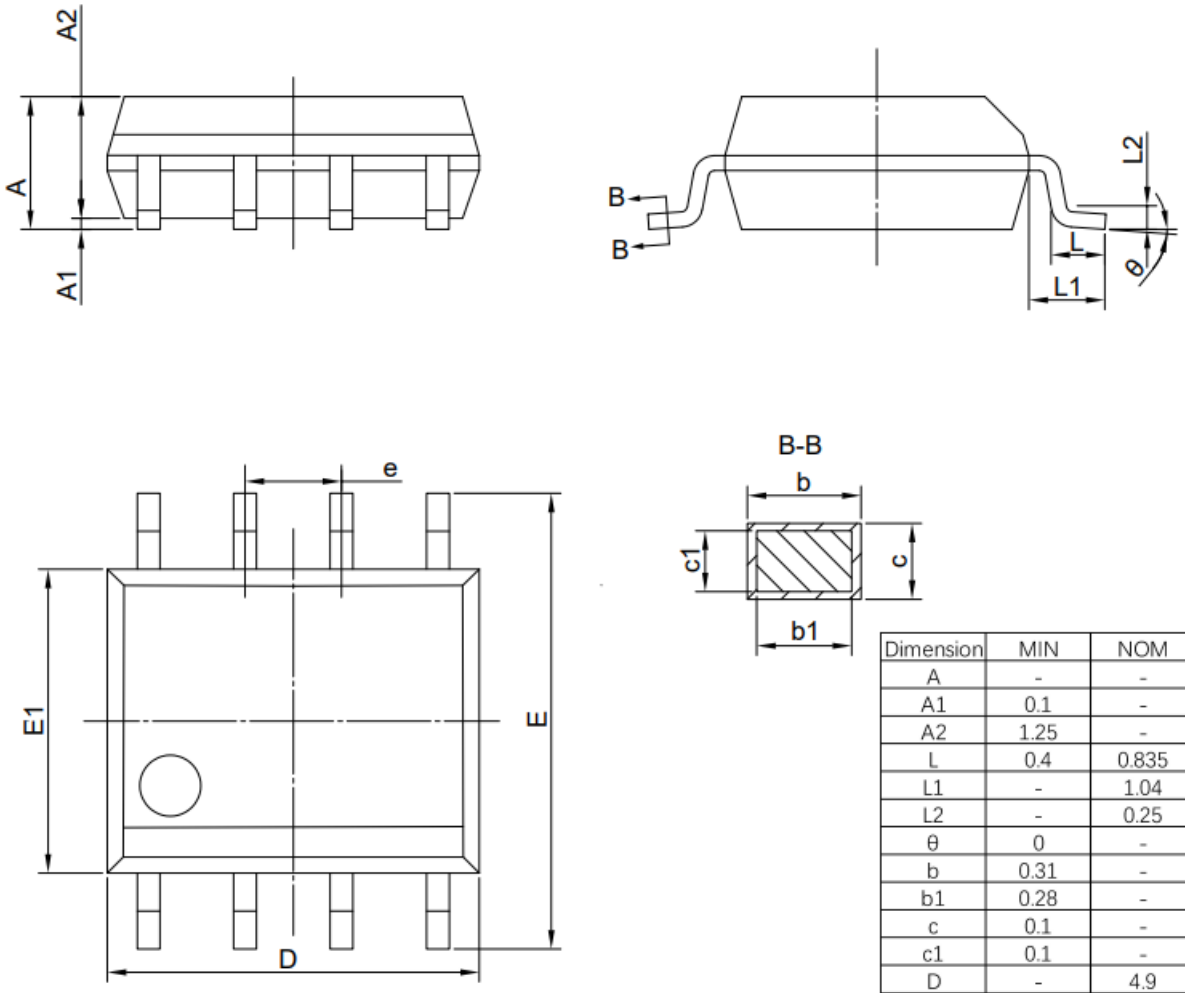


Figure 4. Deadtime Waveform

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	-	4.9	-
E	-	6	-
E1	-	3.9	-
e	1.27 BSC		
Unit : mm			

Figure 5. SOP8 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version.

Page or Item	Subjects (major changes since previous revision)
Rev 0.1 preliminary datasheet 2021-10-19	
Whole document	Rev 0.1 Preliminary datasheet release
Rev 1.0 datasheet 2022-05-16	
Whole document	Rev 1.0 datasheet release
Rev 1.1 Datasheet, 2022-12-29	
Page 8	SOP8 Outline Dimensions Update

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