

## 200V Half-Bridge Driver

### PRODUCT SUMMARY

- $V_{\text{OFFSET}}$  200 V max.
- $I_{\text{O}+/-}$  1A/1.5A
- $V_{\text{OUT}}$  10 V - 18 V
- $t_{\text{on/off}}$  (typ.) 260 ns/150 ns
- **Deadtime** (typ.) 110 ns

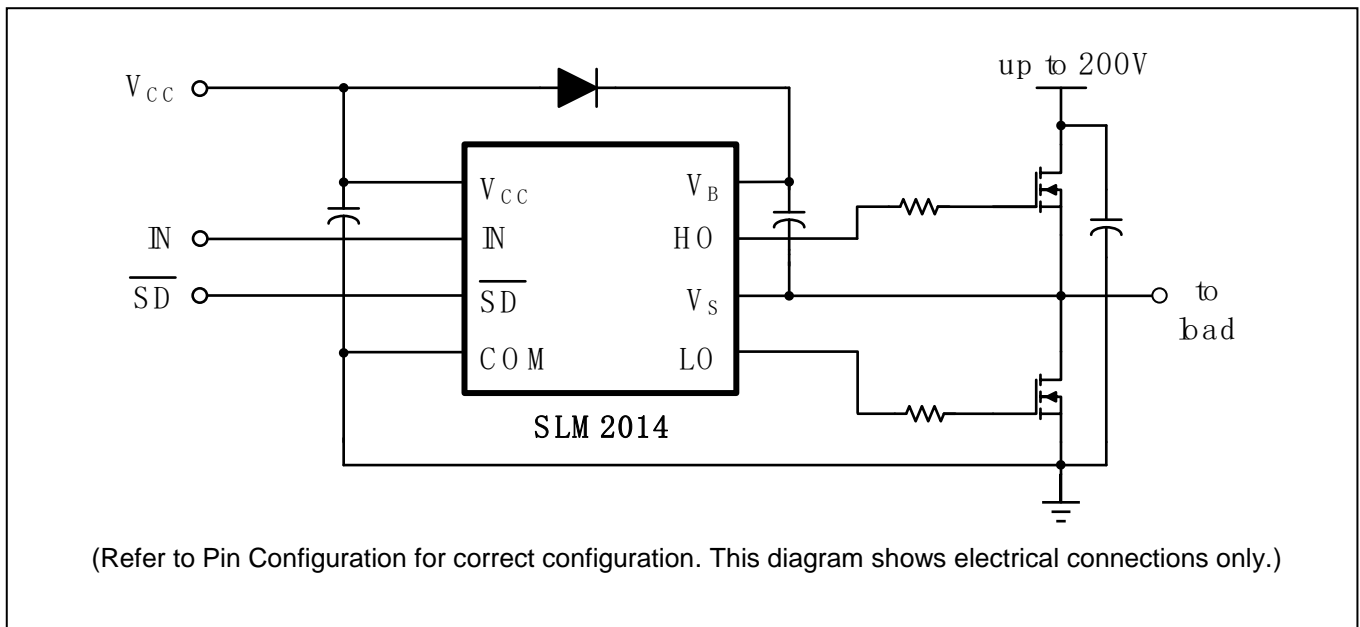
### GENERAL DESCRIPTION

The SLM2014 is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 200 V.

### FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage,  $dV/dt$  immune
- Gate drive supply range from 10 V to 18 V
- Undervoltage lockout
- 3.3 V, 5 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- RoHS compliant
- SOP8 package

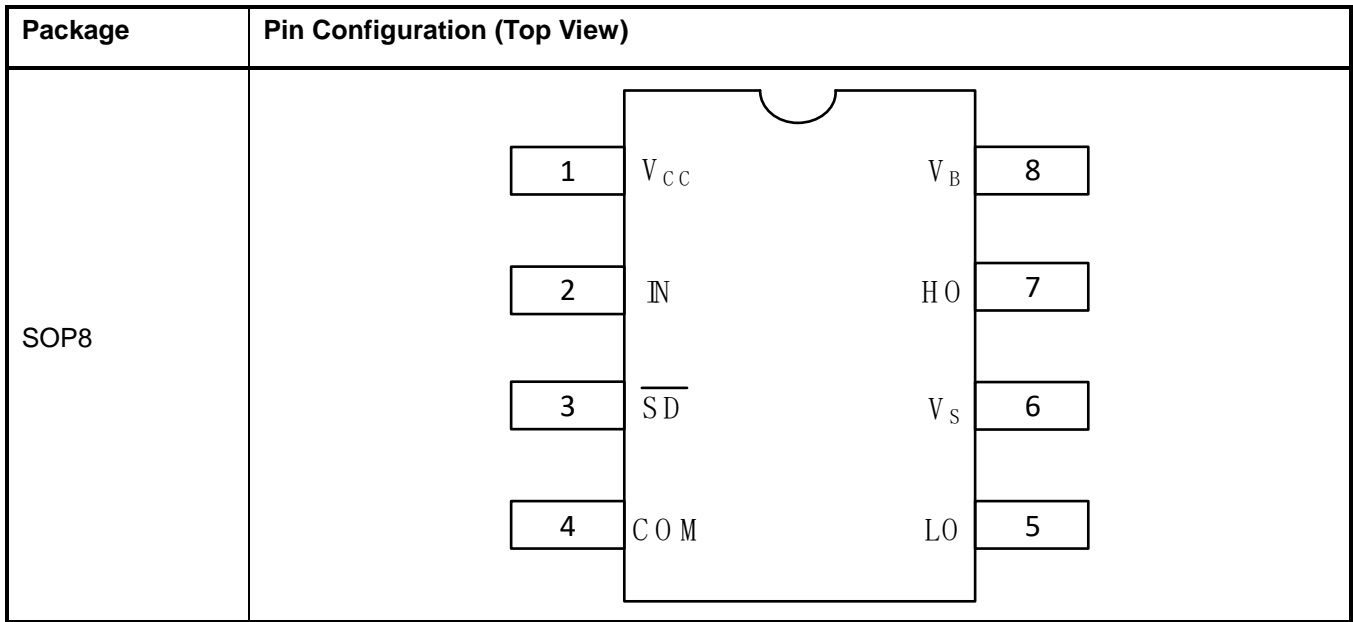
### TYPICAL APPLICATION CIRCUIT



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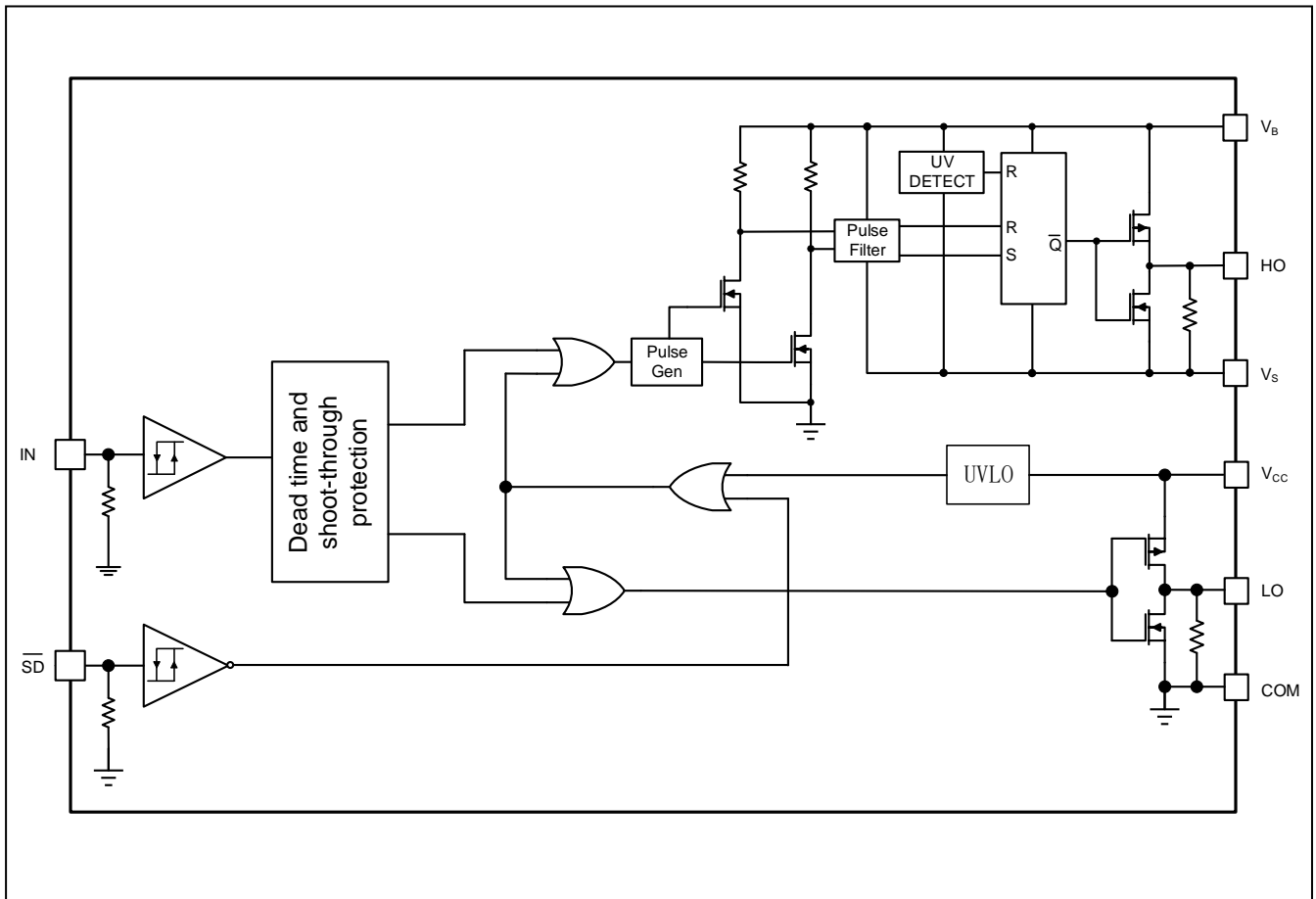
**PIN CONFIGURATION**

**PIN DESCRIPTION**

No.	Pin	Description
1	V <sub>CC</sub>	Low-side and logic fixed supply
2	IN	Logic input to control the high-side and low-side gate driver output (HO/LO). HO: In phase with IN. LO: Out of phase with IN.
3	$\overline{SD}$	Input logic for shutdown control. If $\overline{SD}$ is low, both high side and low side gate output is low.
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V <sub>S</sub>	High-side floating supply return
7	HO	High-side gate drive output
8	V <sub>B</sub>	High-side floating supply

**ORDERING INFORMATION**

Order Part No.	Package	QTY
SLM2014CA-DG	SOP8, Pb-Free	4000/Reel

**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min.	Max.	Units
$V_B$	High-side floating absolute voltage	-0.3	220	V
$V_S$	High-side floating supply offset voltage	$V_B - 20$	$V_B + 0.3$	
$V_{HO}$	High-side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
$V_{CC}$	Low-side and logic fixed supply voltage	-0.3	20	
$V_{LO}$	Low-side output voltage	-0.3	$V_{CC} + 0.3$	
$V_{IN}$	Logic input voltage (IN & $\overline{SD}$ )	-0.3	10	
$dV_S/dt$	Allowable offset supply voltage transient	---	50	V/ns
$P_D$	Package power dissipation at $T_A \leq +25^\circ\text{C}$	---	0.625	W
$\theta_{JA}$	Thermal resistance, junction to ambient	---	200	$^\circ\text{C/W}$
$T_J$	Junction temperature	-40	150	$^\circ\text{C}$
$T_S$	Storage temperature	-55	150	
$T_L$	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

**RECOMMENDED OPERATION CONDITIONS**

Symbol	Definition	Min.	Max.	Units
$V_B$	High-side floating absolute voltage	$V_S + 10$	$V_S + 18$	V
$V_S$	High-side floating supply offset voltage		200	
$V_{HO}$	High-side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low-side and logic fixed supply voltage	10	18	
$V_{LO}$	Low-side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage (IN & $\overline{SD}$ )	0	10	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

Note: For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at a 15 V differential.

## DYNAMIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S = 0$ V	---	260	370	ns
$t_{off}$	Turn-off propagation delay	$V_S = 0$ V	---	150	260	
$t_{SD}$	Shutdown propagation delay			140	260	
$t_r$	Turn-on rise time		---	25	50	
$t_f$	Turn-off fall time		---	10	25	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		50	110	220	

Note: See timing diagram in Figure 1, Figure 2, Figure 3, Figure 4 and Figure 5.

## STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	Logic "1" (IN) input voltage	$V_{CC} = 10$ V to 18V	2.5	---	---	V
	Logic "0" (SD) input voltage					
$V_{IL}$	Logic "0" (IN) input voltage		---	---	0.8	
	Logic "1" (SD) input voltage					
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_O = 20$ mA	---	0.16	0.3	
$V_{OL}$	Low level output voltage, $V_O$		---	0.07	0.15	
$I_{LK}$	Offset supply leakage current	$V_B = V_S = 200$ V	---	---	50	$\mu$ A
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_O = 0$ V	---	67	80	
$I_{QCC}$	Quiescent $V_{CC}$ supply current		---	200	230	
$I_{IN+}$	Logic "1" input bias current on IN	$V_{IN} = 5$ V	---	100	150	
	Logic "0" input bias current on $\overline{SD}$					
$I_{IN-}$	Logic "0" input bias current on IN	$V_{IN} = 0$ V	---	---	5	
	Logic "1" input bias current on $\overline{SD}$					
$V_{CCUV+}$	$V_{CC}$ supply under-voltage positive going threshold		8	8.8	9.8	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{CCUV-}$	$V_{CC}$ supply under-voltage negative going threshold		7.4	8.3	9	
$V_{BSUV+}$	$V_{BS}$ supply under-voltage positive going threshold			4.8		
$V_{BSUV-}$	$V_{BS}$ supply under-voltage negative going threshold			4.3		
$I_{O+}$	Output high short circuit pulsed current	$V_O = 0\text{ V}$ , $V_{IN} = V_{IH}$ $PW \leq 10\ \mu\text{s}$		1		A
$I_{O-}$	Output low short circuit pulsed current	$V_O = 15\text{ V}$ , $V_{IN} = V_{IL}$ $PW \leq 10\ \mu\text{s}$		1.5		

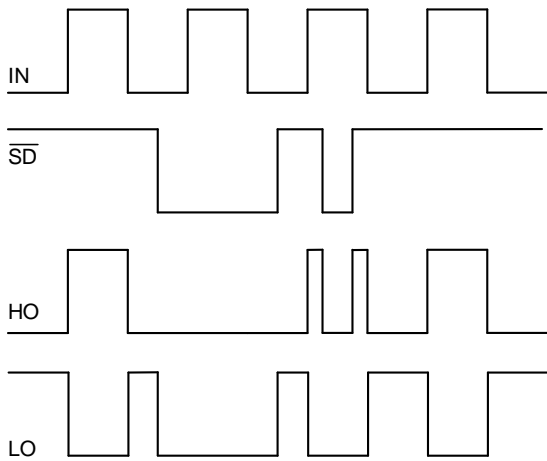


Figure 1. Input/Output Timing Diagram

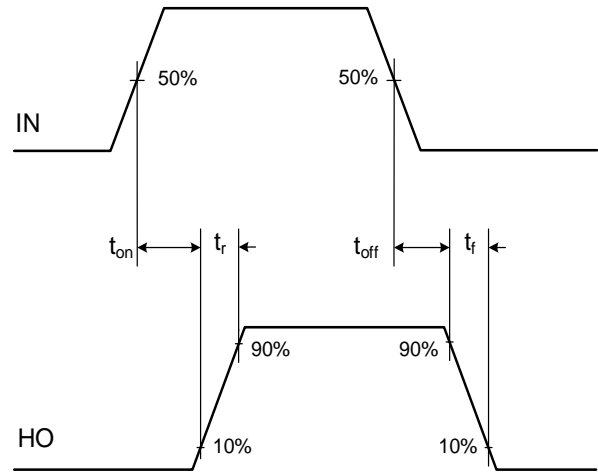


Figure 2. High Side Switching Time Waveform

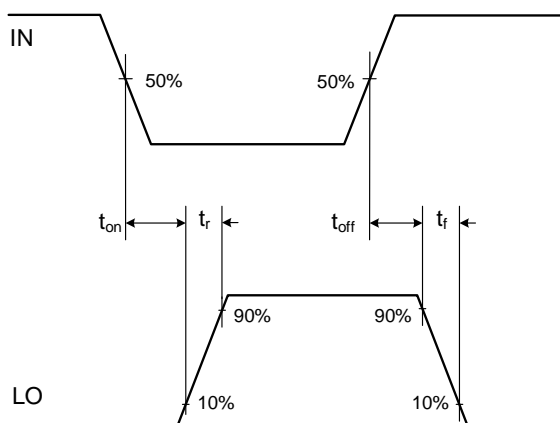


Figure 3. Low Side Switching Time Waveform

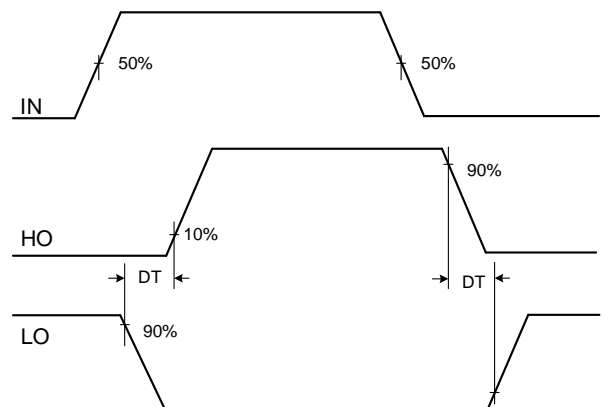


Figure 4. Dead Time Waveform

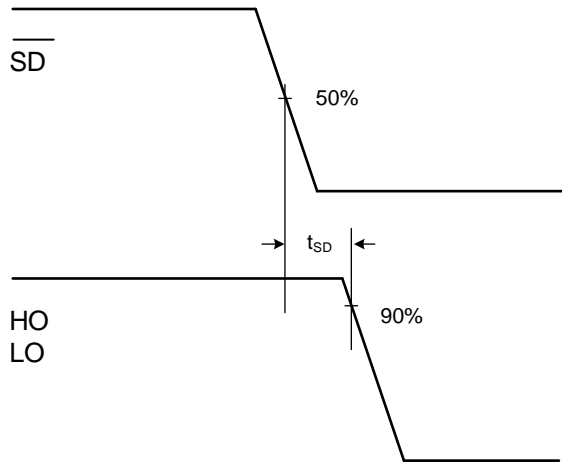


Figure 5. Shutdown Time Waveform



**PACKAGE CASE OUTLINES**

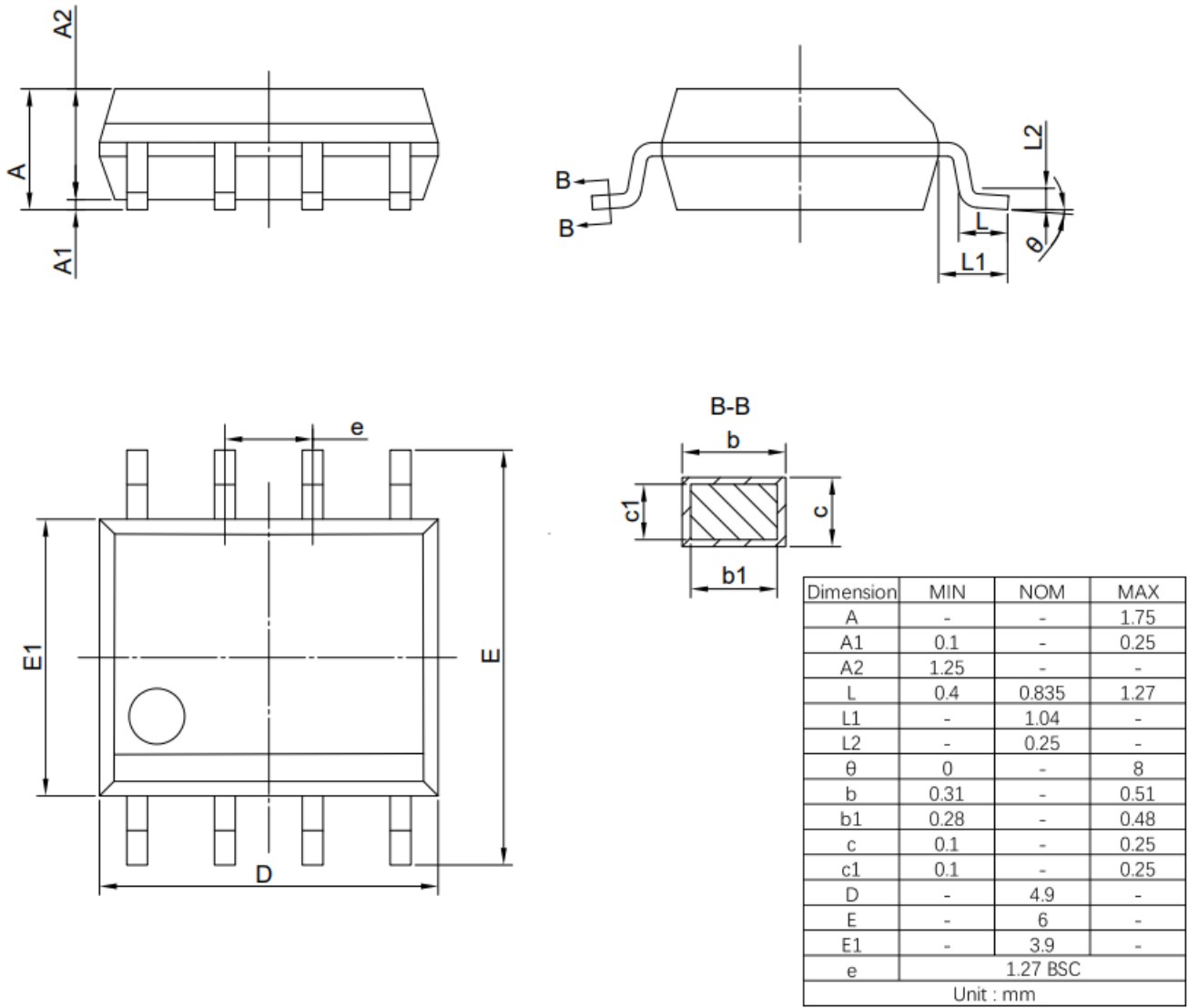


Figure 6. SOP8 Outline Dimensions

**REVISION HISTORY**

Note: page numbers for previous revisions may differ from page numbers in current version.

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>Rev 0.1 preliminary datasheet 2021-08-06</b>	
Whole document	Rev 0.1 Preliminary datasheet release
<b>Rev 1.0 datasheet 2022-05-16</b>	
Whole document	Rev 1.0 datasheet release
<b>Rev 1.1 Datasheet, 2022-12-29</b>	
Page 9	SOP8 Outline Dimensions Update

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