SLM2106S

600V Half Bridge Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 600 V max.
- **I_O+/-** 130 mA/270 mA
- **V_{OUT}** 10 V - 20 V
- **$t_{on/off}$ (typ.)** 220 ns/200 ns
- **Deadtime (typ.)** none

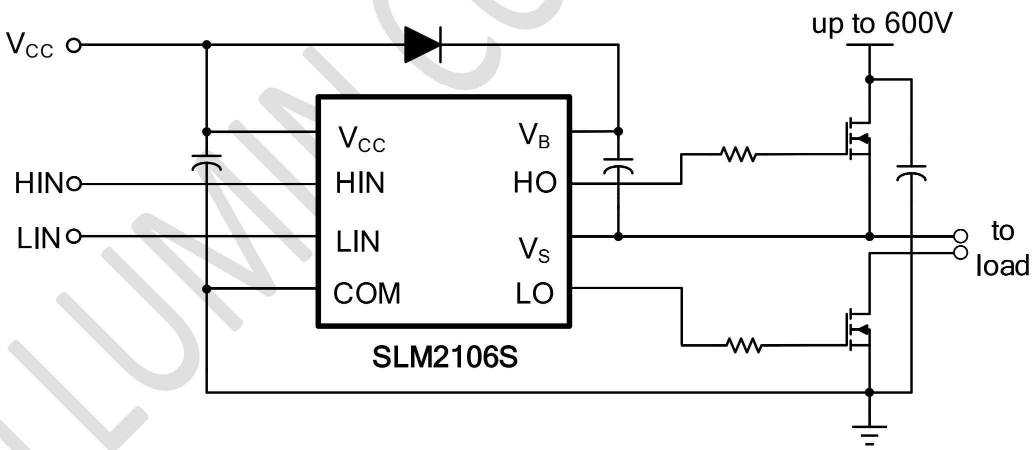
GENERAL DESCRIPTION

The SLM2106S is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- RoHS compliant
- SOIC8 and DIP8 package
- SOIC-14 package

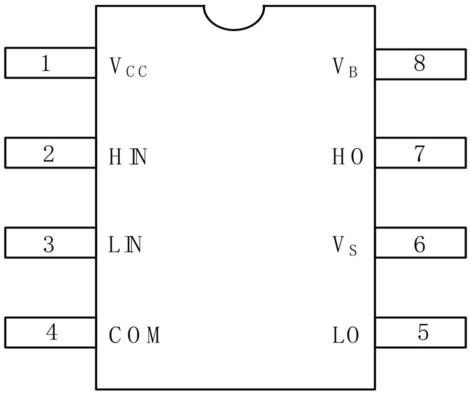
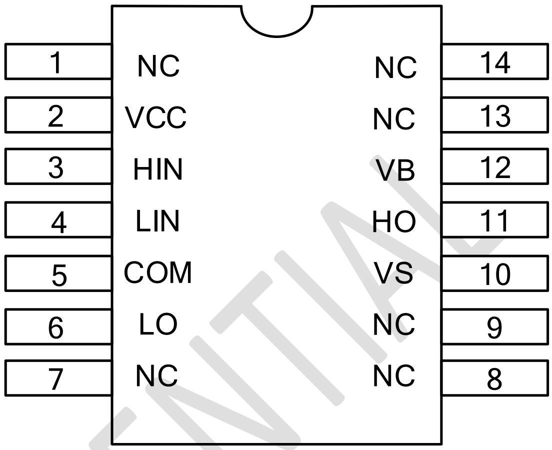
TYPICAL APPLICATION CIRCUIT



(Refer to Lead Assignments for correct configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Typical Application Circuit

PIN CONFIGURATION

Package	SOIC-8 and PDIP-8	SOIC-14
Pin Configuration (Top View)		

PIN DESCRIPTION

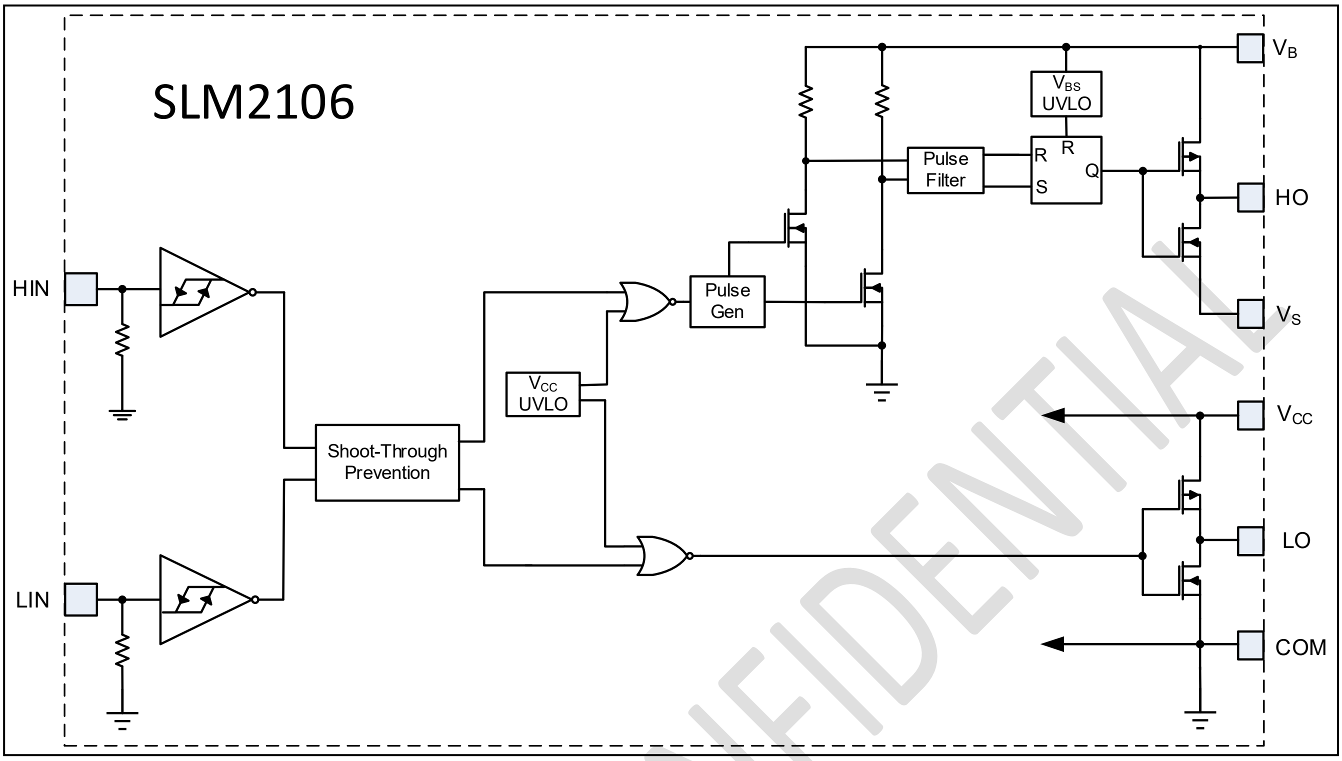
No.		Pin	Description
SOIC-8 and PDIP-8	SOIC-14		
1	2	V_{CC}	Low-side and logic fixed supply
2	3	HIN	Logic input for high-side gate driver output (HO), in phase
3	4	LIN	Logic input for low-side gate driver output (LO), in phase
4	5	COM	Low-side return
5	6	LO	Low-side gate drive output
6	10	V_S	High-side floating supply return
7	11	HO	High-side gate drive output
8	12	V_B	High-side floating supply
	1,7,8,9, 13,14	NC	Floating, no internal connection

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2106SCA-13GTR	SOIC8, Pb-Free	2500/Reel
SLM2106SCA-GT	SOIC8, Pb-Free	100/Tube
SLM2106SDA-GT	PDIP8, Pb-Free	100/Tube
SLM2106SCJ-13GTR	SOIC14, Pb-Free	4000/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant$ +25°C	PDIP-8	---	1.0	W
		SOIC-8	---	0.625	
		SOIC-14		0.892	
Rth_{JA}	Thermal resistance, junction to ambient	PDIP-8	---	125	°C/W
		SOIC-8	---	200	
		SOIC-14		140	
T_J	Junction temperature		---	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

Note:
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATIONG CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage	Note 1	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	V_{CC}	
T_A	Ambient temperature	- 40	125	°C

Note:
The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	220	300	ns
t_{off}	Turn-off propagation delay	V_S = 0 V or 600 V	---	200	280	
t_r	Turn-on rise time	V_S = 0 V	---	100	220	
t_f	Turn-off fall time		---	35	80	
MT	Delay matching, HS & LS turn-on/off		---	0	30	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10 V to 20V	2.5	---	---	V
V_{IL}	Logic "0" input voltage		---	---	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2 mA	---	0.05	0.2	
V_{OL}	Low level output voltage, V_O		---	0.02	0.1	
I_{LK}	Offset supply leakage current	V_B = V_S = 600 V	---	---	50	μA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V or 5 V	20	75	130	
I_{QCC}	Quiescent V_{CC} supply current		60	120	180	
I_{IN+}	Logic "1" input bias current V_{IN} = 5 V		---	5	20	
I_{IN-}	Logic "0" input bias current V_{IN} = 0 V		---	---	5	
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold		8.0	8.9	9.8	V
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold		7.4	8.2	9.0	
I_{O+}	Output high short circuit pulsed current	V_O = 0 V, PW ≤ 10 μs	130	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15 V, PW ≤ 10 μs	270	600		

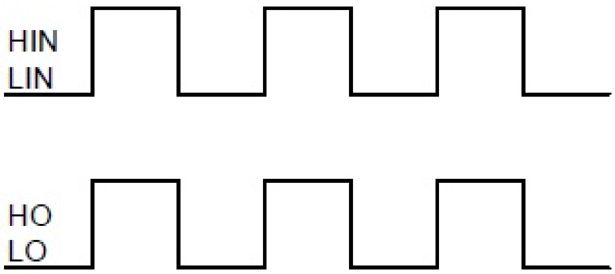


Figure 1. Input/Output Timing Diagram

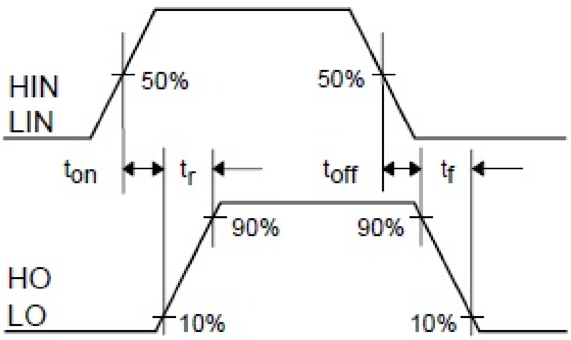


Figure 2. Switching Time Waveform Definitions

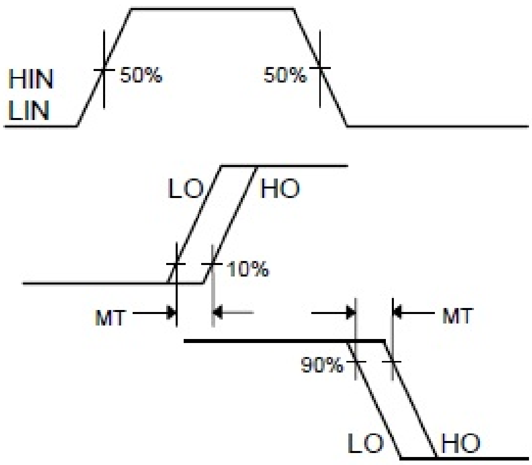


Figure 3. Delay Matching Waveform Definitions

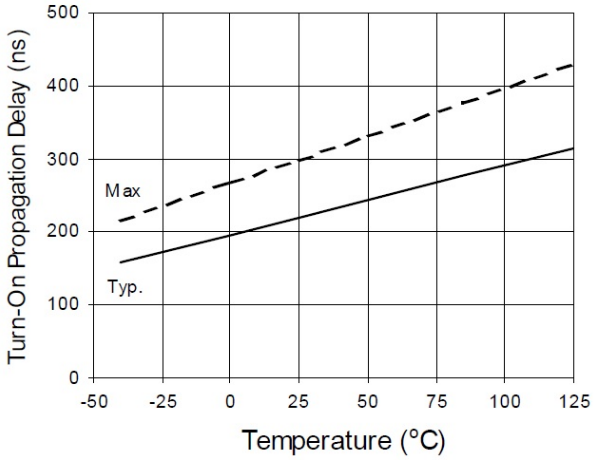


Figure 4A. Turn-On Propagation Delay vs. Temperature

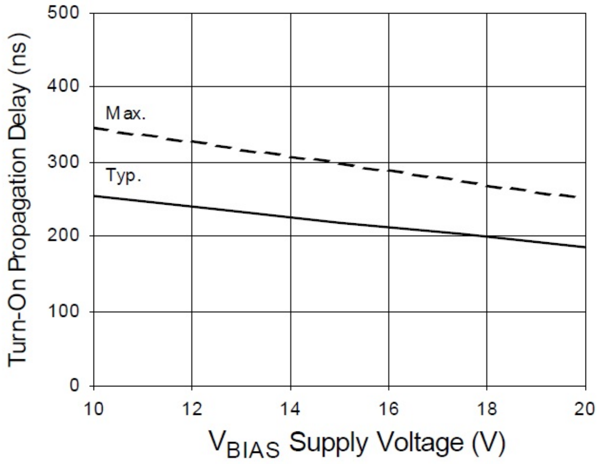


Figure 4B. Turn-On Propagation Delay vs. Supply Voltage

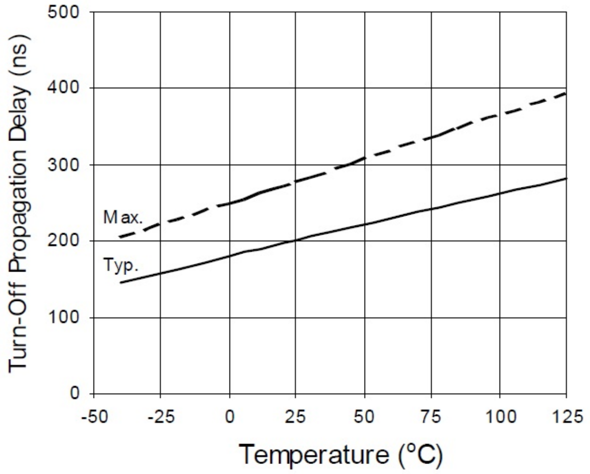


Figure 5A. Turn-Off Propagation Delay vs. Temperature

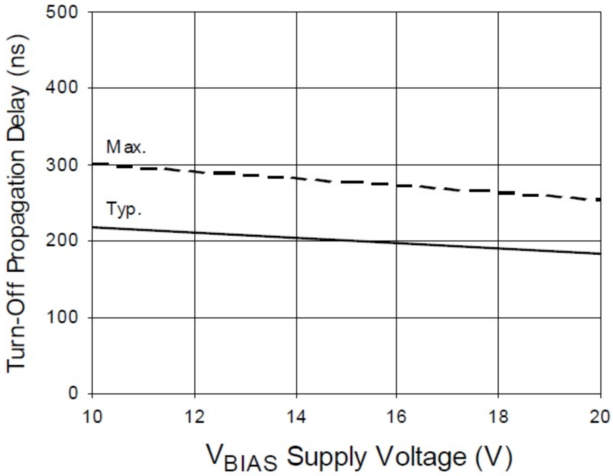


Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage

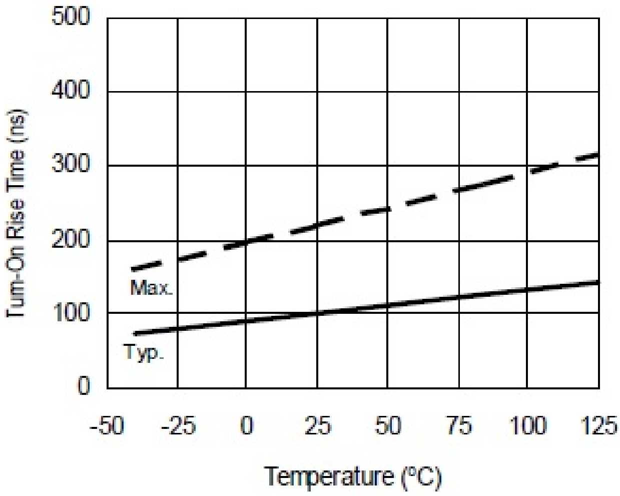


Figure 6A. Turn-On Rise Time vs. Temperature

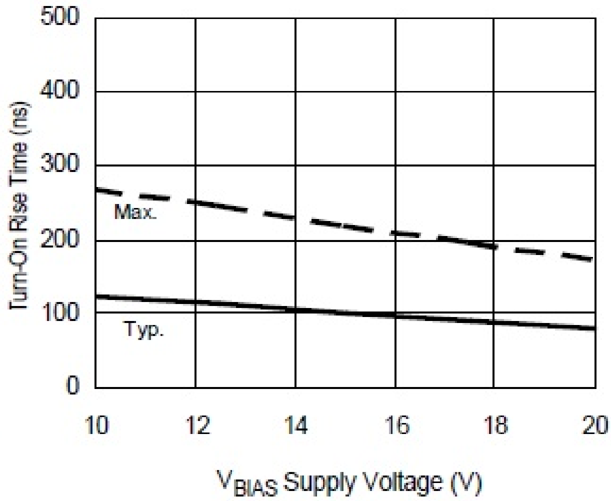


Figure 6B. Turn-On Rise Time vs. Supply Voltage

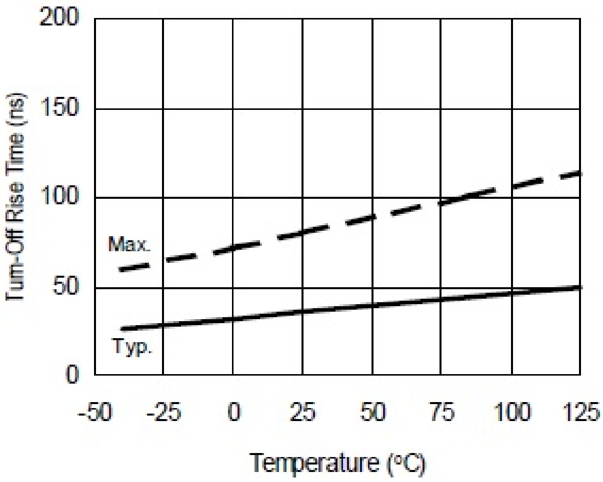


Figure 7A. Turn-Off Fall Time vs. Temperature

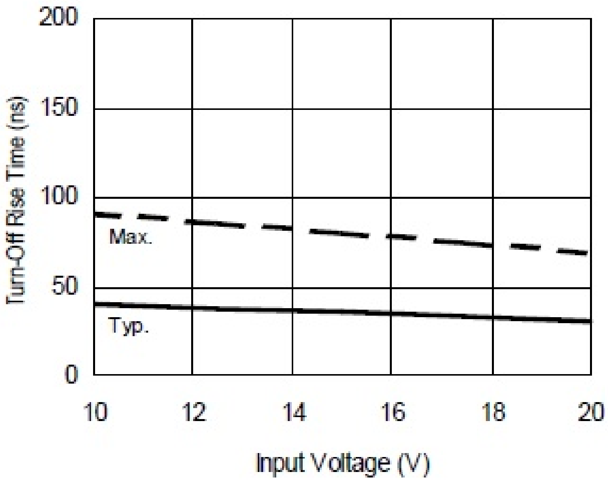


Figure 7B. Turn-Off Fall Time vs. Supply Voltage

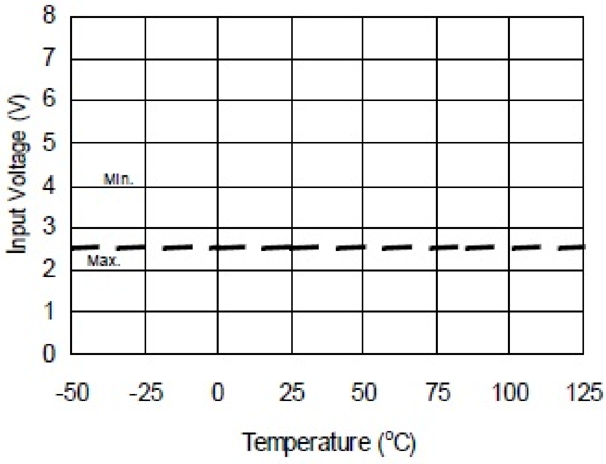


Figure 8A. Logic "1" Input Voltage vs. Temperature

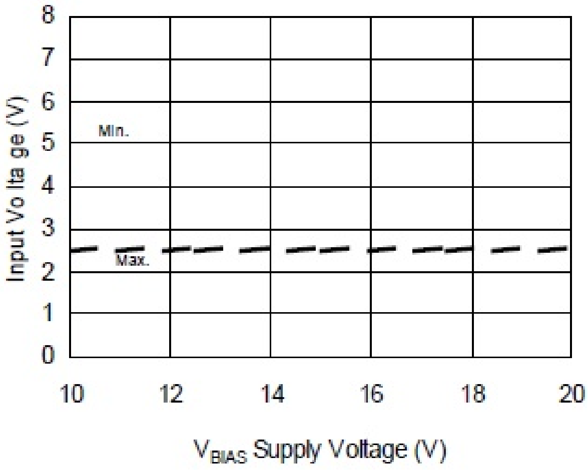


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

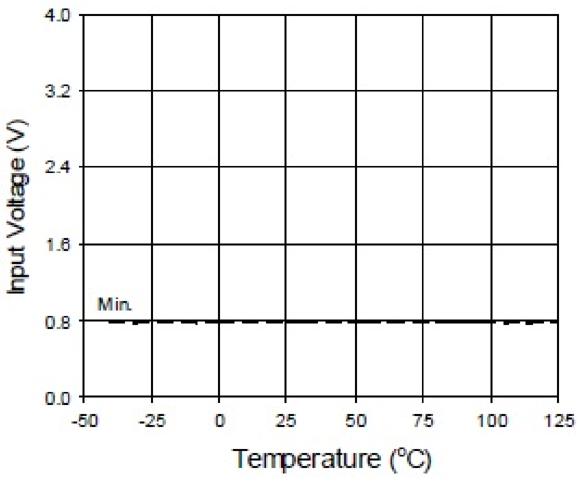


Figure 9A. Logic "0" Input Voltage vs. Temperature

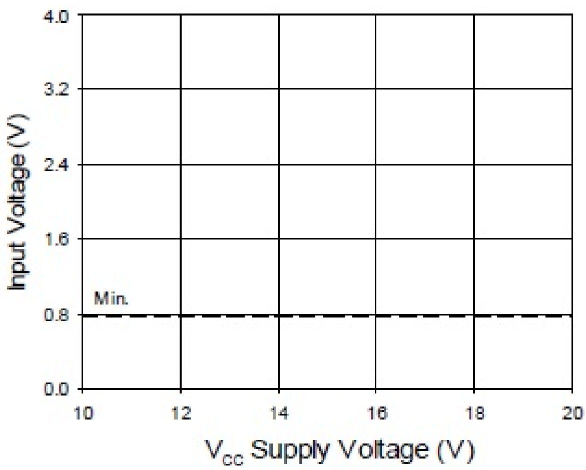


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

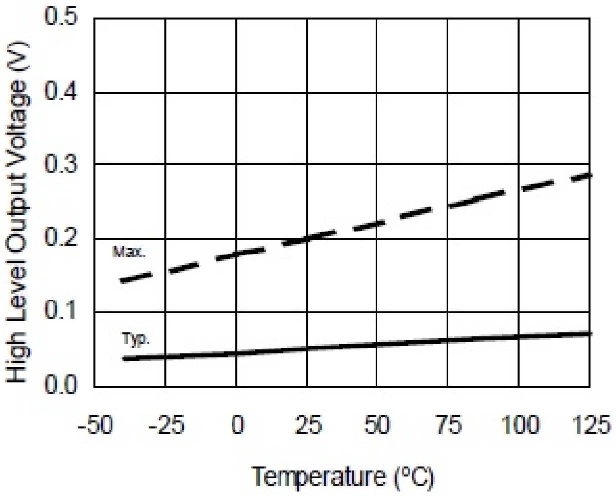


Figure 10A. High Level Output Voltage vs. Temperature

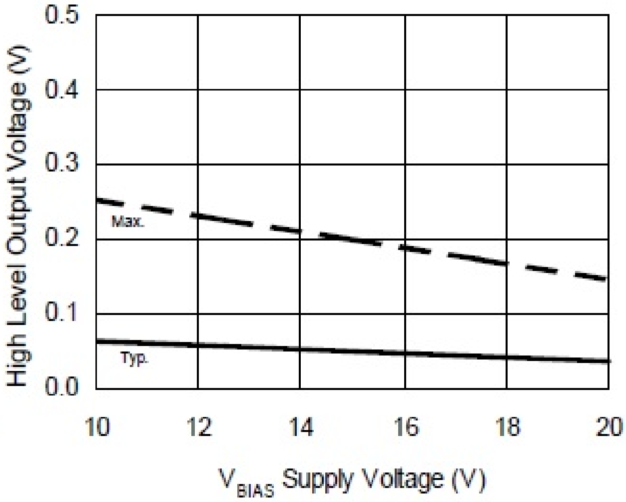


Figure 10B. High Level Output Voltage vs. Supply Voltage

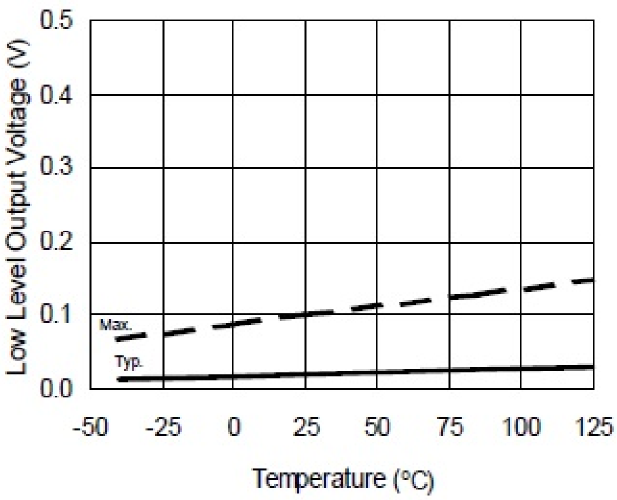


Figure 11A. Low Level Output Voltage vs. Temperature

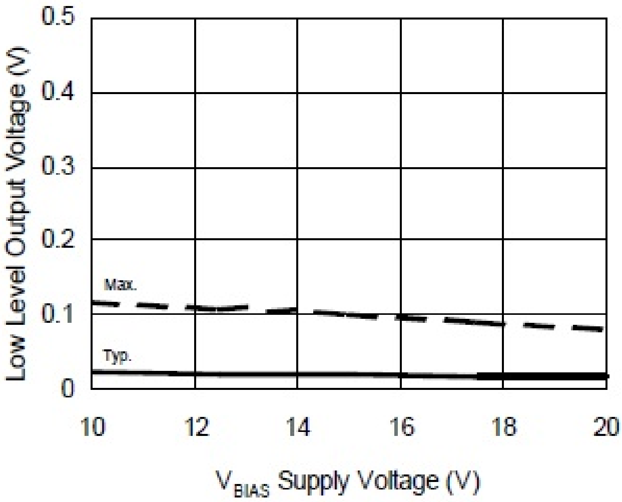


Figure 11B. Low Level Output Voltage vs. Supply Voltage

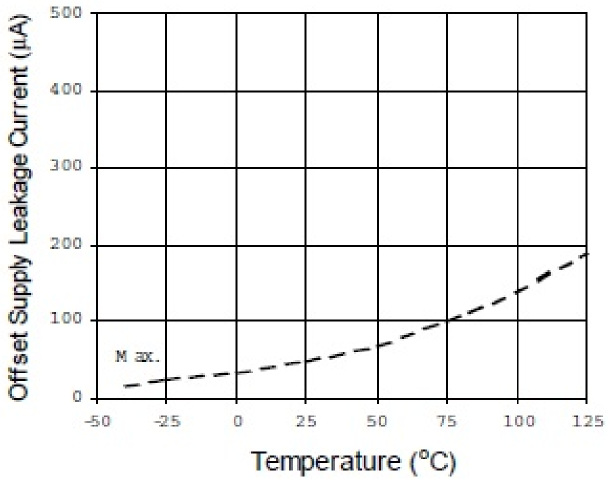


Figure 12A. Offset Supply Leakage Current vs. Temperature

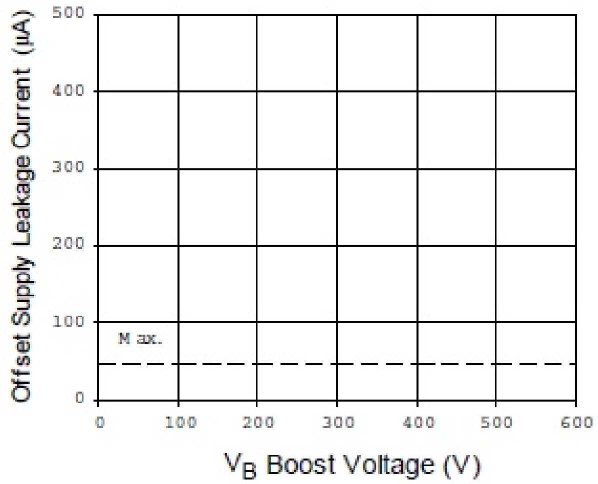


Figure 12B. Offset Supply Leakage Current vs. Supply Voltage

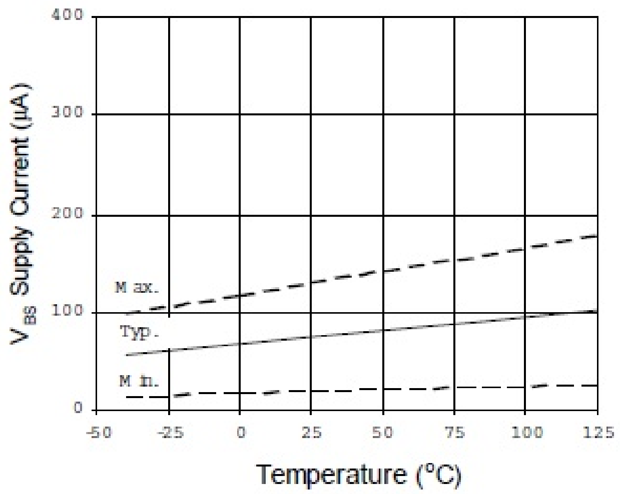


Figure 13A. V_{BS} Supply Current vs. Temperature

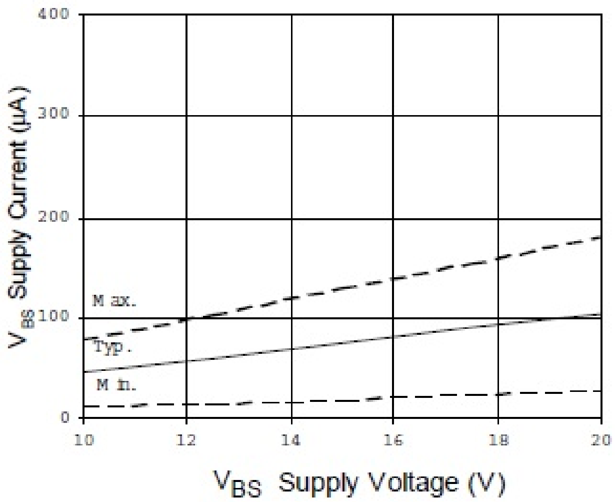


Figure 13B. V_{BS} Supply Current vs. Supply Voltage

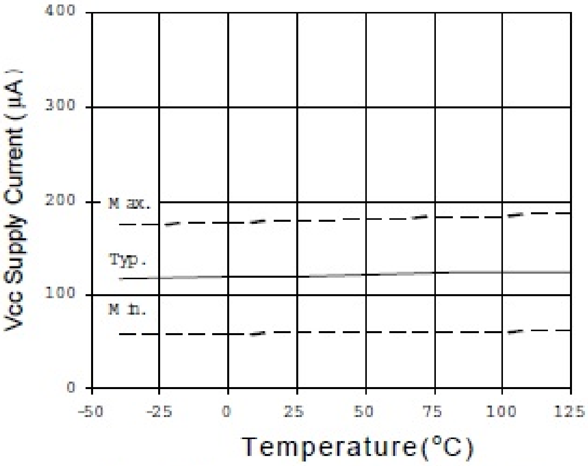


Figure 14A. Quiescent V_{CC} Supply Current vs. Temperature

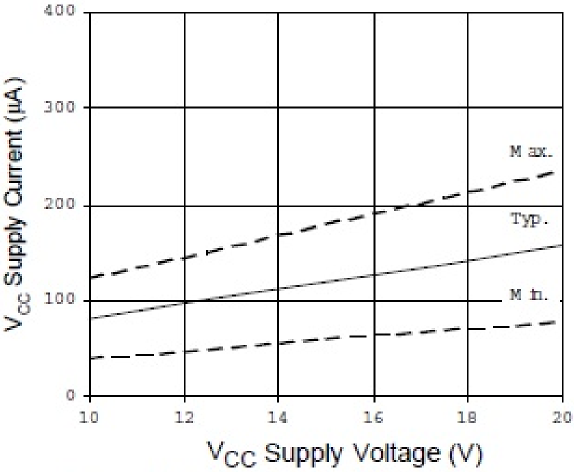


Figure 14B. Quiescent V_{CC} Supply Current vs. V_{CC} Supply Voltage

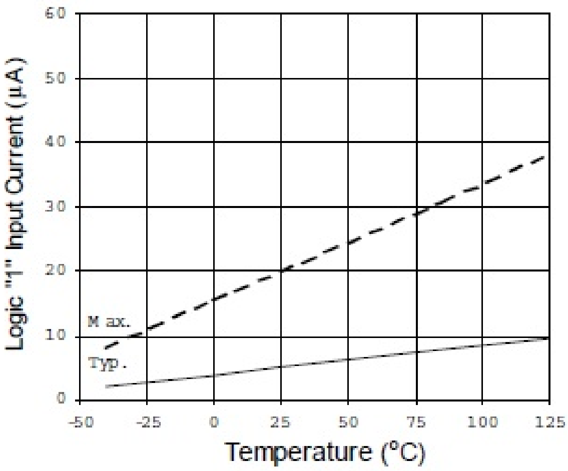


Figure 15A. Logic “1” Input Current vs. Temperature

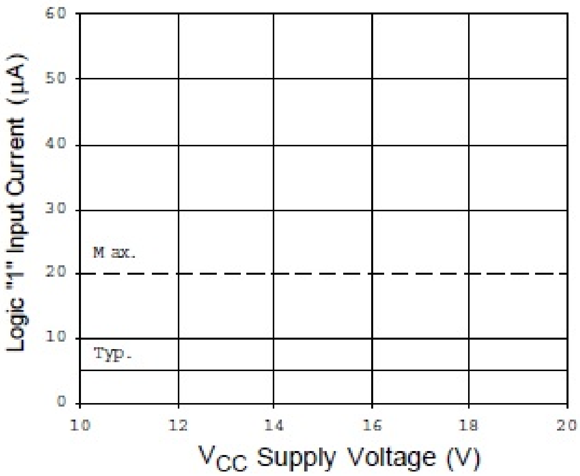


Figure 15B. Logic “1” Bias Current vs. Supply Voltage

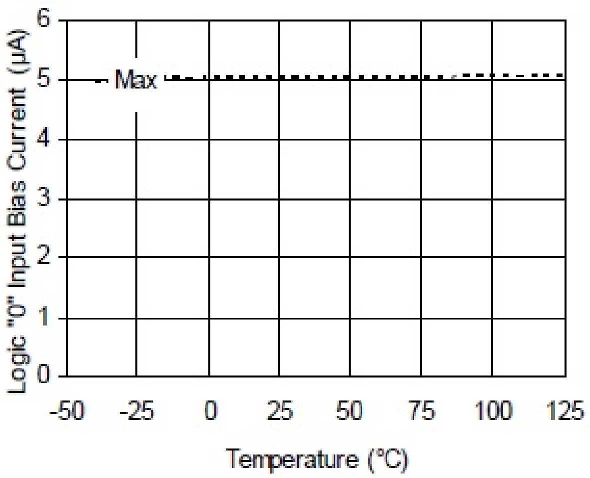


Figure 16A. Logic "0" Input Bias Current vs. Temperature

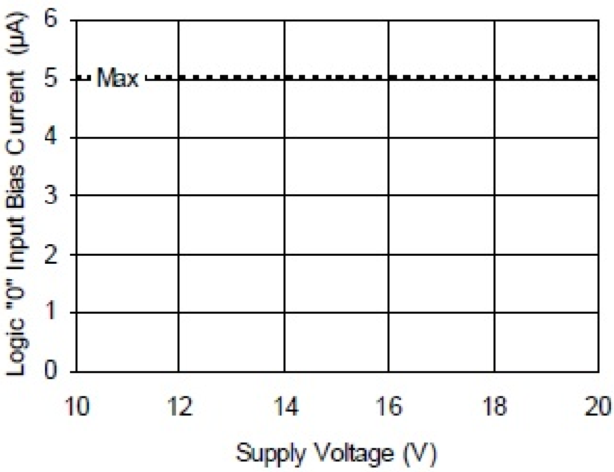


Figure 16B. Logic "0" Input Bias Current vs. Voltage

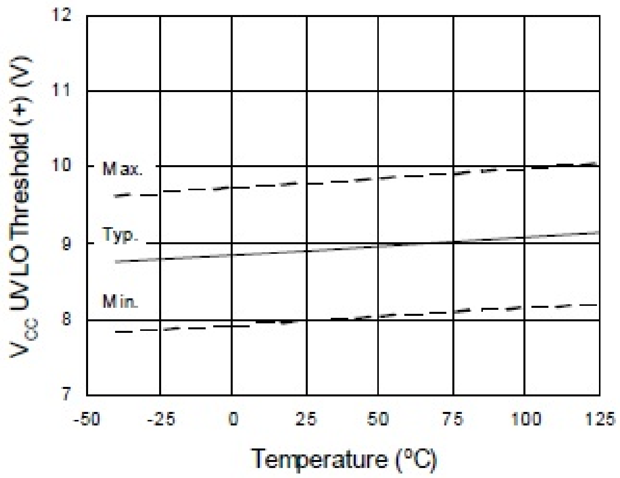


Figure 17. V_{CC} Undervoltage Threshold (+) vs. Temperature

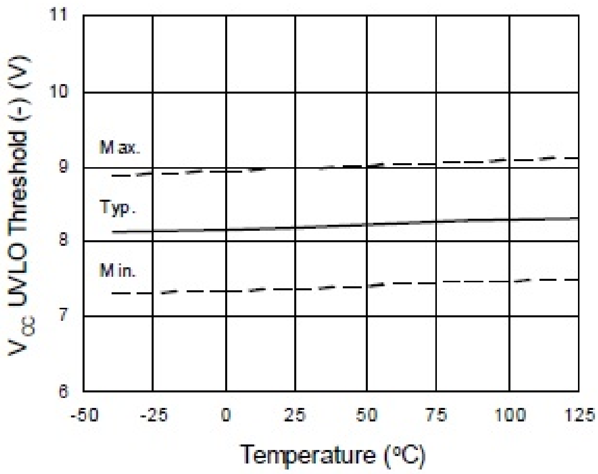


Figure 18. V_{CC} Undervoltage Threshold (-) vs. Temperature

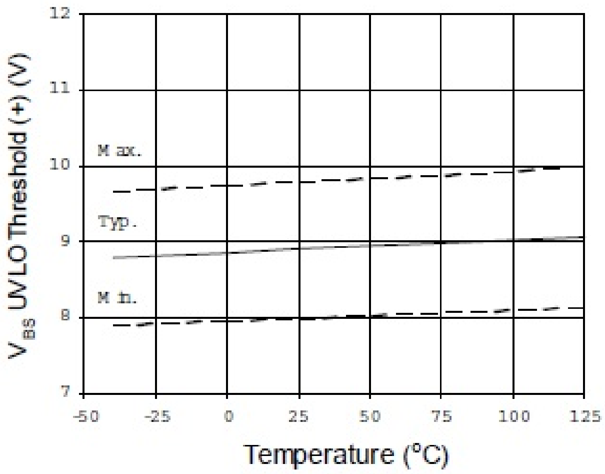


Figure 19. V_{BS} Undervoltage Threshold (+) vs. Temperature

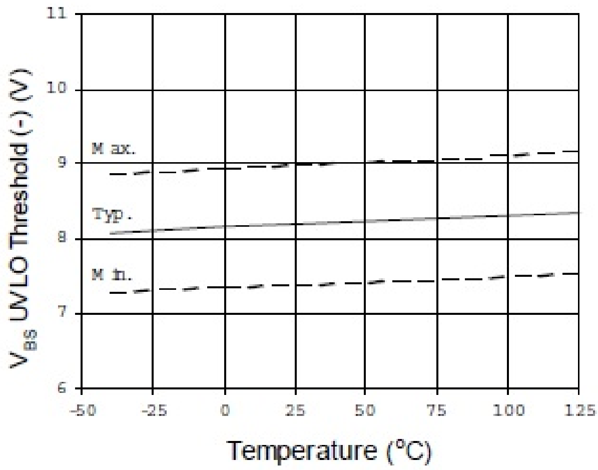


Figure 20. V_{BS} Undervoltage Threshold (-) vs. Temperature

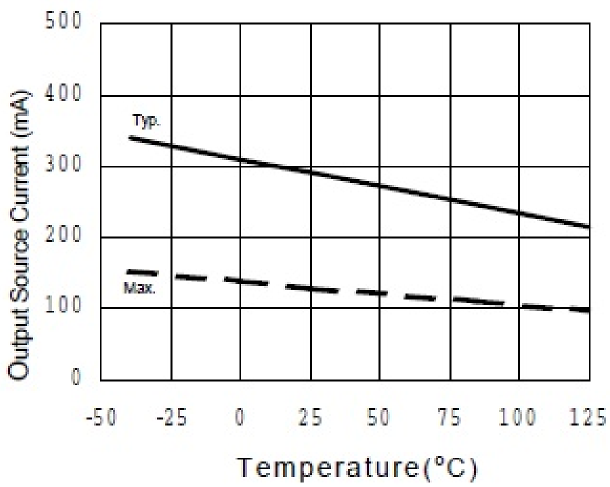


Figure 21A. Output Source Current vs. Temperature

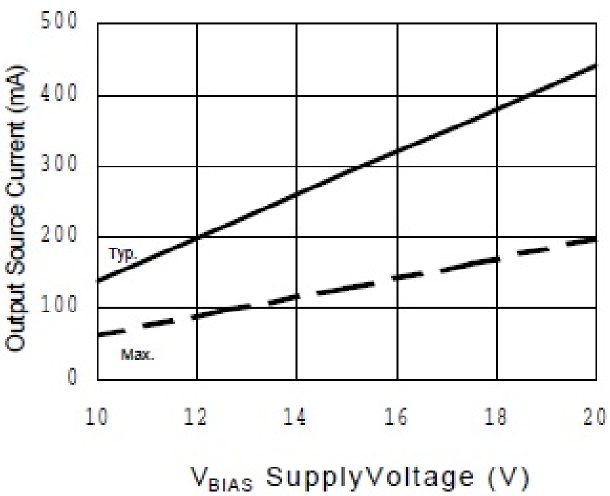


Figure 21B. Output Source Current vs. Supply Voltage

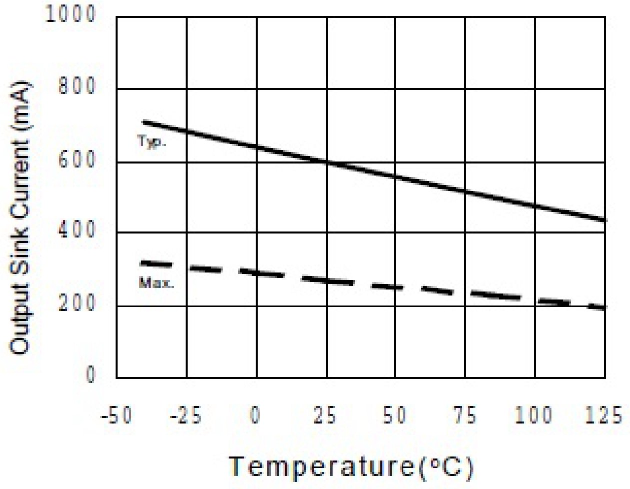


Figure 22A. Output Sink Current vs. Temperature

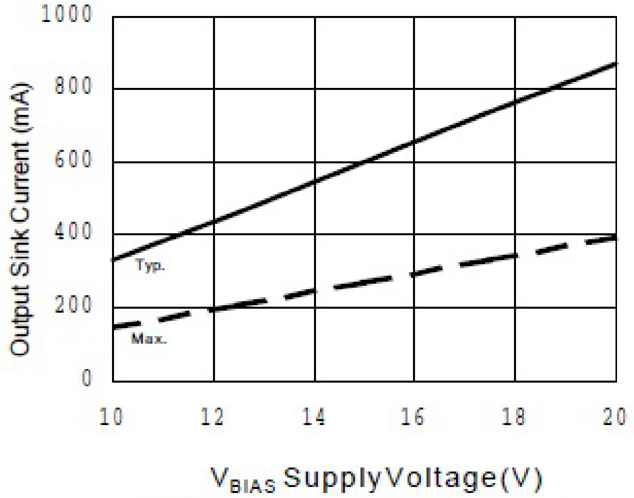


Figure 22B. Output Sink Currentt vs. Supply Voltage

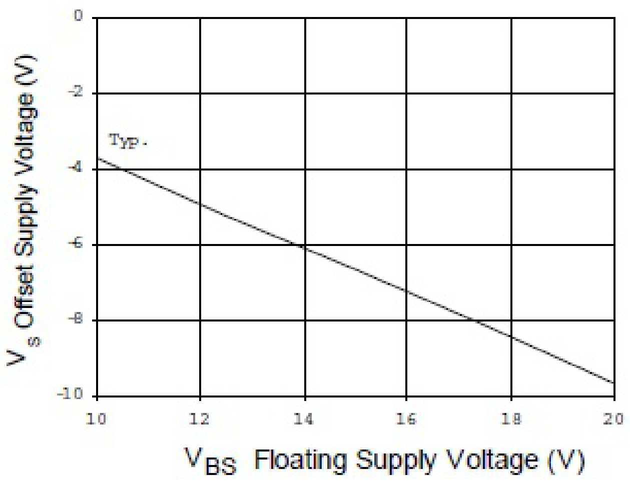
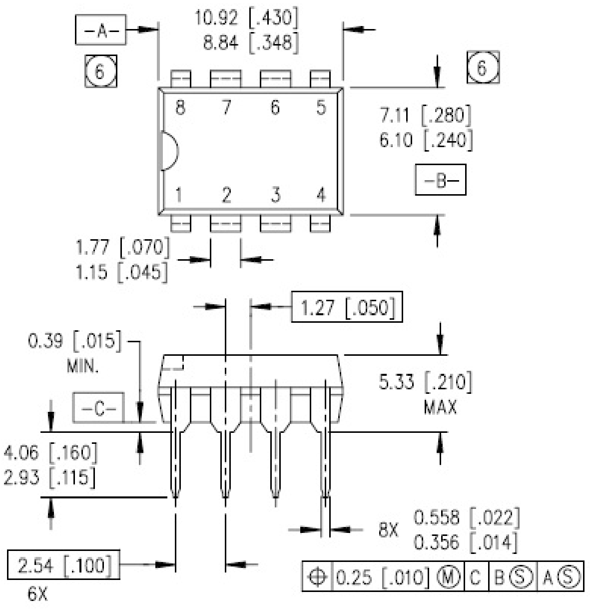


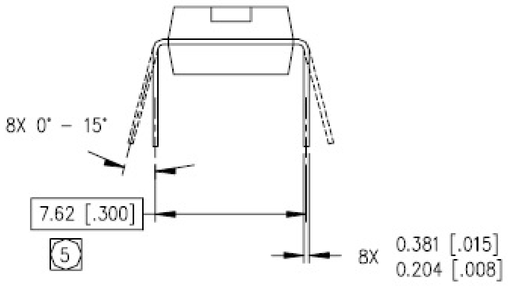
Figure 23. Maximum V_S Negative Offset vs. Supply Voltage

PACKAGE CASE OUTLINES



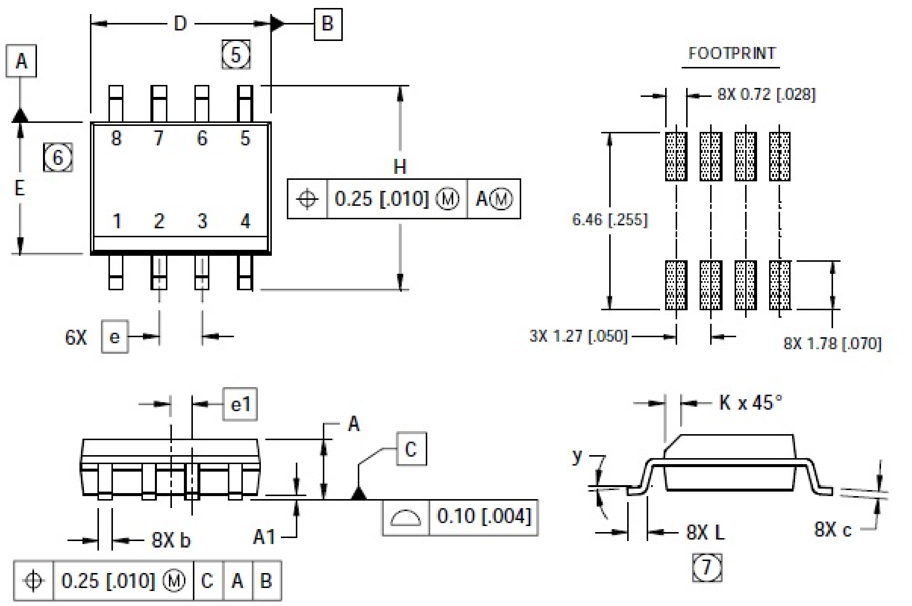
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



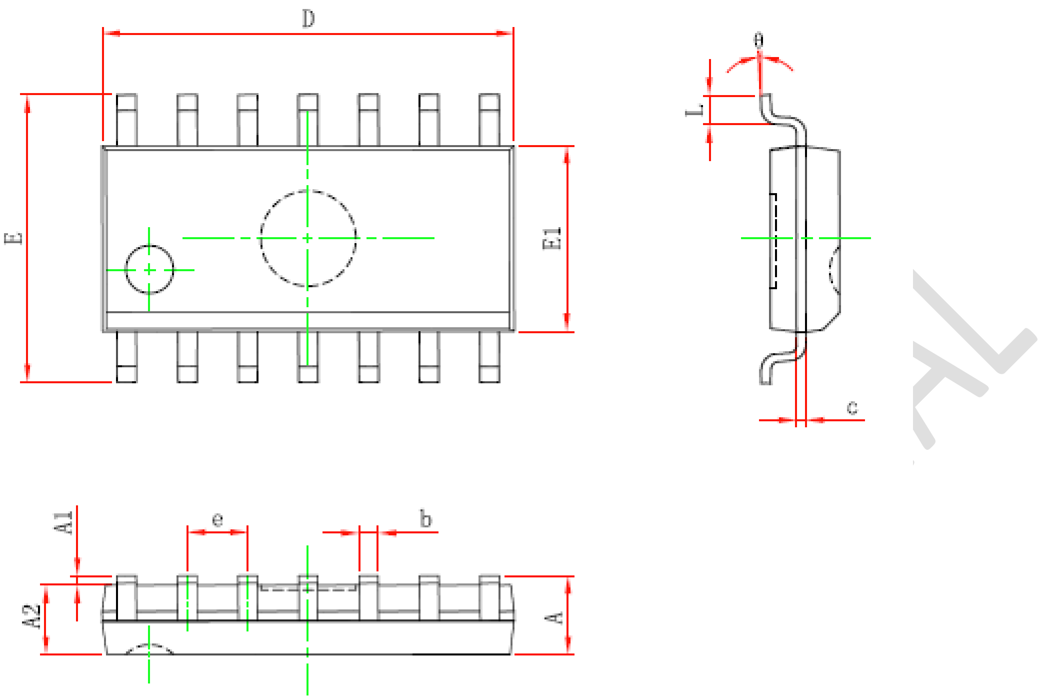
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

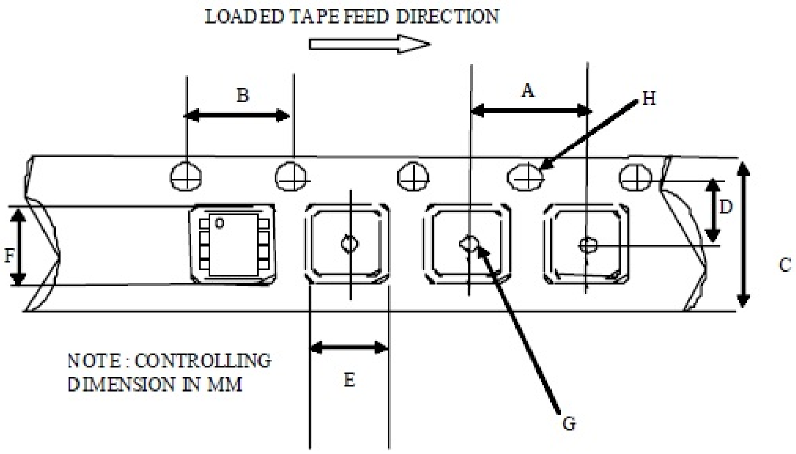


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

14-Lead SOIC

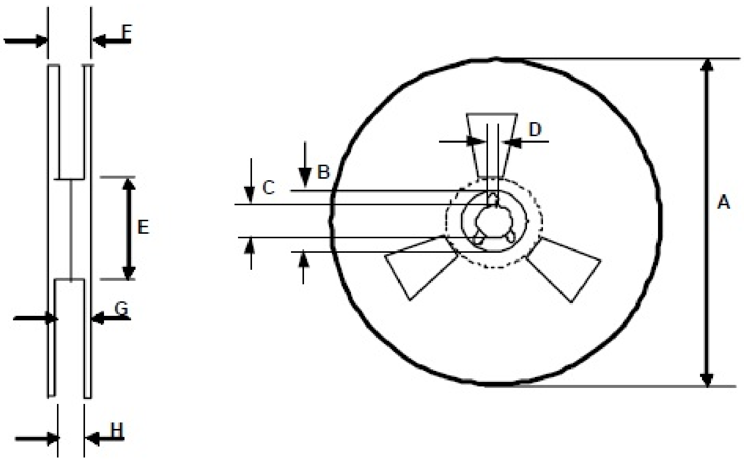
TAPE AND REEL INFORMATION

Tape & Reel
8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

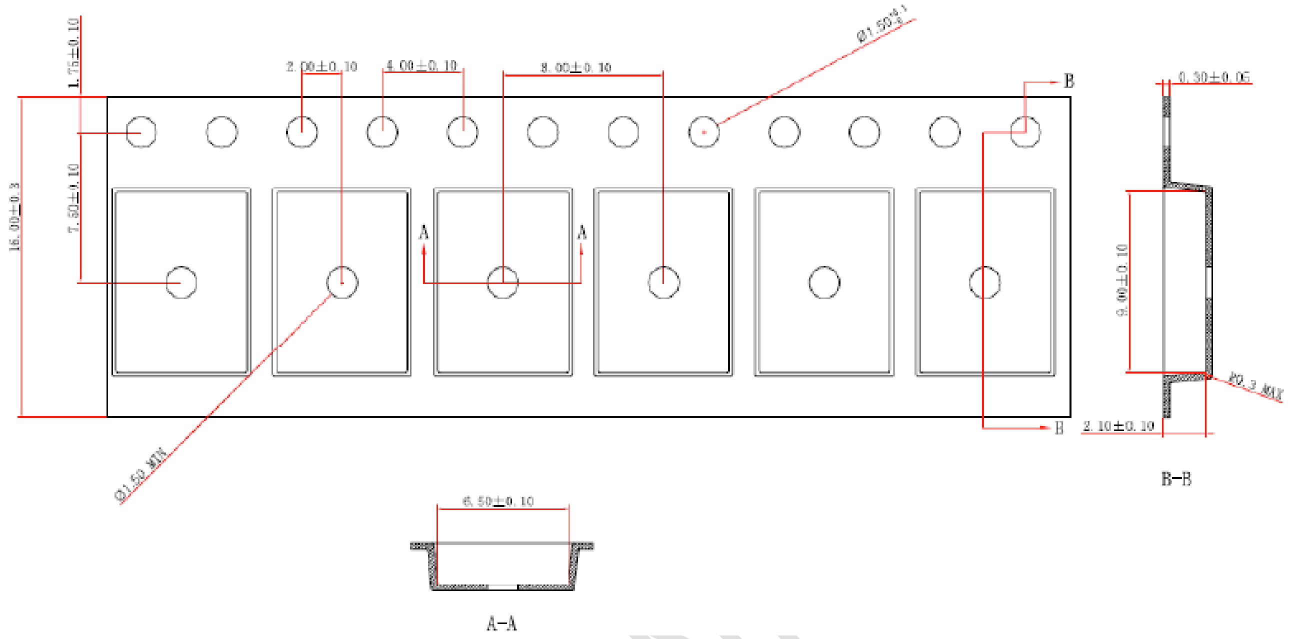
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

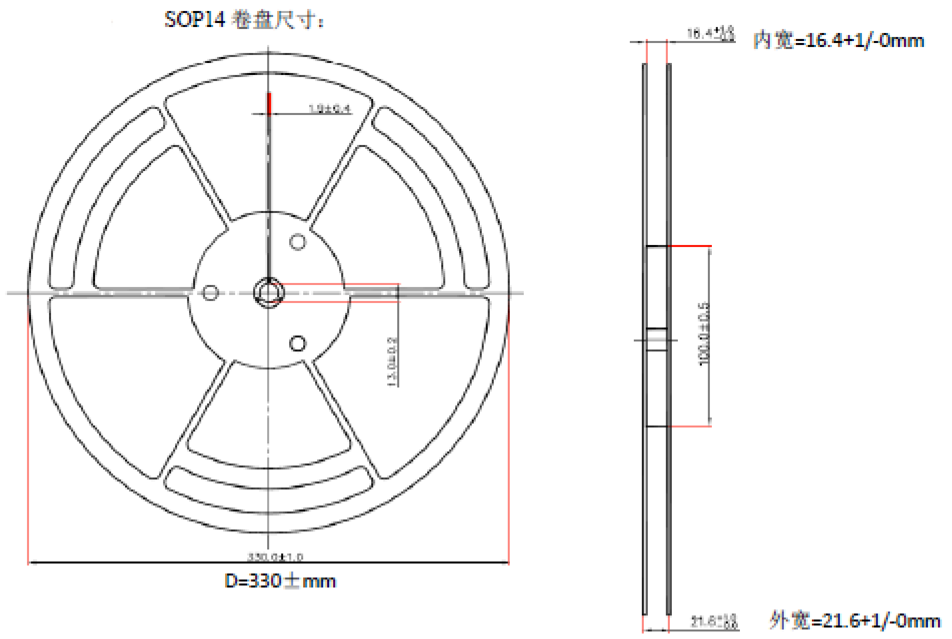


REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Reel
14-lead SOIC


1.75±0.10
2.00±0.10
4.00±0.10
8.00±0.10
B
0.30±0.05
16.00±0.3
7.50±0.10
A
A
9.00±0.10
2.10±0.10
B
B-B
6.50±0.10
A-A


SOP14 卷盘尺寸：
内宽=16.4+1/-0mm
D=330±mm
外宽=21.6+1/-0mm

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Remove “Figure 1. ” and “May 2019”
Rev 1.1 datasheet, 2019-10-21	
Page 1	Change “high side and low side driver” to “600V half bridge driver”
Page 1	Change “independent” to “dependent”