

## Dual-Channel, High-Speed, Low-Side Gate Driver

### GENERAL DESCRIPTION

The SLM2752x family of devices are dual-channel, high-speed, low-side gate drivers that can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, SLM2752x can source and sink high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay, typically 18 ns.

The SLM2752x provides 4.5 A source, 5.5 A sink peak drive current capability at 12V VDD supply.

### APPLICATIONS

- Switching mode power supplies
- DC-to-DC converters
- Motor Control, solar power
- Gate driver for emerging wide band-gap power devices such as GaN

### FEATURES

- Two independent gate drive channels
- 4.5 A peak source and 5.5 A peak sink current drive capability
- Fast propagation delay (18 ns typical)
- Fast rise and fall time (7 ns and 6 ns typical)
- 4.5 to 20V single supply range
- Under-voltage lockout
- TTL and CMOS compatible input logic threshold
- Ability to handle negative voltages (-5V) at inputs
- 2 ns typical delay matching between 2 channels
- Two outputs are paralleled for higher drive current
- Outputs held in low when inputs floating
- Operating temperature range of -40°C to 140°C
- SOP8 and MSOP8-EP package options

### TYPICAL APPLICATION CIRCUIT

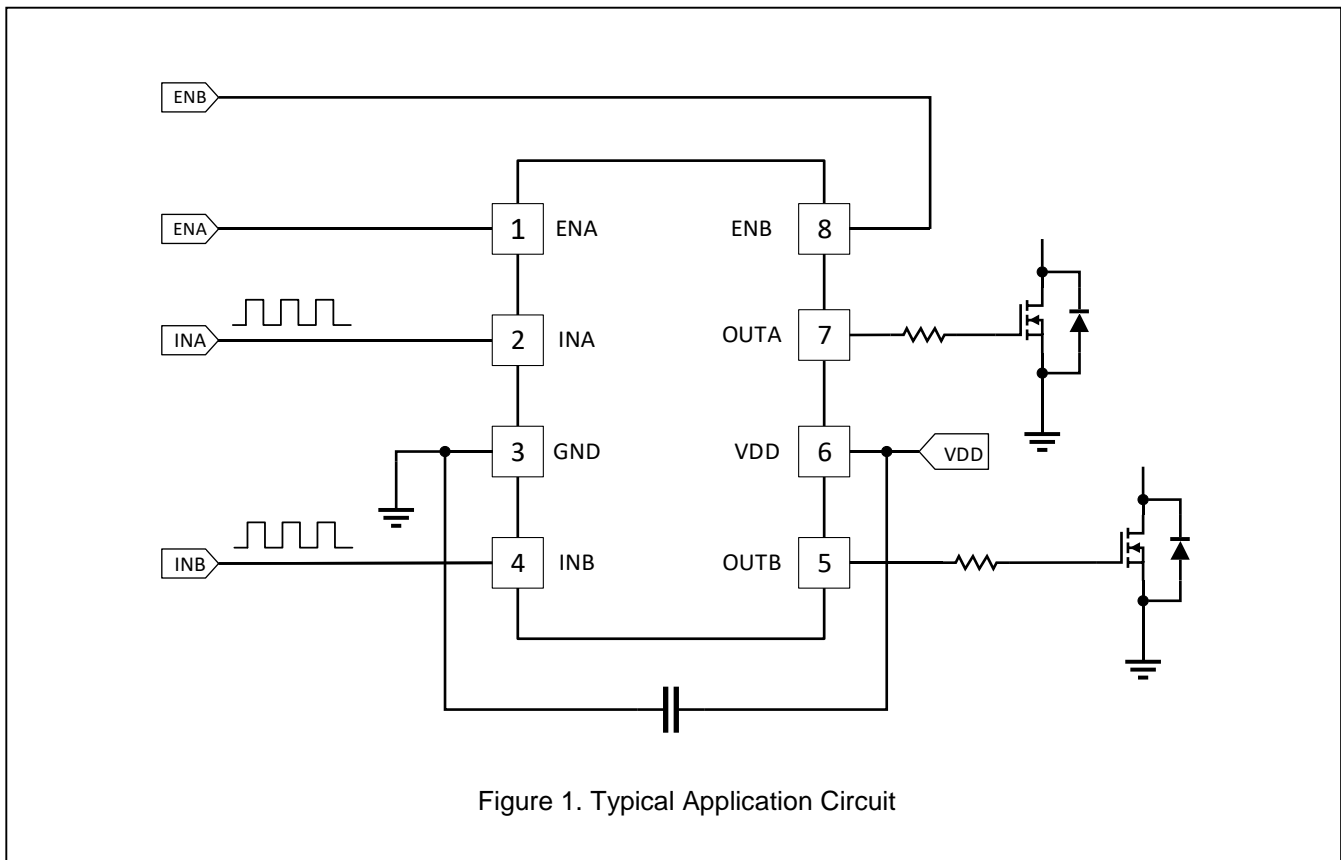


Figure 1. Typical Application Circuit

**Table of Contents**

General Description.....	1
Applications.....	1
Features.....	1
Typical Application Circuit .....	1
PIN Configuration.....	3
PIN Description .....	3
Functional Block Diagram.....	4
Absolute Maximum Ratings <sup>1,2,3</sup> .....	5
Recommended Operation Conditions .....	5
Thermal Resistance.....	5
Ordering Information.....	6
Dynamic Electrical Characteristics .....	7
Static Electrical Characteristics.....	7
Typical Performance Characteristic.....	9
Feature Description .....	12
VDD and Under-Voltage Lockout .....	12
Input Stage .....	12
Enable Function.....	12
Output Stage .....	12
Package Case Outlines .....	13
Revision History.....	14

## PIN CONFIGURATION

Package	Pin Configuration (Top View)		
	SLM27523	SLM27524	SLM27525
	Dual Inverting Inputs	Dual Non-Inverting Inputs	One Inverting and One Non-Inverting Input
SOP8 /MSOP8-EP			

## PIN DESCRIPTION

No.	Pin	Description
1	ENA	Enable input for channel A: ENA is biased LOW to disable the channel A output regardless of the INA state. ENA is biased HIGH or left floating to enable the channel A output. ENA is allowed to float.
2	INA	Input to channel A: Inverting input in the SLM27523 and SLM27525. Non-Inverting input in the SLM27524. OUTA is held LOW if INA is unbiased or floating.
3	GND	Ground: All signals are referenced to this pin.
4	INB	Input to channel B: Inverting input in the SLM27523. Non-Inverting input in the SLM27524 and SLM27525. OUTB is held LOW if INB is unbiased or floating.
5	OUTB	Output of channel B.
6	VDD	Bias Supply Input.
7	OUTA	Output of channel A
8	ENB	Enable input for channel B: ENB is biased LOW to disable the channel B output regardless of the INB state. ENB is biased HIGH or left floating to enable the channel B output. ENB is allowed to float.
	EP	Exposed pad, connect to ground. Only for MSOP8-EP

## FUNCTIONAL BLOCK DIAGRAM

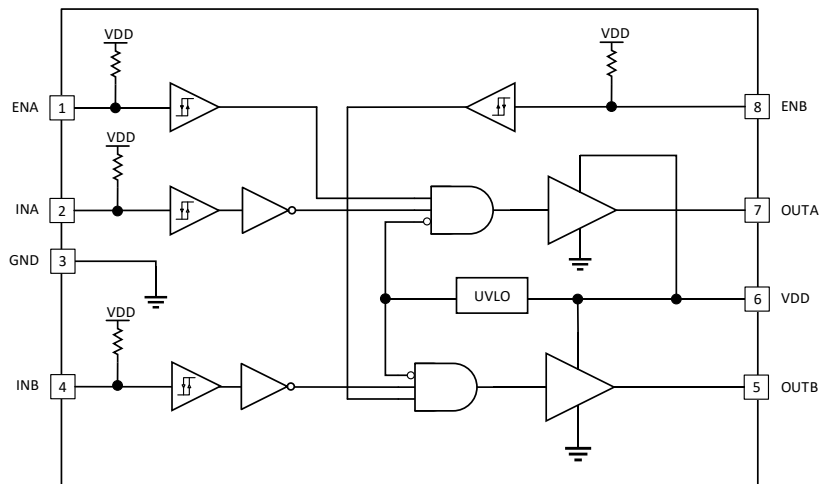


Figure 2. SLM27523 Block Diagram

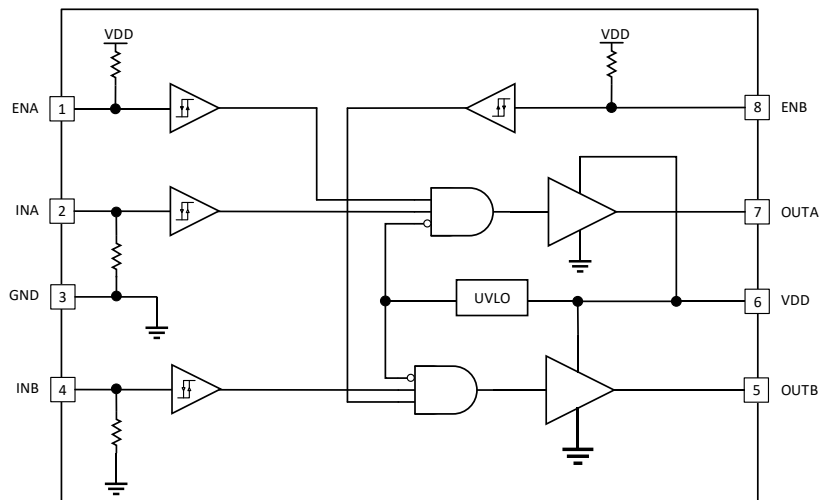


Figure 3. SLM27524 Block Diagram

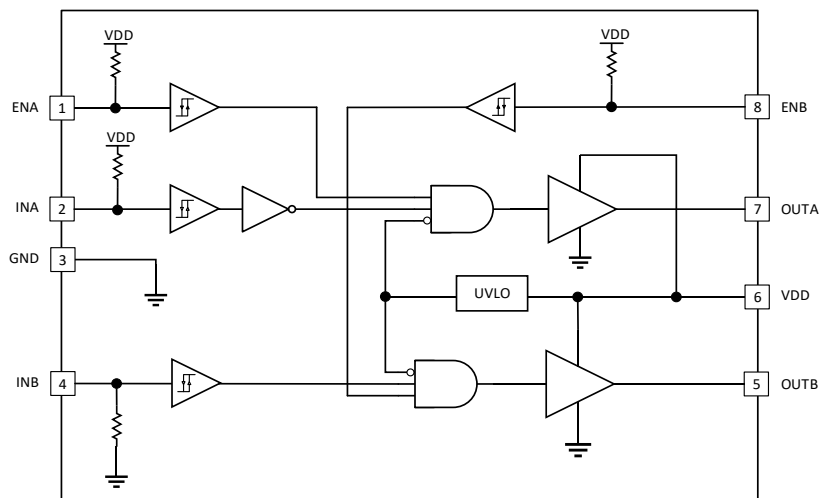


Figure 4. SLM27525 Block Diagram

## ABSOLUTE MAXIMUM RATINGS<sup>1,2,3</sup>

Symbol	Description	Min.	Max.	Units
V <sub>DD</sub>	Supply voltage	-0.3	25	V
V <sub>o</sub>	Continuous voltage on OUTx	-0.3	V <sub>DD</sub> +0.3	
	Repetitive pulse less than 200ns <sup>4</sup>	-2	V <sub>DD</sub> +0.3	
I <sub>o</sub>	Source Continuous Current on OUTx		0.3	A
	Source Pulsed Current on OUTx (0.5 μs) <sup>4</sup>		4.5	
	Sink Pulsed Current on OUTx (0.5 μs) <sup>4</sup>		5.5	
INA, INB, ENA, ENB	Voltage on INA, INB, ENA, ENB.	-6	25	V
T <sub>J</sub>	Operation junction temperature range	-40	150	°C
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)		300	
T <sub>s</sub>	Storage temperature	-55	150	

- 1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2) All voltages are with respect to GND unless otherwise noted.
- 3) These devices are sensitive to electrostatic discharge; follow proper device-handling procedures.
- 4) Values are verified by characterization on bench.

## RECOMMENDED OPERATION CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Definition	Min	Max	Units
V <sub>DD</sub>	Supply voltage	4.5	20	V
INA, INB	Input voltage	-5	20	
ENA, ENB	Enable voltage	-5	20	
T <sub>J</sub>	Operation junction temperature range	-40	140	°C

## THERMAL RESISTANCE

Package	θ <sub>JA</sub>	Units
SOP8	130	°C/W
MSOP8-EP	63	°C/W

**ORDERING INFORMATION**

<b>Order Part No.</b>	<b>Package</b>	<b>QTY</b>
SLM27523CA-DG	SOP8, Pb-Free	2500/Reel
SLM27524CA-DG	SOP8, Pb-Free	2500/Reel
SLM27525CA-DG	SOP8, Pb-Free	2500/Reel
SLM27523GB-DG	MSOP8-EP, Pb-Free	4000/Reel
SLM27524GB-DG	MSOP8-EP, Pb-Free	4000/Reel
SLM27525GB-DG	MSOP8-EP, Pb-Free	4000/Reel

**DYNAMIC ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t <sub>R</sub>	Rise time <sup>1</sup>	C <sub>LOAD</sub> = 1.8 nF		7	15	ns
t <sub>F</sub>	Fall time <sup>1</sup>	C <sub>LOAD</sub> = 1.8 nF		6	10	
t <sub>M</sub>	Delay matching between two channels	INA = INB, OUTA and OUTB at 50% transition point		2	4	
t <sub>PW</sub>	Minimum input pulse width that changes the output state			15	25	
t <sub>D1</sub> , t <sub>D2</sub>	Input to output propagation delay <sup>1</sup>	C <sub>LOAD</sub> = 1.8 nF, 5 V input pulse	7	18	26	
t <sub>D3</sub> , t <sub>D4</sub>	EN to output propagation delay <sup>1</sup>	C <sub>LOAD</sub> = 1.8 nF, 5 V enable pulse	7	18	26	

1) See timing diagrams in Figure 5 to Figure 8.

**STATIC ELECTRICAL CHARACTERISTICS**

 V<sub>DD</sub> = 12 V, C<sub>L</sub> = 1000 pF and T<sub>J</sub> = -40°C to 140°C unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I <sub>DD(off)</sub>	Startup current	V <sub>DD</sub> = 3.4 V INA = INB = V <sub>DD</sub>	55	110	250	uA
		V <sub>DD</sub> = 3.4 V, INA = INB = GND	55	110	250	
V <sub>DDUV+</sub>	Undervoltage positive going threshold	T <sub>J</sub> = 25 °C	3.9	4.2	4.5	V
		T <sub>J</sub> = -40 °C to 140 °C	3.8	4.2	4.6	
V <sub>DDUV-</sub>	Undervoltage negative going threshold		3.7	3.9	4.4	
V <sub>DD_H</sub>	Supply voltage hysteresis			0.3		
V <sub>IH</sub>	Input signal high threshold	Applied to INA, INB, ENA, ENB	1.6	1.9	2.3	V
V <sub>IL</sub>	Input signal low threshold	Applied to INA, INB, ENA, ENB	1.0	1.3	1.5	
I <sub>O</sub>	Source peak current	C <sub>L</sub> = 0.22 μF		4.5		A
	Sink peak current	C <sub>L</sub> = 0.22 μF		5.5		
V <sub>OH</sub>	High level output voltage	I <sub>O</sub> = -10 mA, V <sub>DD</sub> -V <sub>O</sub>		0.008	0.016	V
V <sub>OL</sub>	Low output voltage	I <sub>O</sub> = 10 mA		0.005	0.009	
R <sub>OH</sub>	Output pull-up resistance	I <sub>O</sub> = -10 mA	0.5	0.8	1.6	Ω
R <sub>OL</sub>	Output pull-down resistance	I <sub>O</sub> = 10 mA	0.3	0.5	0.9	

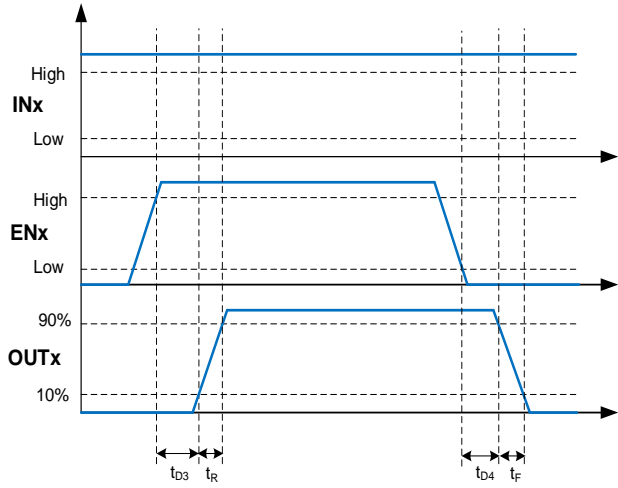


Figure 5. Enable Function for Non-Inverting Input Driver

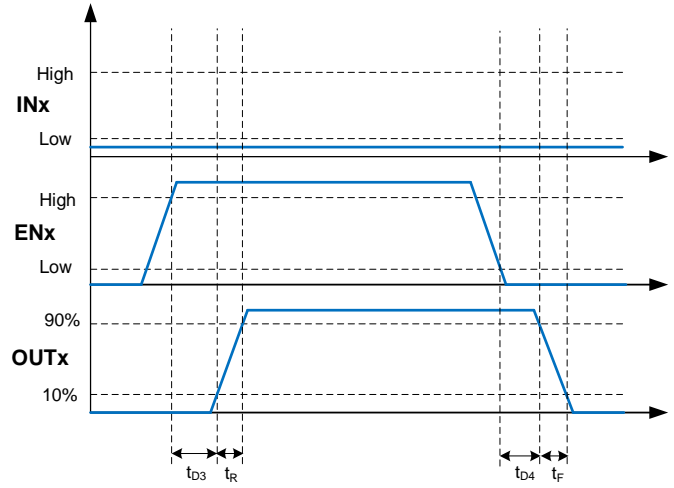


Figure 6. Enable Function for Inverting Input Driver

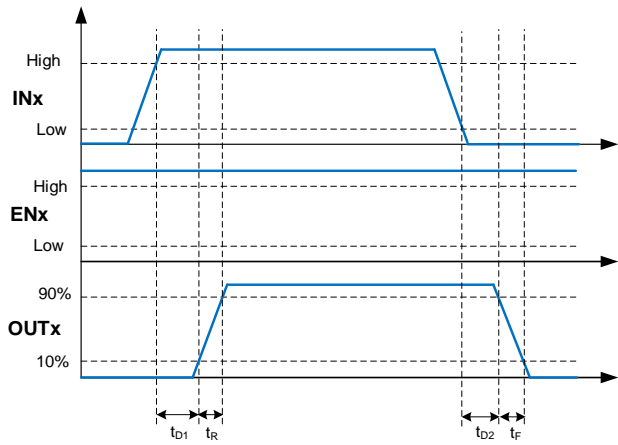


Figure 7. Non-Inverting Input Driver Operation

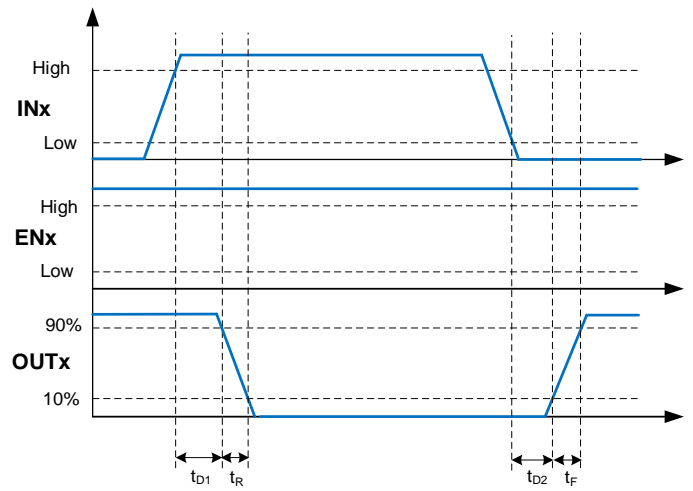


Figure 8. Inverting Input Driver Operation



## TYPICAL PERFORMANCE CHARACTERISTIC

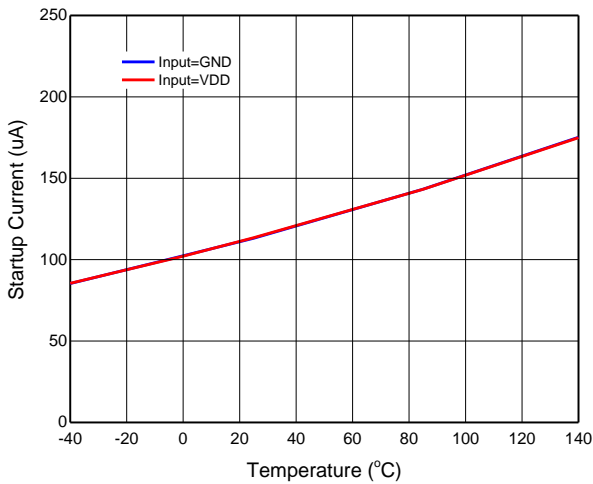


Figure 9. Startup Current vs Temperature, VDD=3.4V

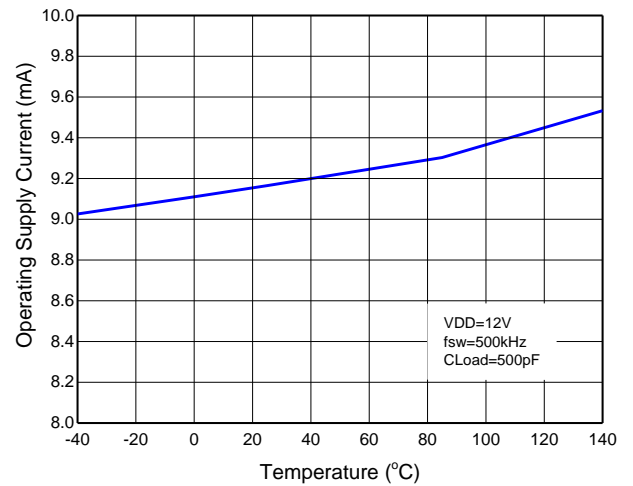


Figure 10. Operating Supply Current vs Temperature

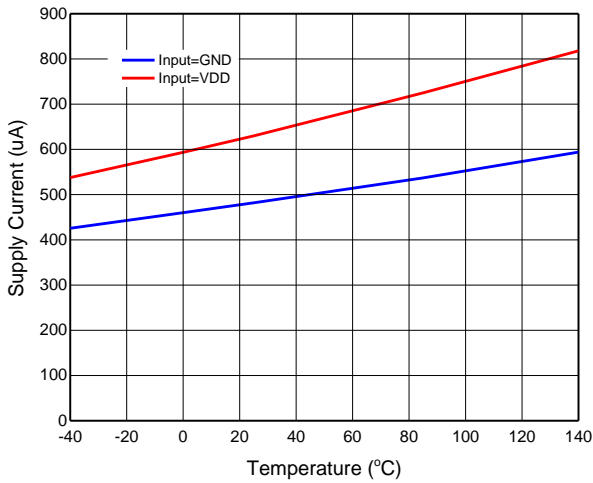


Figure 11. Supply Current vs Temperature (Output in DC ON/OFF condition, ENx=VDD=12V)

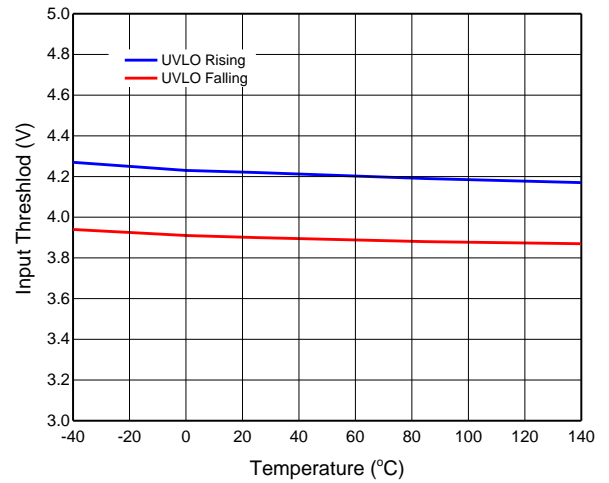


Figure 12. UVLO Threshold vs Temperature

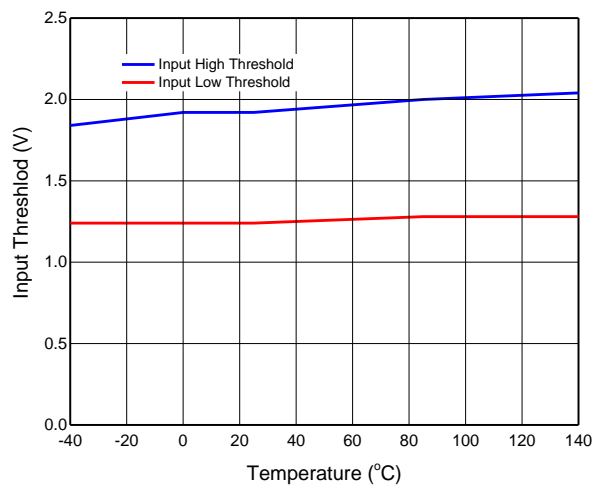


Figure 13. Input Threshold vs Temperature, VDD=12V

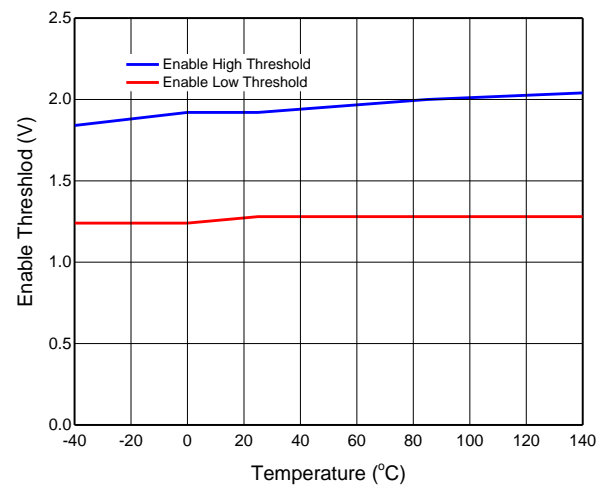


Figure 14. Enable Threshold vs Temperature

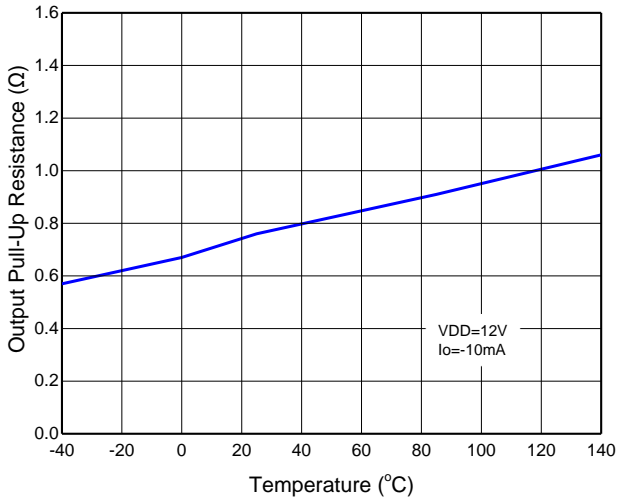


Figure 15. Output Pull-up Resistance vs Temperature

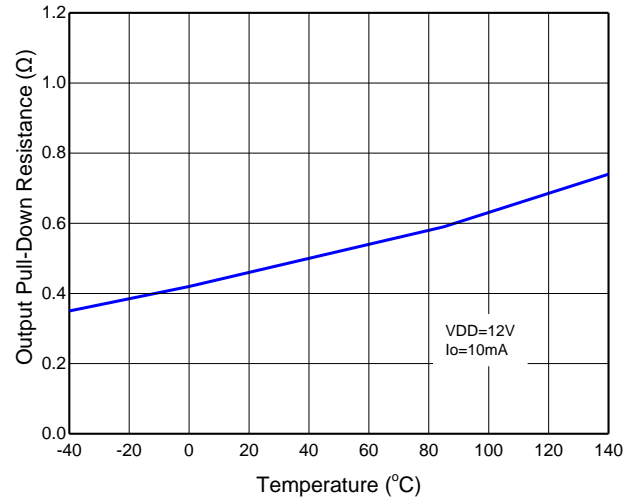


Figure 16. Output Pull-down Resistance vs Temperature

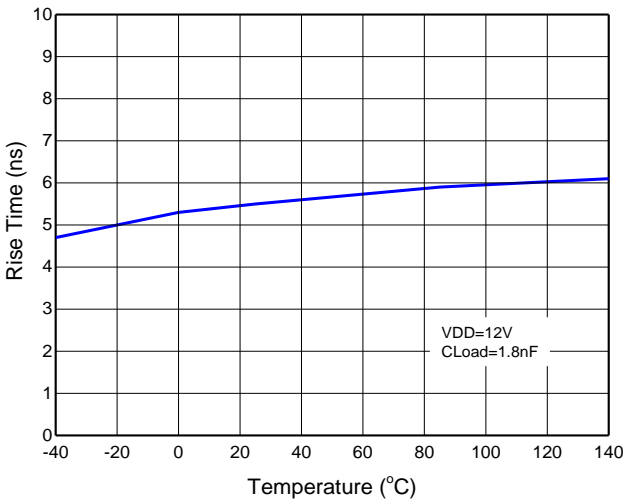


Figure 17. Rise Time vs Temperature

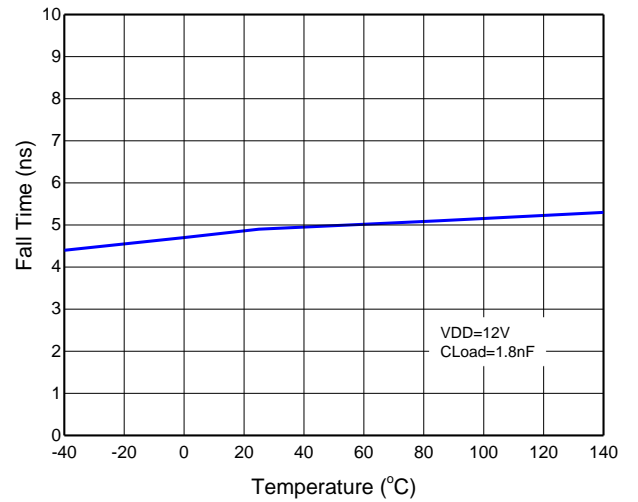


Figure 18. Fall Time vs Temperature

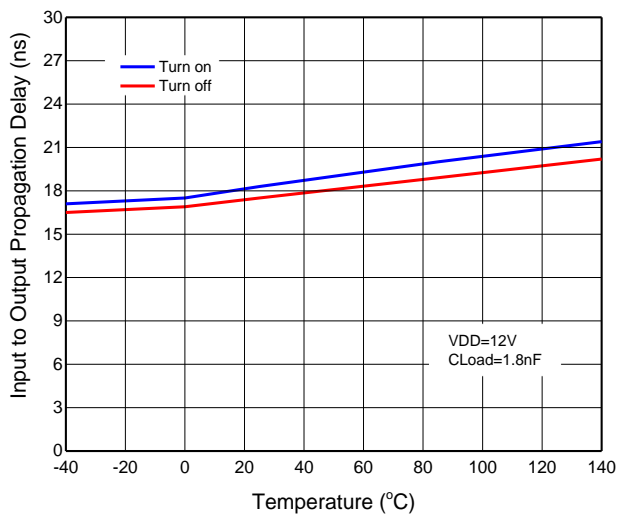


Figure 19. Input to Output Propagation Delay vs Temperature

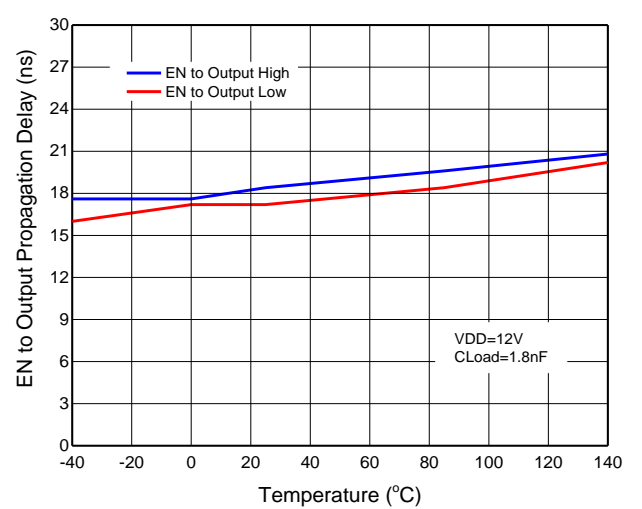


Figure 20. Enable to Output Propagation Delay vs Temperature

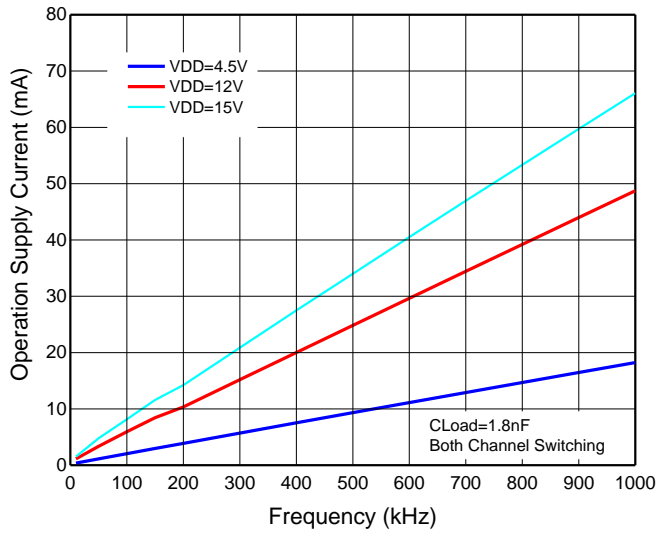


Figure 21. Operating Supply Current vs Frequency

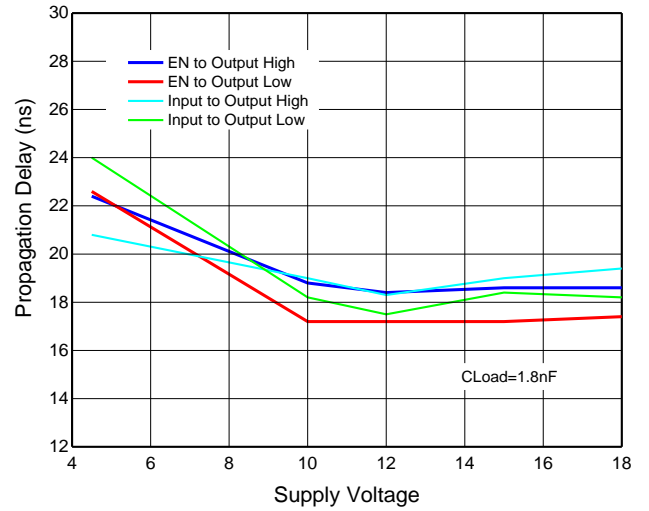


Figure 22. Propagation Delay vs Supply Voltage

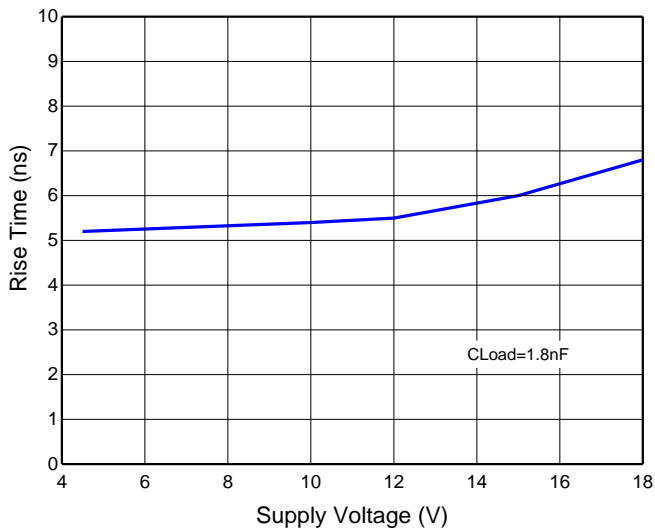


Figure 23. Rise Time vs Supply Voltage

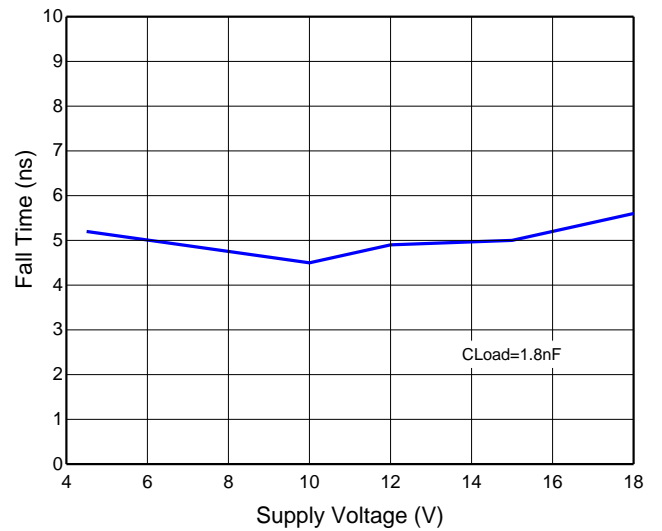


Figure 24. Fall Time vs Supply Voltage

## FEATURE DESCRIPTION

### VDD and Under-Voltage Lockout

The SLM2752x device has internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (for example when  $V_{DD}$  voltage is less than  $V_{DDUV+}$  during power up or when VDD voltage is less than  $V_{DDUV-}$  during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300mV typical hysteresis. This hysteresis helps prevent chatter when low  $V_{DD}$  supply voltage have noise from the power supply and also when there are droops in the VDD bias voltage when the system starts switching and there is a sudden increase in  $I_{DD}$ .

### Input Stage

The input pins of the SLM2752x gate driver are based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typically high threshold = 1.9 V and typically low threshold = 1.3 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3V and 5V digital power-controller devices. SLM2752x also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The SLM2752x features an important safety feature wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using GND pull-down resistors on all the non-inverting input pins and  $V_{DD}$  pull-up resistors on all the inverting input pins (INA, INB), as shown in the device block diagrams.

The input stage of each driver is driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition time. With a slow changing input voltage, the output of the driver may switch repeatedly at a high frequency. While the wide hysteresis offered in SLM2752x definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device.

### Enable Function

SLM2752x is provided with independent enable pins ENx for exclusive control of each driver channel operation. The enable pins are based on a non-inverting configuration (active high operation). Thus, when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the drivers are disabled. Like the input pins, the enable pins are also based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3V and 5V microcontrollers. The SLM2752x also features tight control of the enable function threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The ENx pins are internally pulled up to VDD using pull-up resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. If the channel A and channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB are connected and driven together.

The enable function is an extremely beneficial feature in gate driver devices especially for certain applications such as synchronous rectification where the driver outputs disabled in light load conditions to prevent negative current circulation and to improve light load efficiency.

### Output Stage

Each output stage in the SLM2752x device is capable of supplying 4.5 A peak source and 5.5 A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out.

The channel A and channel B outputs can be paralleled to provide higher driver current capability. In such application, the INA and INB need to be connected together and ENA, ENB also need be connected together.

For example, in applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

## PACKAGE CASE OUTLINES

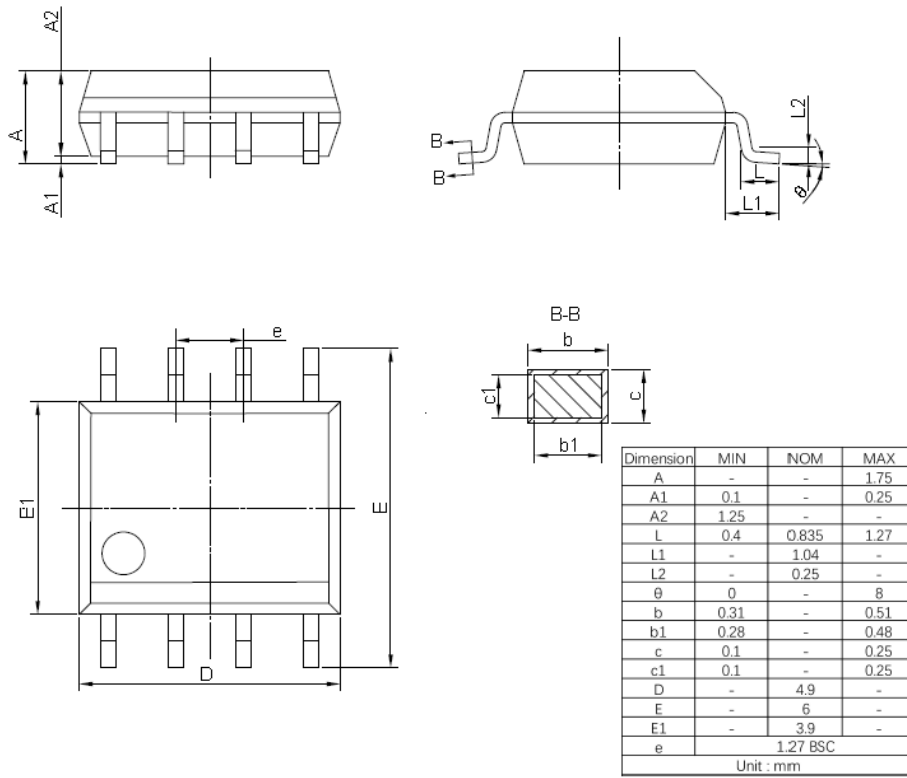


Figure 25. SOP8 Package Outline Dimensions

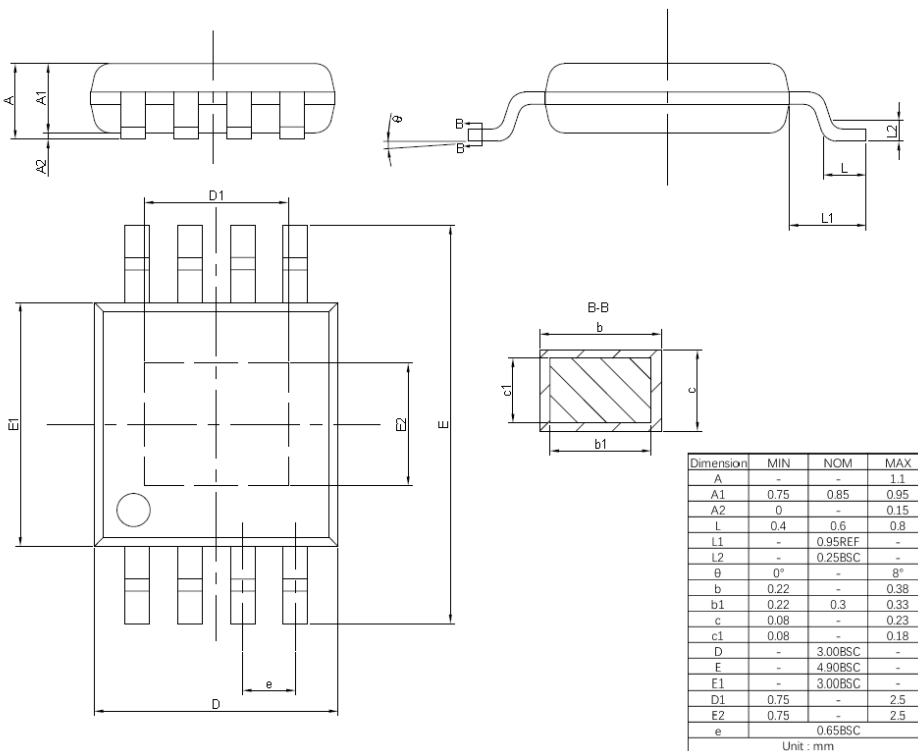


Figure 26. MSOP8-EP Package Outline Dimensions

**REVISION HISTORY**

Note: page numbers for previous revisions may differ from page numbers in current version

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>Rev 1.0 datasheet : 2022-01-26</b>	
Whole document	Initial datasheet release
<b>Rev 1.1 datasheet : 2022-04-28</b>	
Page 5	Add the thermal resistance

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