# 160V 3-Phase Bridge Driver

## PRODUCT SUMMARY

- **$V_{OFFSET}$** 160 V max.
- **$I_O$+/-** 350 mA / 650 mA
- **$V_{OUT}$** 10 V - 20 V
- **$t_{on/off}$ (typ.)** 100 ns / 110 ns
- **Deadtime (typ.)** 270 ns

## FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +160 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- 3.3 V, 5 V, and 15 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Cross-conduction prevention logic with Typ. 270ns dead time
- Available in SOP20W and TSSOP20 packages

## GENERAL DESCRIPTION

The SLM7888 is a high voltage, high speed power MOSFET and IGBT drivers with three independent high- and low-side referenced output channels for 3-phase applications.

Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

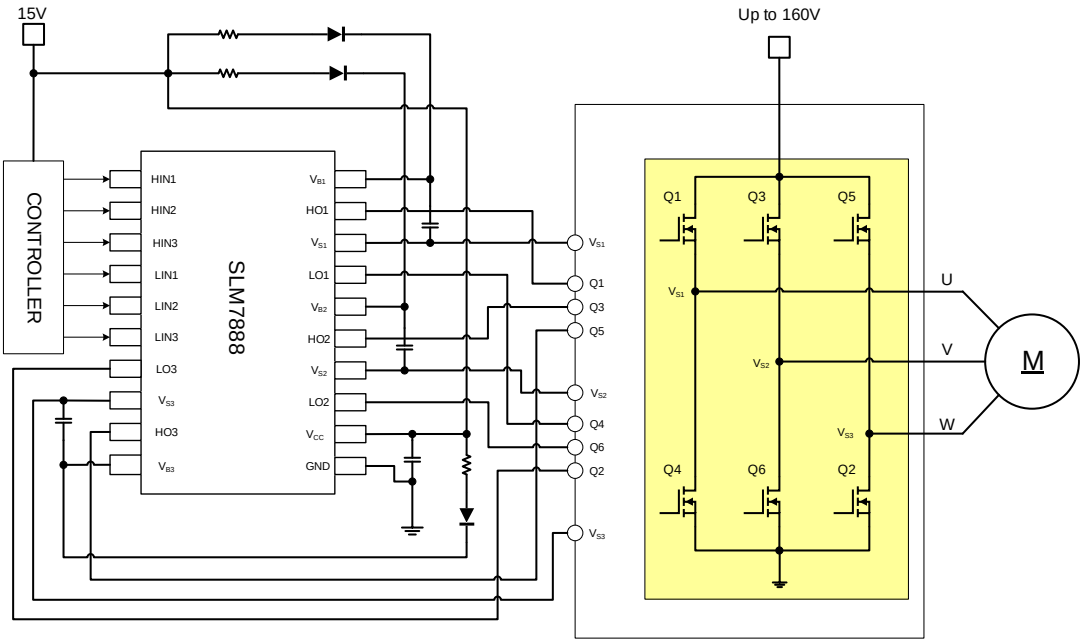
The logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic.

The UVLO circuits prevent malfunction when VDD and VBS are lower than the specified threshold voltage.

Propagation delays are matched to simplify use in high frequency applications.

The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 160 V.

## TYPICAL APPLICATION CIRCUIT




Refer to Lead Assignments for correct configuration. This diagram shows electrical connections only.

Figure 1. Typical Application Circuit

## PIN CONFIGURATION

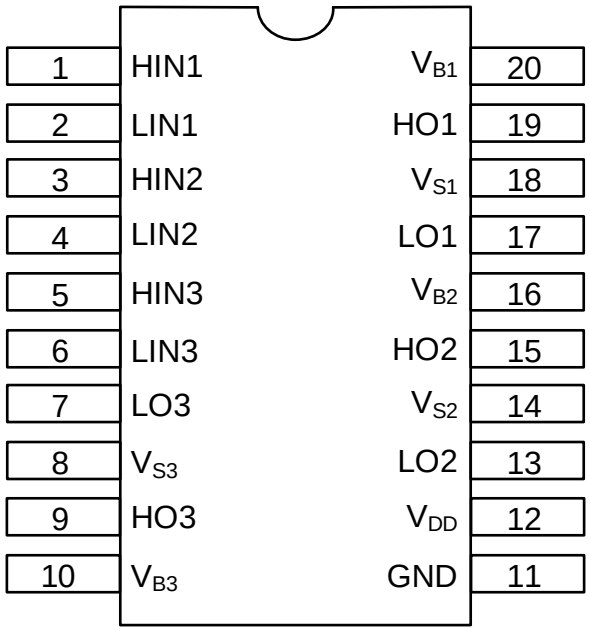
| Package | Pin Configuration (Top View) |
|---|---|
| SOP20W<br>TSSOP20 |  |



Figure 2. Pin Configuration

## PIN DESCRIPTION

| No. | Pin | Description |
|---|---|---|
| 1, 3, 5 | HIN1, 2, 3 | Logic input for high-side gate driver output (HO). |
| 2, 4, 6 | LIN1, 2, 3 | Logic input for low-side gate driver output (LO). |
| 19, 15, 9 | HO1, 2, 3 | High-side gate driver outputs. |
| 17, 13, 7 | LO1, 2, 3 | Low-side gate driver outputs. |
| 18, 14, 8 | $V_{S1, 2, 3}$ | High-side drivers floating supply offset. |
| 20, 16, 10 | $V_{B1, 2, 3}$ | High-side drivers floating supply. |
| 11 | GND | Ground. |
| 12 | $V_{DD}$ | Logic and all low-side gate drivers power supply. |

## ORDERING INFORMATION

INDUSTRIAL RANGE: -40°C TO +125°C

| Order Part No. | Package | QTY |
|---|---|---|
| SLM7888CH | SOP20W, Pb-Free | 1000/Reel |
| SLM7888MD | TSSOP20, Pb-Free | 4000/Reel |

## FUNCTIONAL BLOCK DIAGRAM

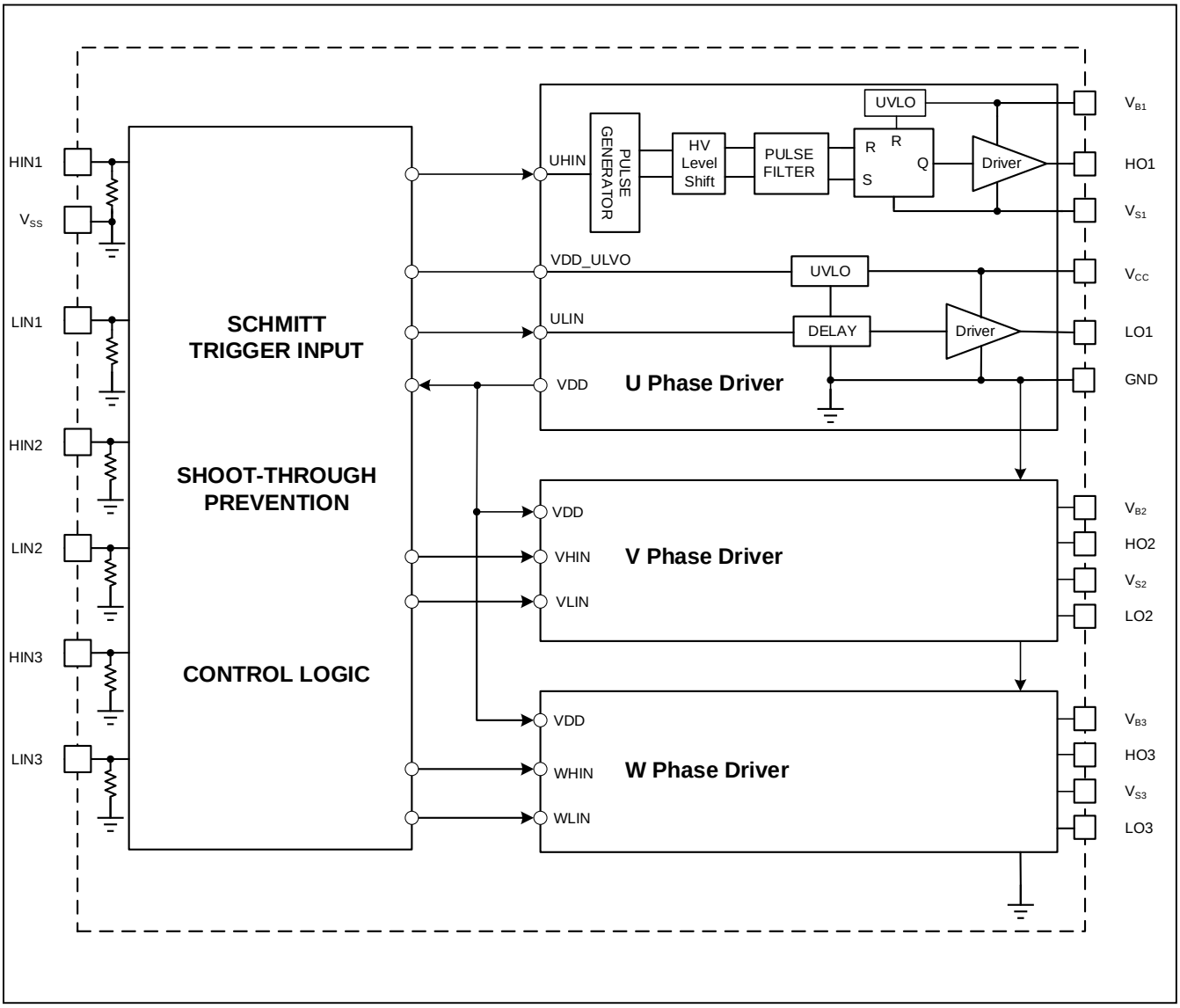



Figure 3. Functional Block Diagram

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_B$ | High-side floating absolute voltage | | -0.3 | 185 | V |
| $V_S$ | High-side floating supply offset voltage | | $V_{B1,2,3}$ - 25 | $V_{B1,2,3}$ + 0.3 | |
| $V_{HO}$ | High-side floating output voltage | | $V_{S1,2,3}$ - 0.3 | $V_{B1,2,3}$ + 0.3 | |
| $V_{CC}$ | Low-side and logic fixed supply voltage | | -0.3 | 25 | |
| $V_{IN}$ | Logic input voltage (LIN, HIN) | | - 0.3 | $V_{DD}$ + 0.3 | |
| $V_{LO1,2,3}$ | Low-side output voltage | | -0.3 | $V_{DD}$ + 0.3 | |
| $dV_S/dt$ | Allowable offset supply voltage transient | | --- | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leqslant$ +25°C | SOP20W | --- | 1.5 | W |
| | | TSSOP20 | --- | 1.2 | |
| $\theta_{JA}$ | Thermal resistance, junction to ambient | SOP20W | --- | 60 | °C/W |
| | | TSSOP20 | --- | 75 | |
| $T_J$ | Junction temperature | | -40 | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | --- | 300 | |

**Note:** Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

## RECOMMENDED OPERATION CONDITIONS

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{B1,2,3}$ | High-side floating supply voltage | $V_{S1,2,3}$ + 10 | $V_{S1,2,3}$ + 20 | V |
| $V_{S1,2,3}$ | High-side floating supply offset voltage[1] | -0.3 | 160 | |
| $V_{HO1,2,3}$ | High-side floating output voltage | $V_{S1,2,3}$ | $V_{B1,2,3}$ | |
| $V_{LO1,2,3}$ | Low-side output voltage | GND | $V_{DD}$ | |
| $V_{DD}$ | Low-side and logic fixed supply voltage | 10 | 20 | |
| $V_{IN}$ | Logic input voltage (LIN, HIN) | GND | $V_{DD}$ | |
| $T_A$ | Ambient temperature | - 40 | 125 | °C |

Note: Tested with VDD=15V.

## DYNAMIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15 V, $V_{S1,2,3}$ = GND, $C_L$ = 1000 pF and $T_A$ = 25°C unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | $V_S$ = 0 V | --- | 100 | 220 | ns |
| $t_{off}$ | Turn-off propagation delay | $V_S$ = 0 V | --- | 110 | 240 | |
| $t_r$ | Turn-on rise time | | --- | 50 | 120 | |
| $t_f$ | Turn-off fall time | | --- | 30 | 80 | |
| DT | Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off | $V_{IN}$ = 0 V & 5 V | 100 | 270 | 440 | |
| MT | Matching delay, HS & LS turn-on/off | | --- | 10 | 50 | |
| MDT | Matching delay, Dead Time | | --- | 45 | 80 | |

## STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}$ ($V_{DD}$, $V_{BS1,2,3}$) = 15 V and $T_A$ = 25°C unless otherwise specified. The $V_{IN}$, $V_{TH}$, and $I_{IN}$ parameters are referenced to GND and are applicable to all 6 channels (LIN, HIN). The $V_O$ and $I_O$ parameters are referenced to GND and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic “1” input voltage (LIN, HIN) | $V_{CC}$ = 10 V to 20V | 2.5 | --- | --- | V |
| $V_{IL}$ | Logic “0” input voltage (LIN, HIN) | | --- | --- | 1.0 | |
| $V_{OH}$ | High level output voltage, $V_{BIAS}$ - $V_O$ | $I_O$ = 20 mA | --- | 0.35 | 0.5 | |
| $V_{OL}$ | Low level output voltage, $V_O$ | | --- | 0.1 | 0.2 | |
| $V_{DDUV+}$ | $V_{DD}$ supply undervoltage positive going threshold | | 5.5 | 6.6 | 7.8 | |
| $V_{DDUV-}$ | $V_{DD}$ supply undervoltage negative going threshold | | 5.2 | 6.3 | 7.5 | |
| $V_{DDUVH}$ | $V_{DD}$ supply undervoltage lockout hysteresis | | | 0.3 | --- | |
| $V_{BSUV+}$ | $V_{BS}$ supply undervoltage positive going threshold | | 5.2 | 6.2 | 7.2 | |
| $V_{BSUV-}$ | $V_{BS}$ supply undervoltage negative going threshold | | 4.9 | 5.9 | 6.9 | |
| $V_{BSUVH}$ | $V_{BS}$ supply undervoltage lockout hysteresis | | | 0.3 | --- | |
| $I_{LK}$ | Offset supply leakage current | $V_{B1,2,3}$ = $V_{S1,2,3}$ = 160 V | --- | --- | 10 | µA |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | $V_{IN}$ = 0 V | --- | 70 | 100 | |
| $I_{QDD}$ | Quiescent $V_{DD}$ supply current | | --- | 400 | 500 | |
| $I_{OPDD}$ | Operating $V_{DD}$ supply current for each channel | $f_{LIN1,2,3}$ = 20 kHz | --- | 560 | 900 | |
| $I_{OPBS}$ | Operating $V_{BS}$ supply current for each channel | $f_{LIN1,2,3}$ = 20 kHz | --- | 200 | 400 | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IN+}$ | Logic “1” input bias current | HIN1, 2, 3 = 5 V,<br>LIN1, 2, 3 = 5 V | --- | 25 | 40 | μA |
| $I_{IN-}$ | Logic “0” input bias current | HIN1, 2, 3 = 0 V,<br>LIN1, 2, 3 = 0 V | --- | --- | 2 | |
| $I_{O+}$ | Output high short circuit pulsed current | $V_O$ = 0 V, $V_{IN}$ = $V_{IH}$<br>PW ⩽ 10 μs | --- | 350 | --- | mA |
| $I_{O-}$ | Output low short circuit pulsed current | $V_O$ = 15 V, $V_{IN}$ = $V_{IL}$<br>PW ⩽ 10 μs | --- | 650 | --- | |
| $R_{IN}$ | Input pull-down resistance | | 150 | 200 | 300 | kΩ |

## TYPICAL PERFORMANCE CHARACTERISTICS

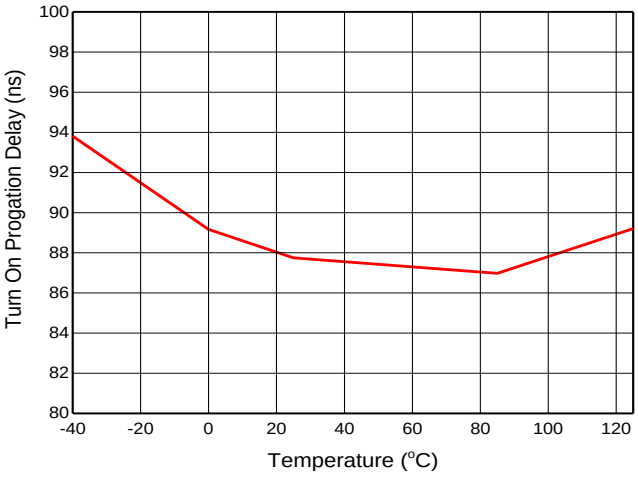



Figure 4. Turn on Propagation Delay vs. Temp.

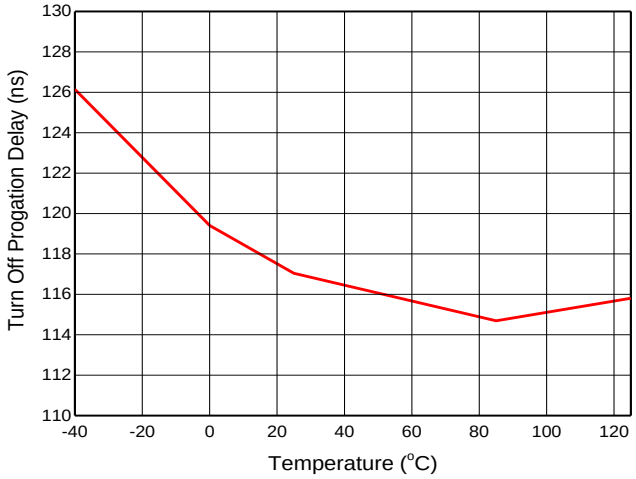



Figure 5. Turn off Propagation Delay vs. Temp.

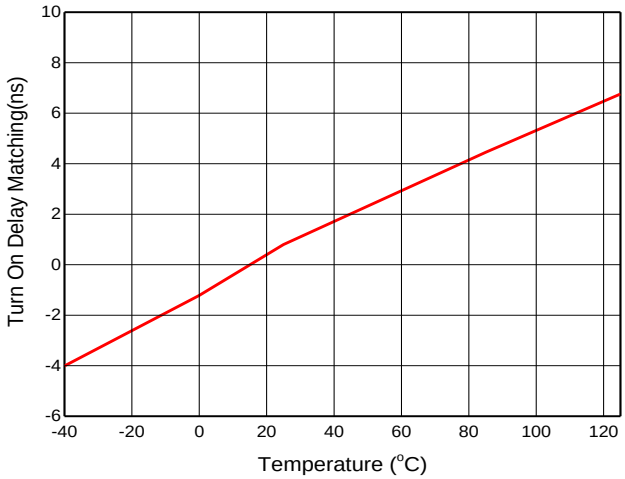



Figure 6.Turn on Delay Matching vs. Temp.

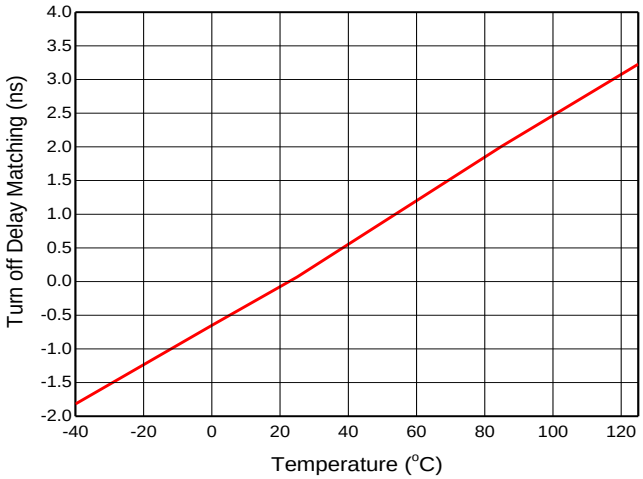



Figure 7. Turn off Delay Matching vs. Temp.

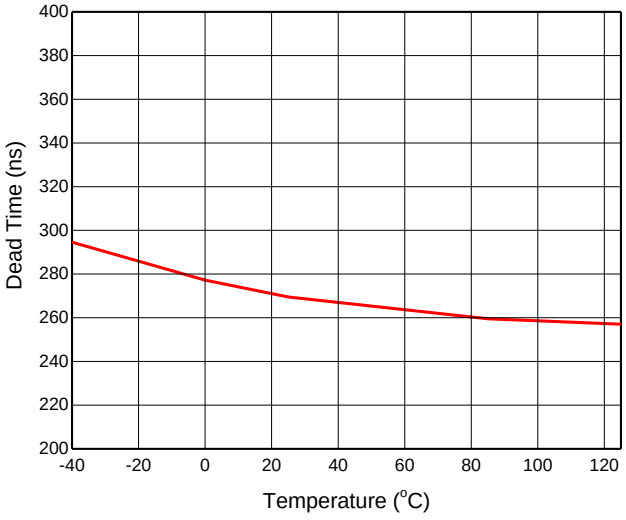



Figure 8. Dead Time vs. Temp.

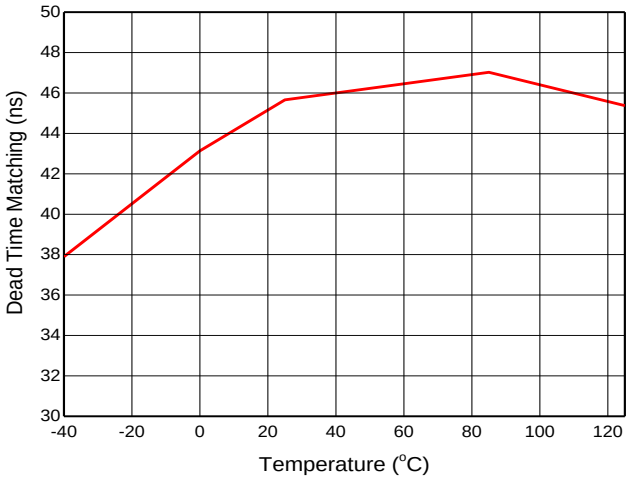



Figure 9. Dead Time Matching vs. Temp.

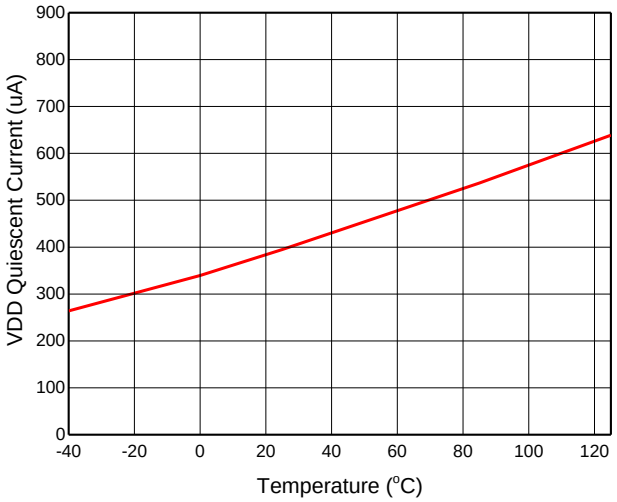



Figure 10. $V_{DD}$ Quiescent Current vs. Temp.

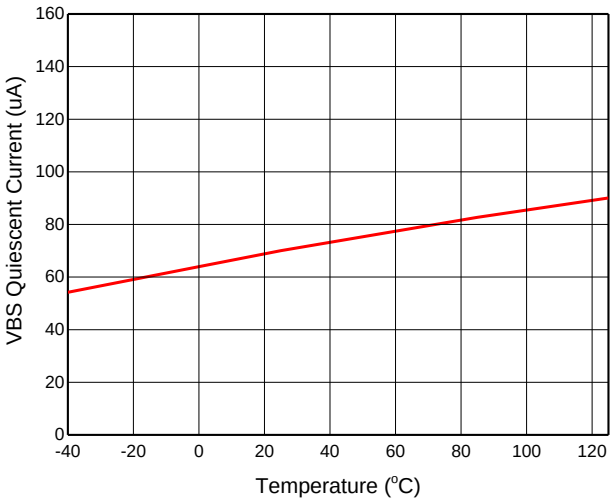



Figure 11. $V_{BS}$ Quiescent Current vs. Temp.

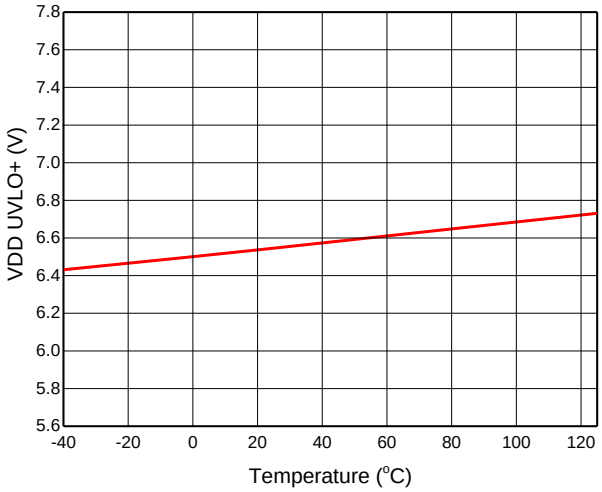



Figure 12. VDD UVLO+ vs. Temp.

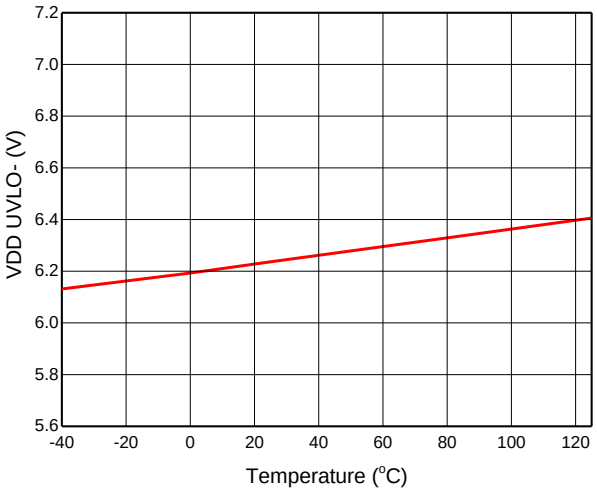



Figure 13. VDD UVLO- vs. Temp.

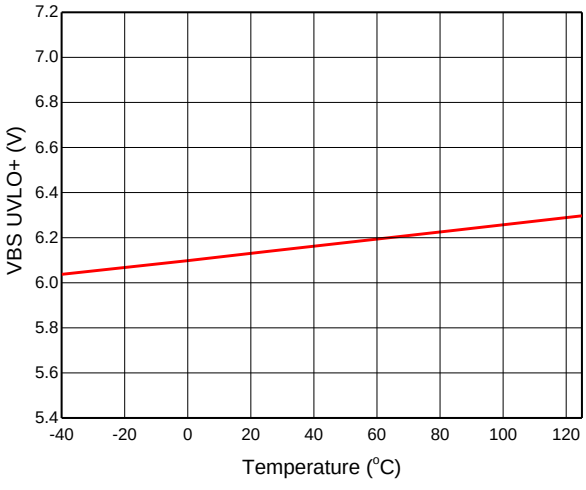



Figure 14. VBS UVLO+ vs. Temp.

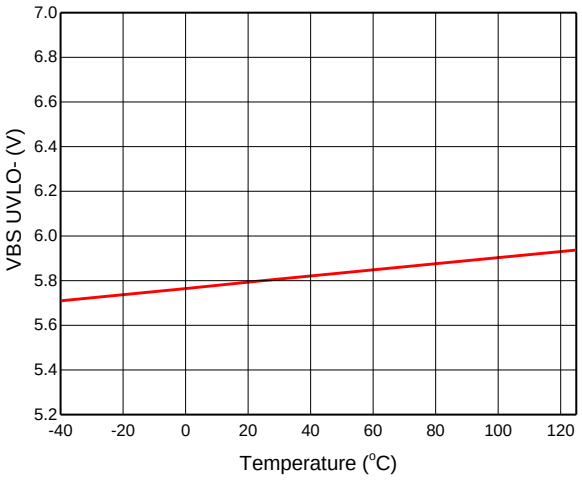



Figure 15. VBS UVLO- vs. Temp.

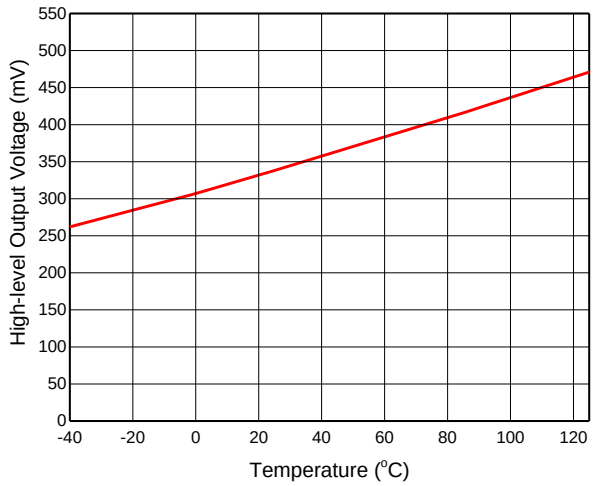



Figure 16. High-level Output Voltage vs. Temp.

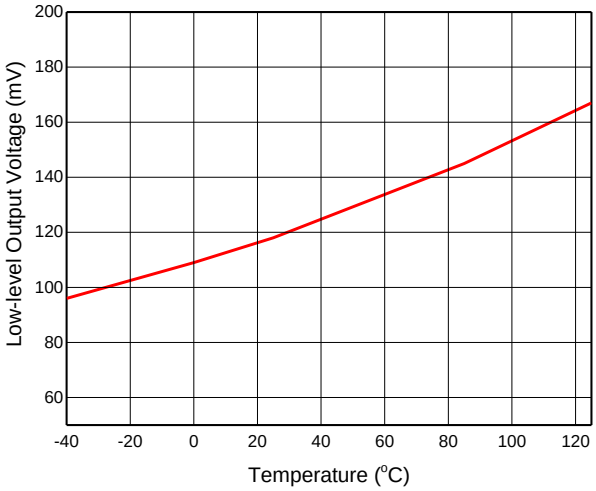



Figure 17. Low-level Output Voltage vs. Temp.

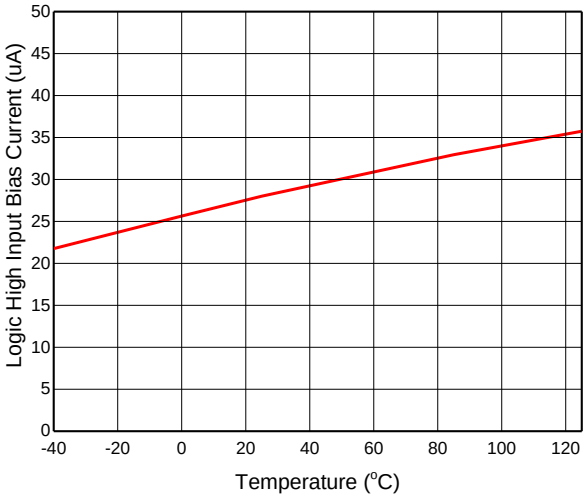



Figure 18. Logic High Input Bias Current vs. Temp

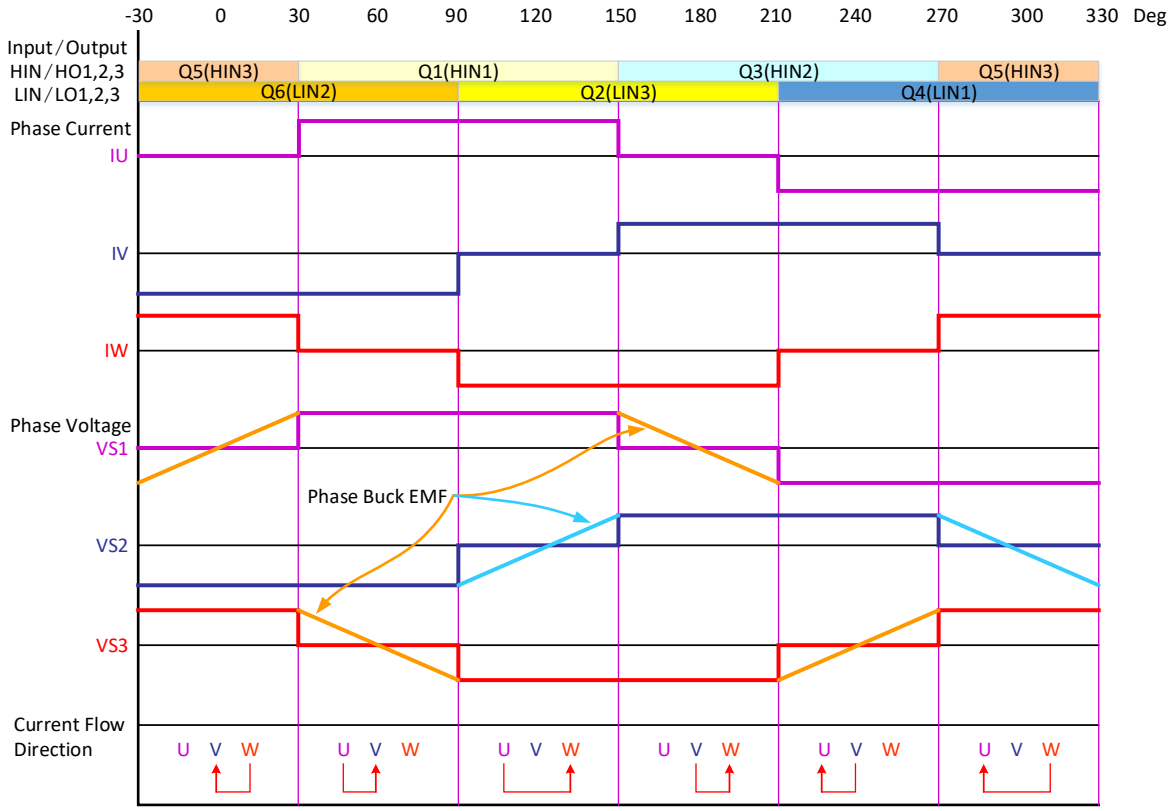



Figure 19. 120° Communication Operation Waveforms for 3-Phase BLDC Motor Application

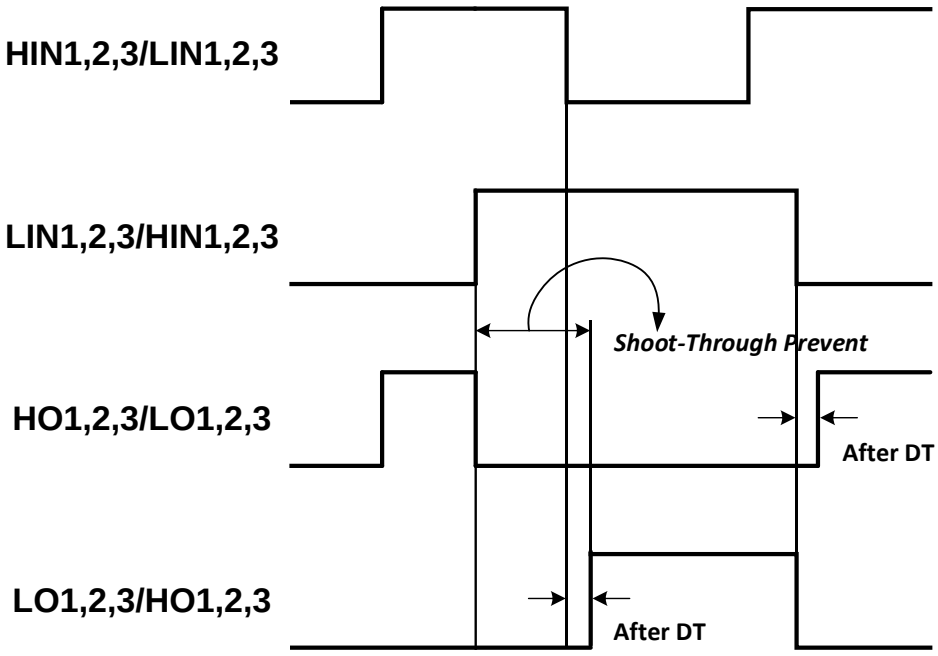



Figure 20. Input/Output Timing Diagram

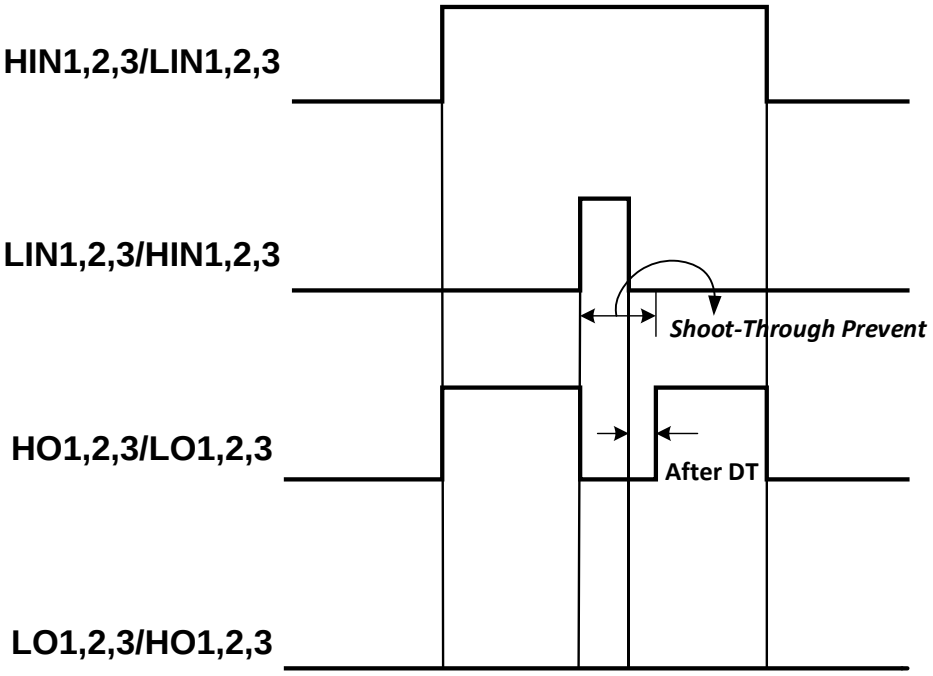



Figure 21. Input/Output Timing Diagram

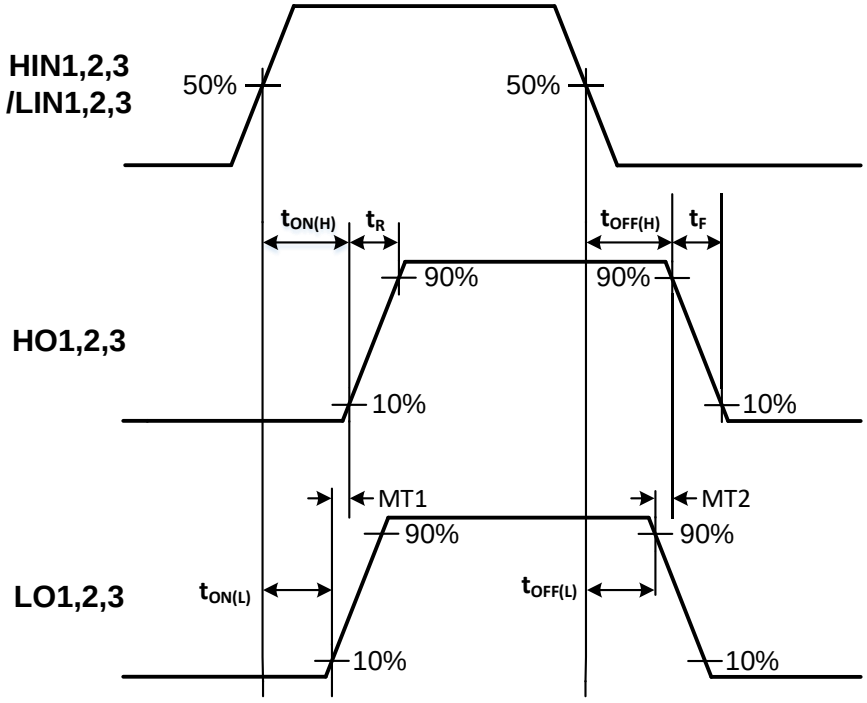
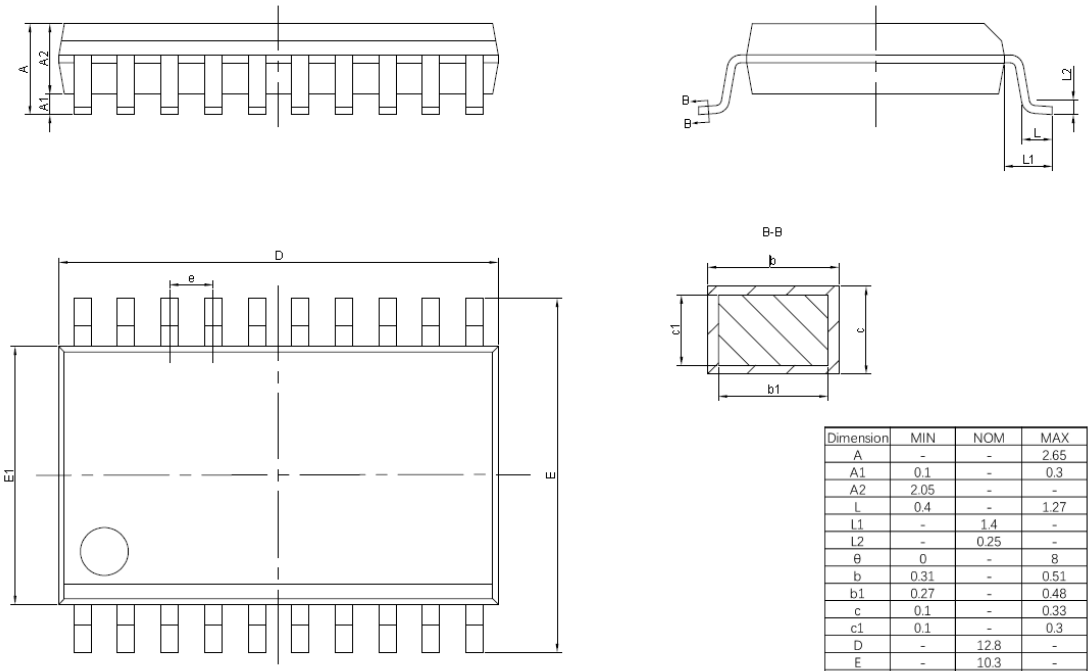


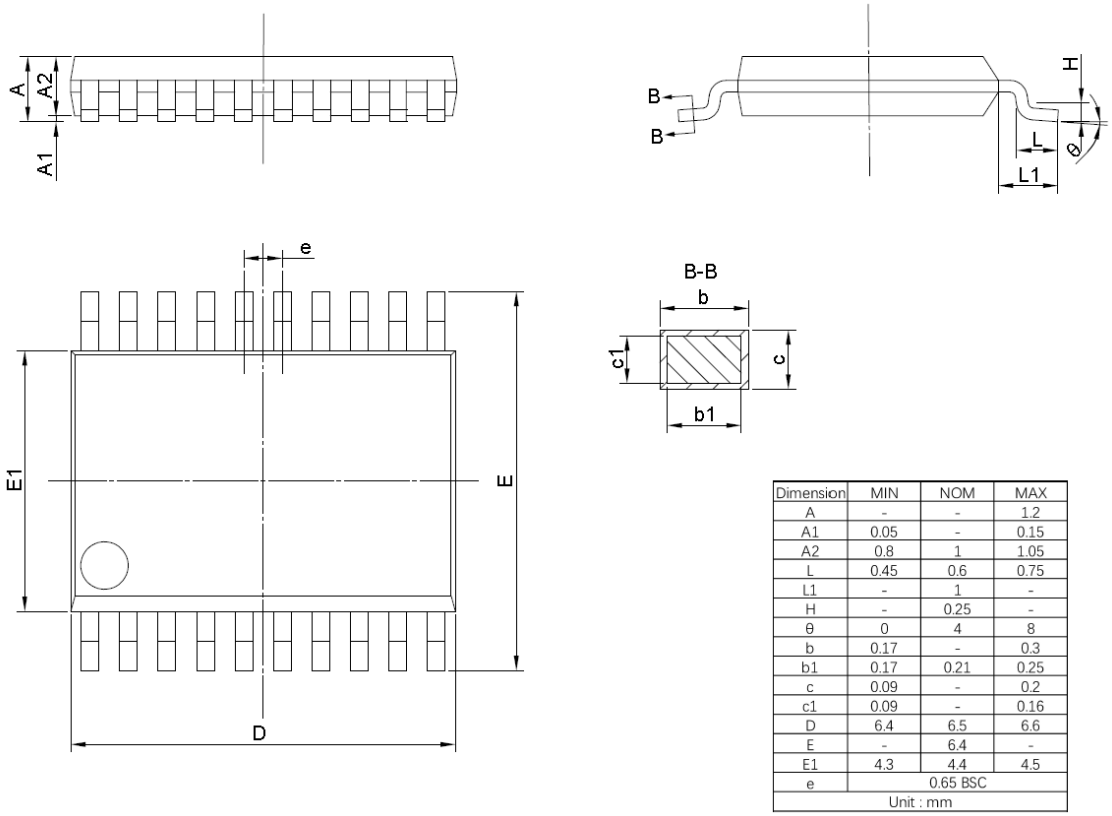

Figure 22. Switching Time Definition

## PACKAGE CASE OUTLINE




| Dimension | MIN | NOM | MAX |
|---|---|---|---|
| A | - | - | 2.65 |
| A1 | 0.1 | - | 0.3 |
| A2 | 2.05 | - | - |
| L | 0.4 | - | 1.27 |
| L1 | - | 1.4 | - |
| L2 | - | 0.25 | - |
| θ | 0 | - | 8 |
| b | 0.31 | - | 0.51 |
| b1 | 0.27 | - | 0.48 |
| c | 0.1 | - | 0.33 |
| c1 | 0.1 | - | 0.3 |
| D | - | 12.8 | - |
| E | - | 10.3 | - |
| E1 | - | 7.5 | - |
| e | 1.27BASIC | | |
| Unit : mm | | | |

Figure 23. SOP20W Outline Dimensions




| Dimension | MIN | NOM | MAX |
|---|---|---|---|
| A | - | - | 1.2 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.8 | 1 | 1.05 |
| L | 0.45 | 0.6 | 0.75 |
| L1 | - | 1 | - |
| H | - | 0.25 | - |
| θ | 0 | 4 | 8 |
| b | 0.17 | - | 0.3 |
| b1 | 0.17 | 0.21 | 0.25 |
| c | 0.09 | - | 0.2 |
| c1 | 0.09 | - | 0.16 |
| D | 6.4 | 6.5 | 6.6 |
| E | - | 6.4 | - |
| E1 | 4.3 | 4.4 | 4.5 |
| e | 0.65 BSC | | |
| Unit : mm | | | |

Figure 24. TSSOP20 Outline Dimensions

## REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

| Page or Item | Subjects (major changes since previous revision) |
|---|---|
| **Rev 1.7 datasheet, 2019-8-27** | |
| Whole document | New company logo released |
| Page 1 | Remove “June 2019” |
| **Rev 1.8 datasheet, 2019-12-19** | |
| Page 2 | Change order information for SLM7888MD |
| **Rev 1.9 datasheet, 2022-5-29** | |
| Whole datasheet | Update the Logo and format |
| Page5, 6 | Update the $t_{on}$, $t_{off}$, MT and MDT in dynamic electrical characteristics<br>Update the $V_{OH}$, $V_{OL}$, VDD UVLO and VBS UVLO, $I_{QBS}$, $I_{QDD}$, $I_{OPDD}$, $I_{OPBS}$, $I_{IN+}$ in static electrical characteristics |
| Page 7, 8, 9 | Update the typical performance characteristics |
| Page 12 | Change the package name from SOIC20L (WB) to SOP20W; from TSSOP-20L (NB) to TSSOP20 |

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