

1. Features

- Compliant with IEEE802.3at Type 1 & Type 2
- Small SIL package size - 56mm (L) x 14mm (H)
- Low cost
- Four independent PSE outputs, capable of up to 30W each
- Minimal (low cost) external components required
- Programmable current limits
- Per Port Current/Voltage monitoring

2. Description

The Ag6400 is a quad Power Sourcing Equipment (PSE) module designed for use in IEEE802.3at Type 1 and Type 2 Power over Ethernet (PoE) applications.

Capable of providing up to 30W per port, Ag6400 is aimed at applications requiring PSE functionality such as IP switches, routers and hubs, CCTV DVR, home networking and industrial ethernet.

Ag6400 is a self-contained module, requiring just a few external components to provide a great deal of control and feedback over each Powered Device (PD) that is connected to the PSE.

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3. Ag6400 Product Selector

Part Number†	Marking	Variant / Date code *
Ag6400-S	Ag6400	ww/yy

• ww/yy represents date code on manufacture. ww – Week yy-Year

† The Ag6400 fully meets the requirements of the RoHS directive 2002/95/EC on the restriction of hazardous substances in electronic equipment.

Table 1: Ordering Information

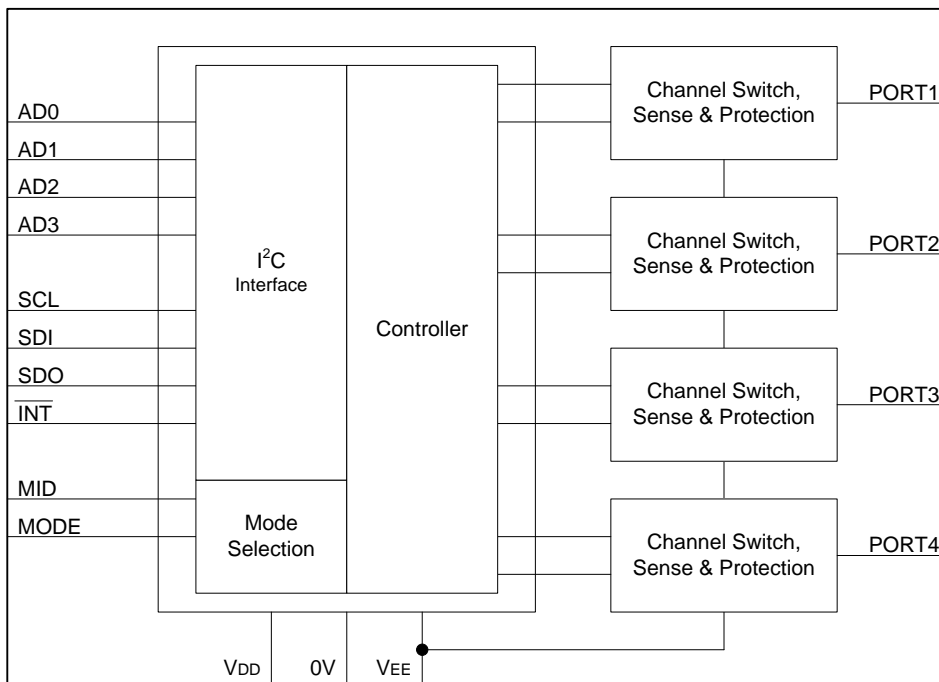


Figure 1: Block Diagram

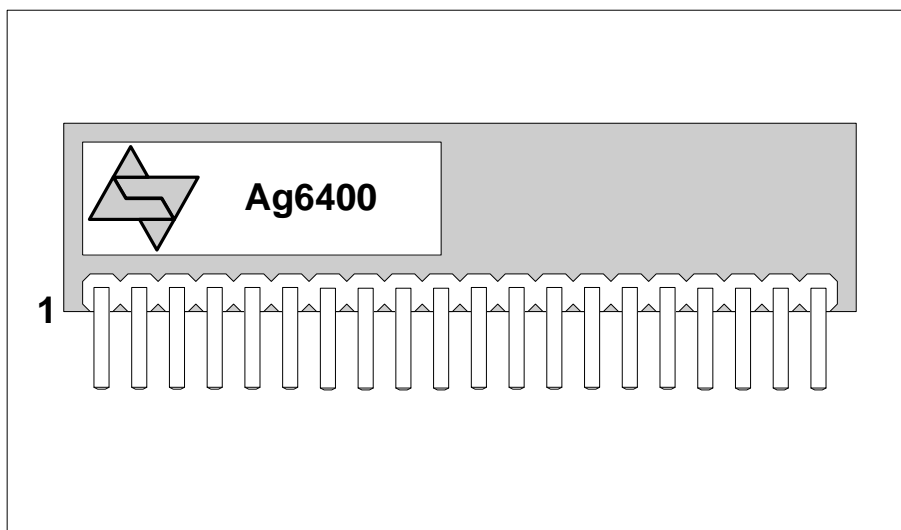


Figure 2: Ag6400 Package Format

4. Pin Description

Pin #	Name	Description
1	V _{DD}	Logic Power Supply. This pin connects to an isolated +3.3V power supply; relative to the 0V.
2	0V	0V. This pin is the return path for the isolated V _{DD} and V _{EE} power supplies, and the PORT1 - 4 outputs.
3		
4	V _{EE}	Main Power Supply. This pin connects to an isolated -45V to -57V supply; relative to the 0V.
5		
6	MODE	Mode Select Input. A Logic 1 on this pin will set the Ag6400 in Hardware mode. A Logic 0 on this pin will set the Ag6400 in Software mode. Internally pulled down to 0V.
7	MID	Midspan Mode Input. A Logic 1 on the pin will set the Ag6400 to act as a PSE Midspan. Internally pulled down to 0V.
8	/INT	Interrupt Output. This open drain output will pull low when one of the programmed interrupt events has occurred.
9	SDO	Serial Data Output. This open drain output is used in conjunction with the SDI and SCL pins to for the I ² C bus.
10	SCL	Serial Clock Input. This high impedance input pin connects to the I ² C bus clock.
11	SDI	Serial Data Input. This high impedance input pin is used in conjunction with the SDO and SCL pins to for the I ² C bus.
12	AD3	Address Input Bit 3. The input is used in conjunction with AD0, AD1 and AD2 to set the I ² C address of the Ag6400.
13	AD2	Address Input Bit 2. The input is used in conjunction with AD0, AD1 and AD3 to set the I ² C address of the Ag6400.
14	AD1	Address Input Bit 1. The input is used in conjunction with AD0, AD2 and AD3 to set the I ² C address of the Ag6400.
15	AD0	Address Input Bit 0. The input is used in conjunction with AD1, AD2 and AD3 to set the I ² C address of the Ag6400.
16	NC	No Connection.
17	PORT1	PORT1 Output. This output pin monitors the line and supplies power to valid powered device.
18	PORT2	PORT2 Output. This output pin monitors the line and supplies power to valid powered device.
19	PORT3	PORT3 Output. This output pin monitors the line and supplies power to valid powered device.
20	PORT4	PORT4 Output. This output pin monitors the line and supplies power to valid powered device.

5. Functional Description

5.1 Power Supplies

The Ag6400 requires two power supplies V_{DD} and V_{EE} , it is very important that the V_{DD} supply is powered up before the V_{EE} supply. Failure to do so may result in damage to the controller chip on the module.

To conform to the IEEE802.3at specification, both V_{DD} and V_{EE} must be isolated from ground, as shown in Figure 3.

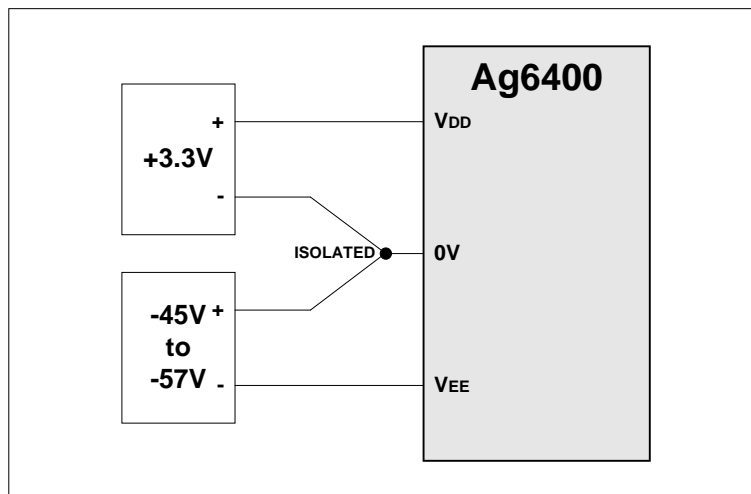


Figure 3: Power Supply Connections

5.2 Output Ports

Each output port can be connected directly to the centre-tap of an IEEE802.3at compliant data transformer or to the spare pair connection for 10/100BASE-T applications, as shown in Figure 4. For 1000BASE-T (Gigabit) Ethernet applications all four cable pairs require magnetics, this is explained in more detail in application note "ANX-1000BASE-T-CONNECTIONS".

It is important that the (return) star point is kept as close to the 0V pins (on the module) as possible.

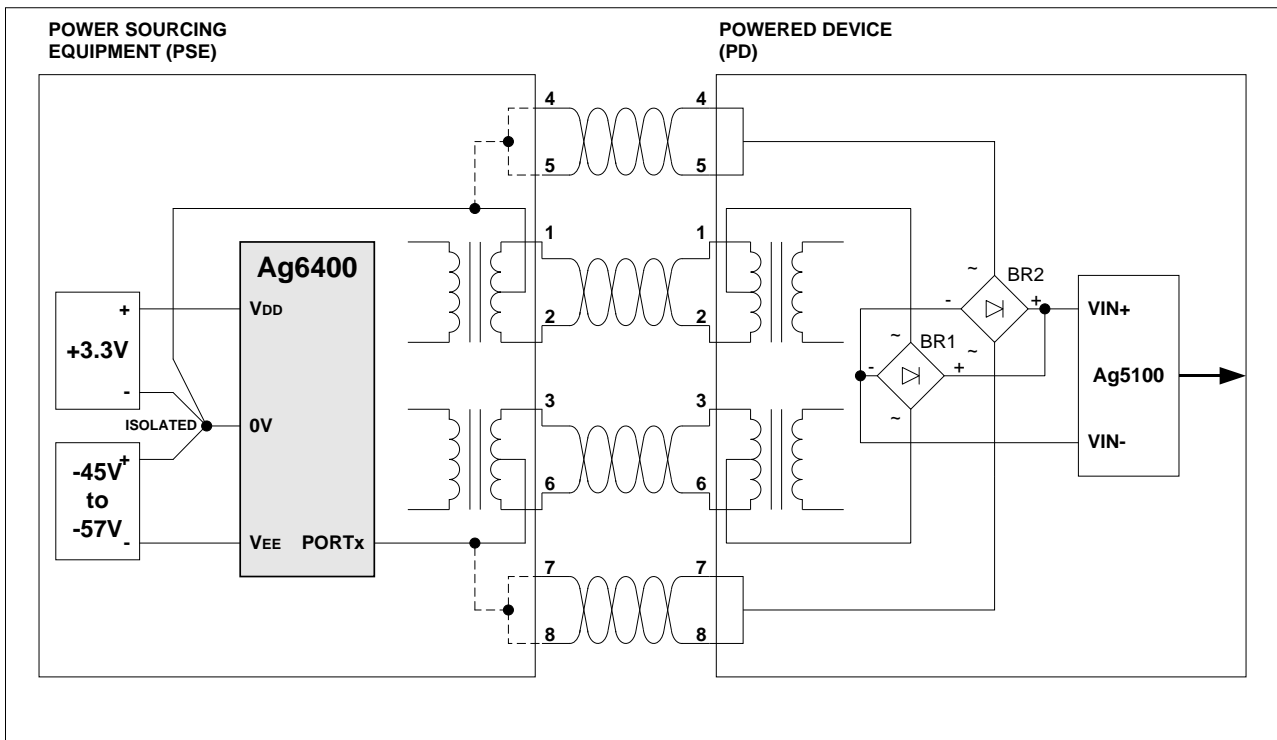


Figure 4: Typical Connection Diagram

5.3 Selection Inputs

The Ag6400 has two mode selection input pins – “MID” and “MODE”.

5.3.1 MID

To use the Ag6400 as a Midspan device, the MID pin must be set to a Logic 1 during power up (setting Midspan mode). This mode continues to support the 2-event classification and includes a two second back-off timer between port detection cycles. For Endpoint devices the MID pin must be set to Logic 0.

5.3.2 MODE

When the Ag6400 is powered up with Logic 1 applied to the MODE pin, the Ag6400 will be set in Hardware mode (this is the easiest mode to use).

In Hardware mode the Ag6400 does not require any user intervention. It will automatically detect and classify ports, apply power after successful detections, and remove power from disconnected ports. For most applications it is recommended to use Hardware Mode.

The Cutoff Current (I_{CUT}) and Current Limit (I_{LIM}) parameters are set in accordance with the detected classification, see Table 2.

	Class 1		Class 2		Class 3 or 0		Class 4 (two event)	
	current	hex	current	hex	current	hex	current	hex
I _{CUT}	112mA	C6h	206mA	CBh	375mA	D4h	638mA	E2h
I _{LIM}	425mA	80h	425mA	80h	425mA	80h	850mA	C0h

Table 2: Hardware Mode Current Settings

When the Ag6400 is powered up with Logic 0 applied to the MODE pin, the Ag6400 will be set in Software mode and is fully controlled using the I²C interface. The Ag6400 should be set in this mode if the Data Link Layer classification is required.

5.4 I²C Interface

The Ag6400 is a slave device, with four pins available to connect to an I²C interface – SDI, SDO, SCL and /INT. The module can communicate with a master device using the I²C bus standard. To implement a standard bidirectional SDA bus, the SDO and SDI must be connected together. These pins have been separated to make it easier to connect them to opto-couplers to implement an isolation barrier, as shown in Figure 8.

5.4.1 I²C Timing

The following Figures show the timing relationship between the SCL and SDA signals.

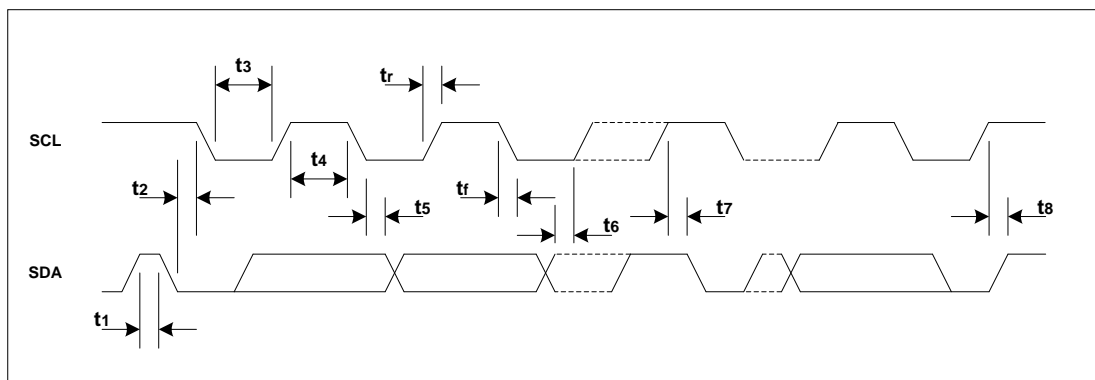


Figure 5: I²C Interface Timing

Figure 6 shows how to write to a register.

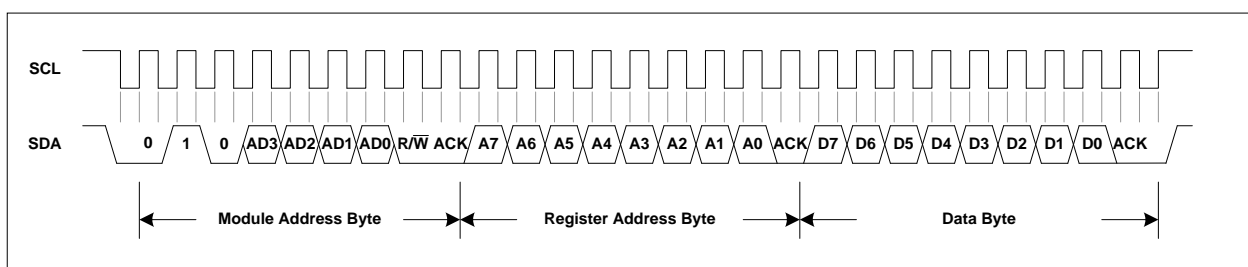


Figure 6: Writing to a Register

Figure 7 shows how to read a register.

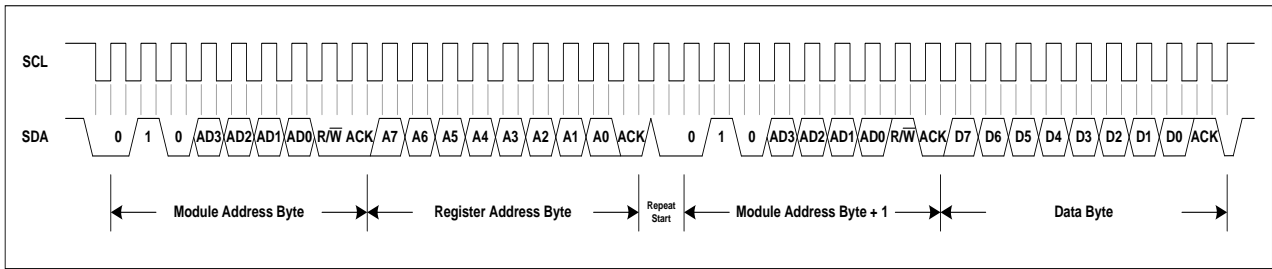


Figure 7: Read a Register

The Ag6400 is non-isolated, so to fully conform to the IEEE specification the V_{DD} and V_{EE} supplies must be isolated from chassis ground. If the controller is powered by a ground referenced power supply, then the I²C bus must be isolated. Although the output ports (on one or more Ag6400's) do not have to be isolated from each other. Figure 8 shows how the I²C bus can be implemented by using opto-isolators to form an isolation barrier, where the controller GND is isolated from the Ag6400 0V.

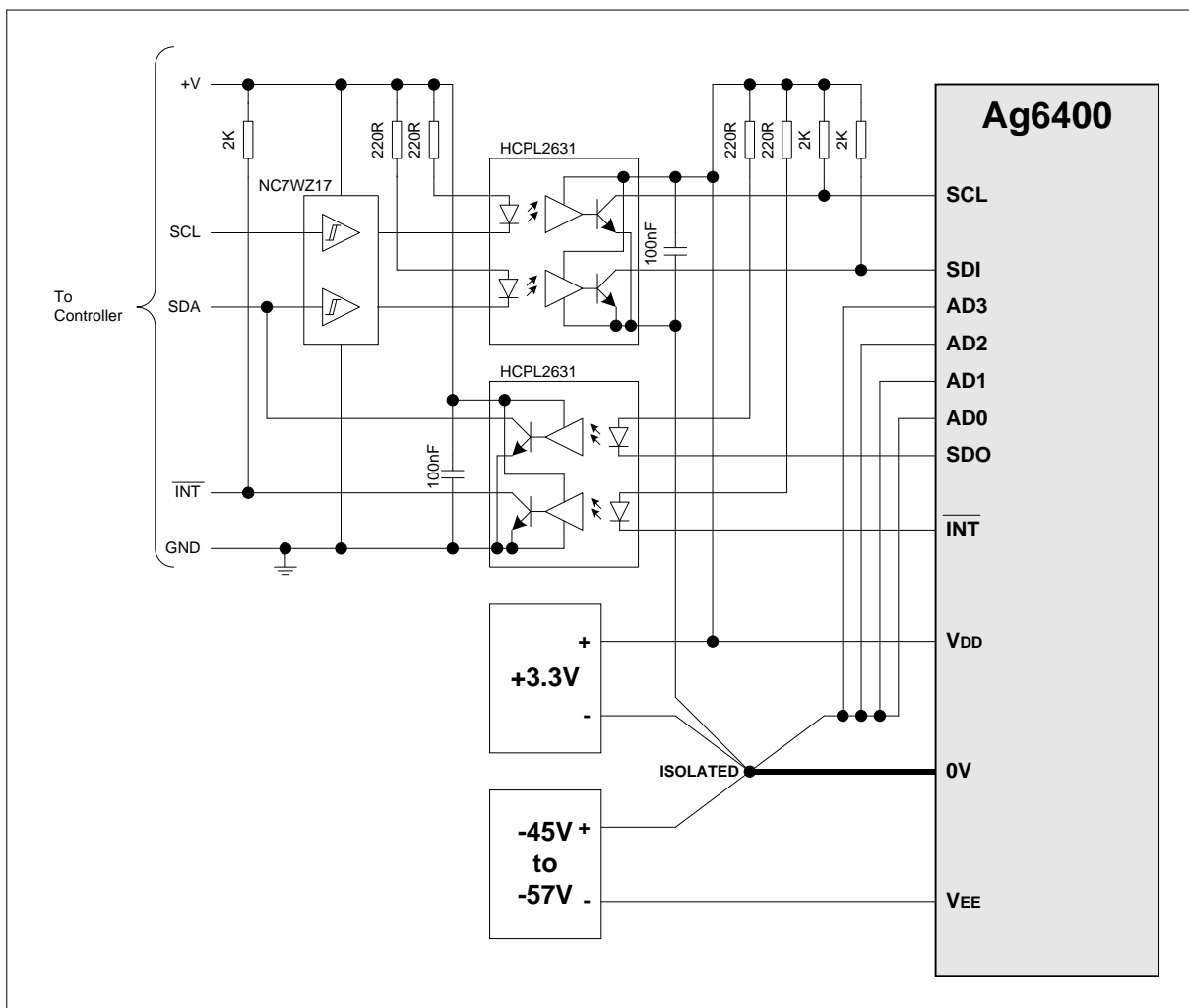


Figure 8: Isolated I²C bus

5.4.2 I²C Module Address

The module address is programmed by using the AD0 to AD3 pins, allowing several Ag6400 modules to be connected to the I²C bus; Table 3 shows the address format.

Module Address	MSB			AD3	AD2	AD1	AD0	LSB
	0	1	0					R/W

Table 3: Module Address

In the example shown in Figure 8, AD0 to AD3 are all connected to 0V (Logic 0). Therefore to write to the module the base address is 40h “01000000” (even), to read from the module the address is 41h, base address + 1 (odd). Each ADn input has an internal 50kΩ pull-up resistor

The interrupt pin (/INT) is only updated between I²C trans-actions and the SDA and SCL line must be set to Logic 1 when the bus is not in use.

6. Signature and Classification

The Ag6400 will automatically perform the Signature and Classification in Hardware or Software mode (when enabled). Figure 9 shows the full timing sequence for a Type 2 Powered Device (PD).

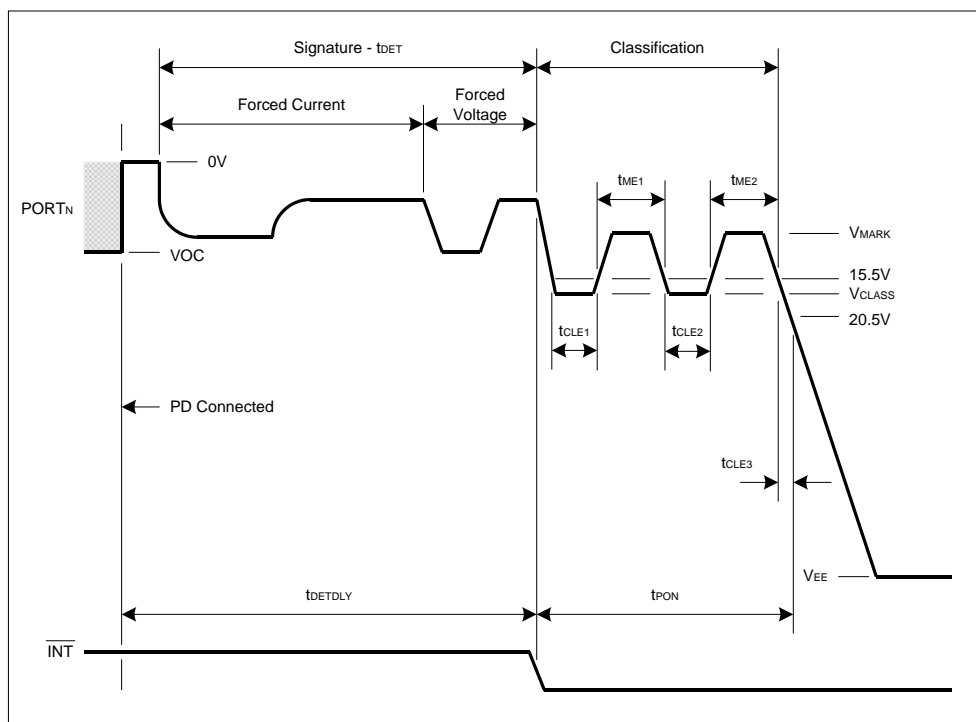


Figure 9: Signature, Class and Turn-On Timing - Type 2 PD

The Ag6400 has a different response when connected to a Type 1 PD, see Figure 10 (Hardware mode).

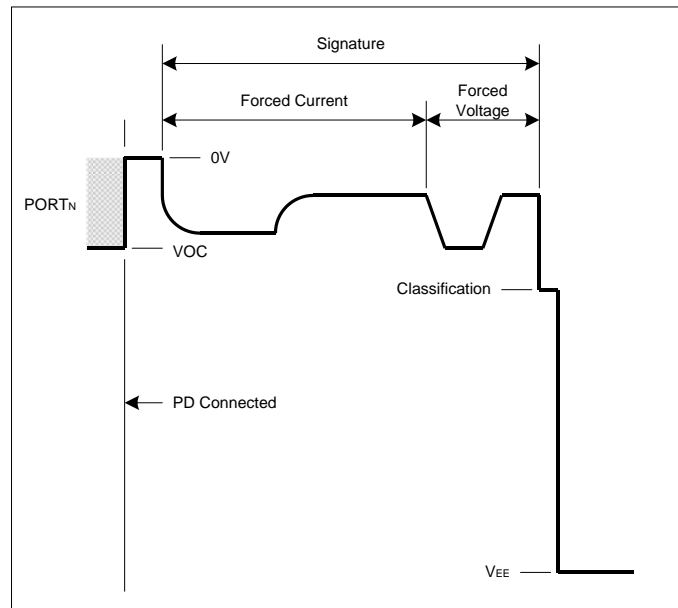


Figure 10: Signature, Class and Turn-On Timing - Type 1 PD

The IEEE802.3at separates the power handling into two basic categories “Type 1” and “Type 2”. In simple terms Type 1 handles power requirements up to 15.4W and is comparable with the IEEE802.3af specification. Type 2 handles the power levels above this, which is commonly referred to as POE+.

6.1 Signature Detection

To ensure that the Ag6400 does not apply power to a non PoE enabled device the output port first checks for a valid PoE signature. The PD should present 25kΩ (23.75kΩ to 26.25kΩ) Signature resistance, but this usually has a dc offset from the polarity protection circuit (0V to 2V).

The Ag6400 checks for a 25kΩ slope and the dc offset voltage by using a 4 point detection method. The first and second points are measured by forcing a current; if these are valid the port will continue with the third and fourth points which force a voltage. From these points the resistive slope and the offset voltage is calculated and tested.

Figure 11 shows a valid signature slope. If the first forced current result measures <1V, the test will be aborted and the relevant port status register bits 0 to 2 will report a “Short Circuit”. A full list of the port status register signature bit setting is shown in Table 4.

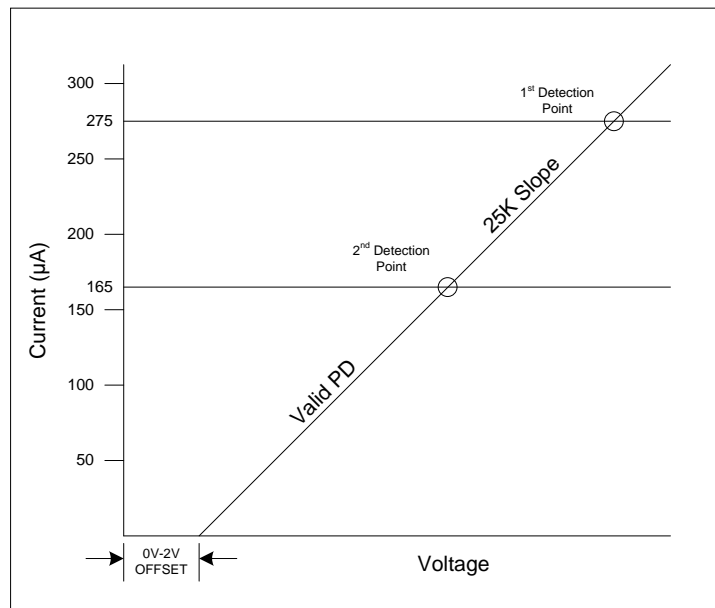


Figure 11: Signature Slope

Bits			Description
2	1	0	
0	0	0	Unknown
0	0	1	Short circuit
0	1	0	PD Input Capacitance (C_{PD}) is too high
0	1	1	Signature Resistance (R_{SIG}) is too low
1	0	0	Signature is valid
1	0	1	R_{SIG} is too high
1	1	0	Open circuit
1	1	1	Port offset voltage is too high

Table 4: Port Status Register – Signature Bits 0 - 2

6.2 Classification

On completion of a valid signature, the Ag6400 will then interrogate the PD to see if a classification signature is present. The classification signature is used to determine the amount of power the PD will draw and limits the output power accordingly (see Table 5). It is optional for the PD to present a classification signature and the Ag6400 will default to Class 0 if the PD does not present one.

The PD presents a classification signature in the form of a constant current load when a PSE port applies a voltage between 15.5V to 20.5V.

Table 5 shows the measured current limits that the Ag6400 uses to assign a classification value.

Measured Current	Classification
0mA to 6.5mA	Class 0
>6.5mA to 14.5mA	Class 1
>14.5mA to 23mA	Class 2
>23mA to 33mA	Class 3
>33mA to 48mA	Class 4
>48mA	Over Current

Table 5: Classification Table

The classification result is reported in bits 4 to 6 of the port status register; these are shown in Table 6.

Bits			Description
6	5	4	
0	0	0	Unknown
0	0	1	Class 1
0	1	0	Class 2
0	1	1	Class 3
1	0	0	Class 4
1	0	1	Reserved
1	1	0	Class 0
1	1	1	Over Current

Table 6: Port Status Register – Classification Bits 4 - 6

The Ag6400 supports 2-event classification required to supply the higher power to a Type 2 PD. When the port detects a Class 4 current, it backs off to a mark voltage level and then makes a second classification measurement. Providing both measurements draw Class 4 current the Ag6400 will set that port to deliver the power levels shown in Table 2.

6.3 Current Cutoff and Limits

When a port has successfully completed the Signature and Classification; the main power will be turned on. The main power is current limited by two parameters I_{CUT} and I_{LIM} . Table 2 show the values assigned to these parameters in Hardware mode. These are the recommend values that should set in Software mode.

The I_{LIM} parameter sets the maximum current that can be delivered from a port. If this is set to 850mA and the PD attempts to draw 1A, then the Ag6400 will current limit that port at 850mA. Table 7 gives a list of I_{LIM} current limit settings that can be programmed into the lim_N registers; the Type 1 and Type 2 default parameters are highlighted.

I_{LIM} (mA)	Setting (hex)
106	88
213	08
359	89
425	80
531	8A
638	90
744	9A
850	C0
956	CA
1063	D0
1169	DA
1275	D1
1381	DB
1488	49
1700	40

Table 7: I_{LIM} Current Limit Settings

The second parameter is I_{CUT}, this lower than I_{LIM} and sets the cutoff operating current for a port. Short transients are allowed to exceed I_{CUT} (limited by I_{LIM}), to handle load step changes from the PD. But if the PD continually exceeds I_{CUT} the Ag6400 will shut down that port.

The i_{CUT} registers have a 6 bit resolution, in normal mode the Least Significant Bit (LSB) = 18.75mA, giving a programming range up to 1181mA. These registers also have a double bit and when this is cleared (= 0), the LSB = 37.5mA, increasing the programming range up to 2363mA.

7. Software Mode

If you require the Ag6400 to respond to the Data Link Layer (DLL) communication noted in the IEEE802.3at specification, the Ag6400 must be configured in software mode. In hardware mode providing the Ag6400 sees a Class 4 signature it will automatically supply the higher output current (see Table 2). The PSE uses the DLL communication to confirm that the product is indeed a Type 2 product but this is not required for compliance.

The detail of the Data Link Layer structure is detailed in the IEEE802.3at specification.

7.1 Register Map

The Register Map is shown in Table 8, the following list shows the R/W codes: -

- CoR = Clear on Read: Register cleared after a read (writing to the register has no effect).
- R/W = Read/Write: Register can be read (without affecting the register) or written to.
- RO = Read Only: Register can be read without affecting the register (writing to the register has no effect).
- SO = Set Only: Register can be written to (data read from the register is meaningless).

Addr	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mode = 0	Mode = 1	
Interrupt Registers													
00h	int	RO	supply	t _{START}	t _{CUT}	class	det	dis	pgd	per	1000 0000	1000 0000	
01h	intmask	R/W	supply	t _{START}	t _{CUT}	class	det	dis	pgd	per	1000 0000	1110 0100	
Event Registers													
02h	per	RO	pgd4	pgd3	pgd2	pgd1	psc4	psc3	psc2	psc1	0000 0000	0000 0000	
03h	per_cor	CoR	pgd4	pgd3	pgd2	pgd1	psc4	psc3	psc2	psc1	0000 0000	0000 0000	
04h	det	RO	class4	class3	class2	class1	sig4	sig3	sig2	sig1	0000 0000	0000 0000	
05h	det_cor	CoR	class4	class3	class2	class1	sig4	sig3	sig2	sig1	0000 0000	0000 0000	
06h	fer	RO	dis4	dis3	dis2	dis1	t _{CUT4}	t _{CUT3}	t _{CUT2}	t _{CUT1}	0000 0000	0000 0000	
07h	fer_cor	CoR	dis4	dis3	dis2	dis1	t _{CUT4}	t _{CUT3}	t _{CUT2}	t _{CUT1}	0000 0000	0000 0000	
08h	tsr	RO	t _{LIM4}	t _{LIM3}	t _{LIM2}	t _{LIM1}	t _{START4}	t _{START3}	t _{START2}	t _{START1}	0000 0000	0000 0000	
09h	tsr_cor	CoR	t _{LIM4}	t _{LIM3}	t _{LIM2}	t _{LIM1}	t _{START4}	t _{START3}	t _{START2}	t _{START1}	0000 0000	0000 0000	
0Ah	ser	RO	temp	-	uvlo3	uvlo48	-	-	-	-	0011 0010	0011 0010	
0Bh	ser_cor	CoR	temp	-	uvlo3	uvlo48	-	-	-	-	0011 0010	0011 0010	
Status Registers													
0Ch	psr1	RO	-	class[2:0]		-	-	detect[2:0]		-	0000 0000	0000 0000	
0Dh	psr2	RO	-	class[2:0]		-	-	detect[2:0]		-	0000 0000	0000 0000	
0Eh	psr3	RO	-	class[2:0]		-	-	detect[2:0]		-	0000 0000	0000 0000	
0Fh	psr4	RO	-	class[2:0]		-	-	detect[2:0]		-	0000 0000	0000 0000	
10h	pwsr	RO	pg4	pg3	pg2	pg1	pe4	pe3	pe2	pe1	0000 0000	0000 0000	
11h	pinsr	RO	-	-	ad3	ad2	ad1	ad0	mid	mode	00xx xxx0	00xx xxx1	
Configuration Registers													
12h	omr	R/W	omp4[1:0]		omp3[1:0]		omp2[1:0]		omp1[1:0]		0000 0000	1111 1111	
13h	disenr	R/W	e_ac4	e_ac3	e_ac2	e_ac1	dc4	dc3	dc2	dc1	0000 0000	1111 0000	
14h	dcenr	R/W	cep4	cep3	cep2	cep1	dep4	dep3	dep2	dep1	0000 0000	1111 1111	
15h	midspan	R/W	-	-	-	-	mid4	mid3	mid2	mid1	0000 0000	0000 MMMM	
16h	tr	R/W	-	-	t _{START} [1:0]		t _{CUT} [1:0]		t _{DIS} [1:0]		0000 0000	0000 0000	
17h	conf	R/W	inten	detchg	-	-	-	-	-	-	1010 0000	1010 0000	
Action Registers													
18h	detar	SO	cls4	cls3	cls2	cls1	det4	det3	det2	det1	0000 0000	0000 0000	
19h	pwr	SO	off4	off3	off2	off1	on4	on3	on2	on1	0000 0000	0000 0000	
1Ah	reset	SO	allclr	intclr	-	allrst	rst4	rst3	rst2	rst1	0000 0000	0000 0000	
Limit Timing Registers													
1Eh	tlim12	R/W	t _{LIM2} [3:0]				t _{LIM1} [3:0]				0000 0000	0000 0000	
1Fh	tlim34	R/W	t _{LIM4} [3:0]				t _{LIM3} [3:0]				0000 0000	0000 0000	
Port Measurement Registers													
30h	ip1lsb	RO					ip1lsb[7:0]				0000 0000	0000 0000	
31h	ip1msb	RO					ip1msb[7:0]				0000 0000	0000 0000	
32h	vp1lsb	RO					vp1lsb[7:0]				0000 0000	0000 0000	
33h	vp1msb	RO					vp1msb[7:0]				0000 0000	0000 0000	
34h	ip2lsb	RO					ip2lsb[7:0]				0000 0000	0000 0000	
35h	ip2msb	RO					ip2msb[7:0]				0000 0000	0000 0000	
36h	vp2lsb	RO					vp2lsb[7:0]				0000 0000	0000 0000	
37h	vp2msb	RO					vp2msb[7:0]				0000 0000	0000 0000	
38h	ip3lsb	RO					ip3lsb[7:0]				0000 0000	0000 0000	
39h	ip3msb	RO					ip3msb[7:0]				0000 0000	0000 0000	
3Ah	vp3lsb	RO					vp3lsb[7:0]				0000 0000	0000 0000	
3Bh	vp3msb	RO					vp3msb[7:0]				0000 0000	0000 0000	
3Ch	ip4lsb	RO					ip4lsb[7:0]				0000 0000	0000 0000	
3Dh	ip4msb	RO					ip4msb[7:0]				0000 0000	0000 0000	
3Eh	vp4lsb	RO					vp4lsb[7:0]				0000 0000	0000 0000	
3Fh	vp4msb	RO					vp4msb[7:0]				0000 0000	0000 0000	
Power Management Registers													
44h	pen	R/W	-	-	-	-	pen4	pen3	pen2	pen1	0000 0000	0000 1111	
46h	pm1	R/W	-	-	-	-	-	-	legen1	cl4en1	0000 0000	0000 0001	
47h	icut1	R/W	rdis	cutdbl	icut[5:0]						0001 0100	1101 0100	
48h	ilim1	R/W	ilim[7:0]									0000 0000	0000 0000
49h	pstat1	R/W	-	-	-	-	-	-	-	cl4det1	0000 0000	0000 0000	
4Bh	pm2	R/W	-	-	-	-	-	-	legen2	cl4en2	0000 0000	0000 0001	
4Ch	icut2	R/W	rdis	cutdbl	icut[5:0]						0001 0100	1101 0100	
4Dh	ilim2	R/W	ilim[7:0]									0000 0000	0000 0000
4Eh	pstat2	R/W	-	-	-	-	-	-	-	cl4det2	0000 0000	0000 0000	
50h	pm3	R/W	-	-	-	-	-	-	legen3	cl4en3	0000 0000	0000 0001	
51h	icut3	R/W	rdis	cutdbl	icut[5:0]						0001 0100	1101 0100	
52h	ilim3	R/W	ilim[7:0]									0000 0000	0000 0000
53h	pstat3	R/W	-	-	-	-	-	-	-	cl4det3	0000 0000	0000 0000	
55h	pm4	R/W	-	-	-	-	-	-	legen4	cl4en4	0000 0000	0000 0001	
56h	icut4	R/W	rdis	cutdbl	icut[5:0]						0001 0100	1101 0100	
57h	ilim4	R/W	ilim[7:0]									0000 0000	0000 0000
58h	pstat4	R/W	-	-	-	-	-	-	-	cl4det4	0000 0000	0000 0000	

Table 8: Register Map

M = State of the MID pin.

7.1.1 Interrupt Registers

There are two registers that are directly associated with the Ag6400 interrupt:-

int (Address 00h): Interrupt Status Register.

This is a Read only register; that monitors the status of the event registers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
supply	t _{START}	t _{CUT}	class	det	dis	pgd	per

Bits	Symbol	Description
0	per	Power Enable Interrupt: Set if any of the power event interrupt register (02h) psc _N bits are set.
1	pgd	Power Good Interrupt: Set if any of the power event interrupt register (02h) pgd _N bits are set.
2	dis	Disconnect Interrupt: Set if any of the event interrupt register (06h) t _{CUTN} bits are set.
3	det	Detect Interrupt: Set if any of the detect event register (04h) sig _N bits are set.
4	class	Class Interrupt: Set if any of the detect event register (04h) class _N bits are set.
5	t _{CUT}	t _{CUT} Interrupt: Set if any of the t _{CUT} event register (06h) dis _N bits are set
6	t _{START}	t _{START} Interrupt: Set if any of the t _{START} event register (08h) bits are set
7	supply	Power Interrupt: Set if any of the supply event register (0Ah) bits are set

intmask (Address 01h): Interrupt Mask Register.

This is a Read/Write register; that controls which events will pull the /INT pin low.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
supply	t _{START}	t _{CUT}	class	det	dis	pgd	per

Bits	Symbol	Description
0	per	A Power Enable event will pull the /INT pin low.
1	pgd	A Power Good event will pull the /INT pin low.
2	dis	A Disconnect event will pull the /INT pin low.
3	det	A Detect event will pull the /INT pin low.
4	class	A Class event will pull the /INT pin low.
5	t _{CUT}	A t _{CUT} event will pull the /INT pin low.
6	t _{START}	A t _{START} event will pull the /INT pin low.
7	supply	A Supply event will pull the /INT pin low.

7.1.2 Event Registers

There are ten event registers that are associated with the Ag6400 interrupt registers:-

per (Address 02h): Power Event Register.

This is a Read only register; the four lower bits indicate if a port has been turned on or off. The four upper bits indicate if the power good status has changed (see pwsr register 10h).

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
pgd4	pgd3	pgd2	pgd1	psc4	psc3	psc2	psc1

Bits	Symbol	Description
0	psc1	Port 1 power status change
1	psc2	Port 2 power status change
2	psc3	Port 3 power status change
3	psc4	Port 4 power status change
4	pgd1	Port 1 power good change
5	pgd2	Port 2 power good change
6	pgd3	Port 3 power good change
7	pgd4	Port 4 power good change

per_cor (Address 03h): Power Event Register.

This is a Clear on Read register; it is identical to “per” register (02h) except that reading from this register clears both the “per” and “per_cor” registers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
pgd4	pgd3	pgd2	pgd1	psc4	psc3	psc2	psc1

Bits	Symbol	Description
0	psc1	Port 1 power status change
1	psc2	Port 2 power status change
2	psc3	Port 3 power status change
3	psc4	Port 4 power status change
4	pgd1	Port 1 power good change
5	pgd2	Port 2 power good change
6	pgd3	Port 3 power good change
7	pgd4	Port 4 power good change

det (Address 04h): Detect and Classification Event Register.

This is a Read only register; the four lower bits indicate that the port signature detection has completed. The four upper bits indicate that the port classification has completed. The results for each port are shown in the psr_N registers (0Ch to 0Fh).

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
class4	class3	class2	class1	sig4	sig3	sig2	sig1

Bits	Symbol	Description
0	sig1	Port 1 signature detection complete
1	sig2	Port 2 signature detection complete
2	sig3	Port 3 signature detection complete
3	sig4	Port 4 signature detection complete
4	class1	Port 1 classification complete
5	class2	Port 2 classification complete
6	class3	Port 3 classification complete
7	class4	Port 4 classification complete

det_cor (Address 05h): Detect and Classification Event Register.

This is a Clear on Read register; it is identical to “det” register (04h) except that reading from this register clears both the “det” and “det_cor” registers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
class4	class3	class2	class1	sig4	sig3	sig2	sig1

Bits	Symbol	Description
0	sig1	Port 1 signature detection complete
1	sig2	Port 2 signature detection complete
2	sig3	Port 3 signature detection complete
3	sig4	Port 4 signature detection complete
4	class1	Port 1 classification complete
5	class2	Port 2 classification complete
6	class3	Port 3 classification complete
7	class4	Port 4 classification complete

fer (Address 06h): Fault Event Register.

This is a Read only register; the four lower bits indicate that the port has been turned off because the port current was above i_{CUT} . The upper four bits are set when the port current falls below 5mA.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
dis4	dis3	dis2	dis1	t_{CUT4}	t_{CUT3}	t_{CUT2}	t_{CUT1}

Bits	Symbol	Description
0	t_{CUT1}	Port 1 over-current timeout. While the port was powered the output current exceeded (i_{CUT}) for longer than (t_{CUT})
1	t_{CUT2}	Port 2 over-current timeout
2	t_{CUT3}	Port 3 over-current timeout
3	t_{CUT4}	Port 4 over-current timeout
4	dis1	Port 1 disconnect timeout (t_{DIS})
5	dis2	Port 2 disconnect timeout (t_{DIS})
6	dis3	Port 3 disconnect timeout (t_{DIS})
7	dis4	Port 4 disconnect timeout (t_{DIS})

fer_cor (Address 07h): Fault Event Register.

This is a Clear on Read register; it is identical to “fer” register (06h) except that reading from this register clears both the “fer” and “fer_cor” registers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
dis4	dis3	dis2	dis1	t_{CUT4}	t_{CUT3}	t_{CUT2}	t_{CUT1}

Bits	Symbol	Description
0	t_{CUT1}	Port 1 over-current timeout. While the port was powered the output current exceeded (i_{CUT}) for longer than (t_{CUT})
1	t_{CUT2}	Port 2 over-current timeout
2	t_{CUT3}	Port 3 over-current timeout
3	t_{CUT4}	Port 4 over-current timeout
4	dis1	Port 1 disconnect timeout (t_{DIS})
5	dis2	Port 2 disconnect timeout (t_{DIS})
6	dis3	Port 3 disconnect timeout (t_{DIS})
7	dis4	Port 4 disconnect timeout (t_{DIS})

tsr (Address 08h): t_{START} Event Register.

This is a Read only register; the four lower bits indicate an over-current fault. The upper four bits indicate that the port has been turned off because the port current was above i_{LIM} .

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
t_{LIM4}	t_{LIM3}	t_{LIM2}	t_{LIM1}	t_{START4}	t_{START3}	t_{START2}	t_{START1}

Bits	Symbol	Description
0	t_{START1}	Port 1 start-up over-current timeout (t_{START}). While turning on the port the PD has drawn more than 375mA for longer than t_{START} causing the port to turn off
1	t_{START2}	Port 2 start-up over-current timeout (t_{START})
2	t_{START3}	Port 3 start-up over-current timeout (t_{START})
3	t_{START4}	Port 4 start-up over-current timeout (t_{START})
4	t_{LIM1}	Port 1 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM1} field of the $tlim12$ register (1Eh)
5	t_{LIM2}	Port 2 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM2} field of the $tlim12$ register (1Eh)
6	t_{LIM3}	Port 3 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM3} field of the $tlim34$ register (1Fh)
7	t_{LIM4}	Port 4 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM4} field of the $tlim34$ register (1Fh)

tsr_cor (Address 09h): t_{START} Event Register.

This is a Clear on Read register; it is identical to “tsr” register (08h) except that reading from this register clears both the “tsr” and “tsr_cor” registers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
t_{LIM4}	t_{LIM3}	t_{LIM2}	t_{LIM1}	t_{START4}	t_{START3}	t_{START2}	t_{START1}

Bits	Symbol	Description
0	t_{START1}	Port 1 start-up over-current timeout (t_{START}). While turning on the port the PD has drawn more than 375mA for longer than t_{START} causing the port to turn off
1	t_{START2}	Port 2 start-up over-current timeout (t_{START})
2	t_{START3}	Port 3 start-up over-current timeout (t_{START})
3	t_{START4}	Port 4 start-up over-current timeout (t_{START})
4	t_{LIM1}	Port 1 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM1} field of the $tlim12$ register (1Eh)
5	t_{LIM2}	Port 2 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM2} field of the $tlim12$ register (1Eh)
6	t_{LIM3}	Port 3 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM3} field of the $tlim34$ register (1Fh)
7	t_{LIM4}	Port 4 current limit timeout. The length of the current limit (t_{LIM}) is controlled by the t_{LIM4} field of the $tlim34$ register (1Fh)

ser (Address 0Ah): Supply Event Register.

This is a Read only register; the bits in this register are set when a problem occurs with the power supplies or temperature.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
temp	-	uvlo3	uvlo48	-	-	-	-

Bits	Symbol	Description
0	-	Reserved
1	-	Reserved
2	-	Reserved
3	-	Reserved
4	uvlo48	V_{EE} Under Voltage Lock Out (UVLO). Set when the V_{EE} supply is too low for normal operation.
5	uvlo3	V_{DD} UVLO. Set when the V_{DD} supply is too low for normal operation.
6	-	Reserved
7	temp	Over Temperature. Set when the controller temperature is too high. If set, signature and class must be re-enabled manually.

ser_cor (Address 0Bh): Supply Event Register.

This is a Clear on Read register; it is identical to “ser” register (0Ah) except that reading from this register clears both the “ser” and “ser_cor” registers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
temp	-	uvlo3	uvlo48	-	-	-	-

Bits	Symbol	Description
0	-	Reserved
1	-	Reserved
2	-	Reserved
3	-	Reserved
4	uvlo48	V_{EE} Under Voltage Lock Out (UVLO). Set when the V_{EE} supply is too low for normal operation.
5	uvlo3	V_{DD} UVLO. Set when the V_{DD} supply is too low for normal operation.
6	-	Reserved
7	temp	Over Temperature. Set when the controller temperature is too high. If set, signature and class must be re-enabled manually.

7.1.3 Status Registers

There are six status registers that are used by the Ag6400:-

psr1 (Address 0Ch): Port1 Status Register.

This is a Read only register; that shows the results of the signature and classification measurements for Port 1.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	class[2:0]			-	detect[2:0]		

Bits	Symbol	Description
2:0	detect	See Table 9
3	-	Reserved
6:4	class	See Table 10
7	-	Reserved

detect[2:0]			Description
detect[2]	detect[1]	detect[0]	
0	0	0	Unknown
0	0	1	Short
0	1	0	Cpd too high
0	1	1	R _{SIG} low
1	0	0	Good
1	0	1	R _{SIG} high
1	1	0	Open
1	1	1	Reserved

Table 9: Signature Results

class[2:0]			Description
detect[2]	detect[1]	detect[0]	
0	0	0	Unknown
0	0	1	Class 1
0	1	0	Class 2
0	1	1	Class 3
1	0	0	Class 4
1	0	1	Reserved
1	1	0	Class 0
1	1	1	Over Current

Table 10: Classification Results

psr2 (Address 0Dh): Port2 Status Register.

This is a Read only register; that shows the results of the signature and classification measurements for Port 2.

See psr1 for full details.

psr3 (Address 0Eh): Port3 Status Register.

This is a Read only register; that shows the results of the signature and classification measurements for Port 3.

See psr1 for full details.

psr4 (Address 0Fh): Port4 Status Register.

This is a Read only register; that shows the results of the signature and classification measurements for Port 3.

See psr1 for full details.

pwsr (Address 10h): Power Status Register.

This is a Read only register; that shows the power status of each port.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
pg4	pg3	pg2	pg1	pe4	pe3	pe2	pe1

Bits	Symbol	Description
0	pe1	Power enabled on port 1
1	pe2	Power enabled on port 2
2	pe3	Power enabled on port 3
3	pe4	Power enabled on port 4
4	pg1	Power good on port 1
5	pg2	Power good on port 2
6	pg3	Power good on port 3
7	pg4	Power good on port 4

pinsr (Address 11h): Pin Status Register.

This is a Read only register; that shows the logic state of the hardware input pin.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	ad3	ad2	ad1	ad0	mid	mode

Bits	Symbol	Description
0	mode	MODE pin logic state
1	mid	MID pin logic state
2	ad0	AD0 pin logic state
3	ad1	AD1 pin logic state
4	ad2	AD2 pin logic state
5	ad3	AD3 pin logic state
6	-	Reserved
7	-	Reserved

7.1.4 Configuration Registers

There are six configuration registers that are used by the Ag6400:-

omr (Address 12h): Operating Mode Register.

This is a Read/Write register; that shows and can set the operating mode of the Ag6400.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
omp4[1:0]		omp3[1:0]		omp2[1:0]		omp1[1:0]	

Bits	Symbol	Description
1:0	omp1	Operating mode, port 1
3:2	omp2	Operating mode, port 2
5:4	omp3	Operating mode, port 3
7:6	omp4	Operating mode, port 4

omp _N [1:0]		Description
omp _N [1]	omp _N [0]	
0	0	Shutdown
0	1	Manual*
1	0	Software
1	1	Hardware

Table 11: Classification Results

*Note: The Manual mode is a further extension of Software mode, where the Ag6400 require full control over the I²C Bus.

disenr (Address 13h): Disconnect Sensing Enable Register.

This is a Read/Write register; that enables the port disconnect feature of the Ag6400. When using DC disconnect, if the port current is <5mA (for t_{DIS}) the port will be turned off.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
e-ac4	e-ac3	e-ac2	e-ac1	dc4	dc3	dc2	dc1

Bits	Symbol	Description
0	dc1	Enables DC disconnect on port 1
1	dc2	Enables DC disconnect on port 2
2	dc3	Enables DC disconnect on port 3
3	dc4	Enables DC disconnect on port 4
4	e-ac1	Emulates AC disconnect on port 1
5	e-ac2	Emulates AC disconnect on port 2
6	e-ac3	Emulates AC disconnect on port 3
7	e-ac4	Emulates AC disconnect on port 4

dcenr (Address 14h): Detect and Class Enable Register.

This is a Read/Write register; that enables the PD signature and classification on each port. These bits can also be set by writing to the “detar” register (18h). The behaviour of this port will depend on the settings on the “omr” register (12h).

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
cep4	cep3	cep2	cep1	dep4	dep3	dep2	dep1

Bits	Symbol	Description
0	dep1	Enable signature on port 1*
1	dep2	Enable signature on port 2*
2	dep3	Enable signature on port 3*
3	dep4	Enable signature on port 4*
4	cep1	Enable classification on port 1*
5	cep2	Enable classification on port 2*
6	cep3	Enable classification on port 3*
7	cep4	Enable classification on port 4*

*Note: In Hardware or Software modes the Ag6400 will periodically detect and report the result. In Manual mode when this bit is set the Ag6400 will only perform this operation once, this bit will be cleared. In Shutdown mode this bit has no effect.

midspan (Address 15h): Midspan Backoff Enable Register.

This is a Read/Write register; that enables the midspan back-off timer. When these bits are set, the port will wait the back-off time of 2.5s (typ.) between port detection cycles.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	-	-	mid4	mid3	mid2	mid1

Bits	Symbol	Description
0	mid1	Enable midspan back-off on port 1
1	mid2	Enable midspan back-off on port 2
2	mid3	Enable midspan back-off on port 3
3	mid4	Enable midspan back-off on port 4
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved

tcr (Address 16h): Timing Configuration Register.

This is a Read/Write register; that changes the length of t_{START} , t_{CUT} and t_{DIS} timers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	$t_{START}[1:0]$		$t_{CUT}[1:0]$		$t_{DIS}[1:0]$	

Bits	Symbol	Description
1:0	t_{START}	Timing control for t_{START} , see Table 12
3:2	t_{CUT}	Timing control for t_{CUT} , see Table 12
5:4	t_{DIS}	Timing control for t_{DIS} , see Table 12
6	-	Reserved
7	-	Reserved

[1:0]		t_{START} (typ.)	t_{CUT} (typ.)	t_{DIS} (typ.)
[1]	[0]			
0	0	60ms	60ms	360ms
0	1	30ms	30ms	90ms
1	0	120ms	120ms	180ms
1	1	240ms	240ms	720ms

Table 12: Timing Controls

conf (Address 16h): General Configuration Register.

This is a Read/Write register; that changes the length of t_{START} , t_{CUT} and t_{DIS} timers.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
inten	detchg	-	-	-	-	-	-

Bits	Symbol	Description
0	-	Reserved
1	-	Reserved
2	-	Reserved
3	-	Reserved
4	-	Reserved
5	-	Reserved
6	detchg	Detect Change. When this bit is set, detect events are only generated when the result differs from the previous detected result. When the bit is cleared, a port bit in the “det” register (04h) is set every time the Ag6400 performs detection on that port.
7	inten	Interrupt Pin Enable. When the bit is cleared the /INT pin will be high impedance regardless of the state of the interrupt registers (00h & 01h).

7.1.5 Action Registers

There are three action registers that are used by the Ag6400:-

detar (Address 18h): Detect and Classification Enable Register.

This is a Set Only register; that is used to set the corresponding bit in the “dcenr” register (14h). The four lower bits affect the signature on each port and the four upper bits affect the classification.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
cls4	cls3	cls2	cls1	det4	det3	det2	det1

Bits	Symbol	Description
0	det1	Sets bit 0 (dep1) in the “dcenr” register (14h)
1	det2	Sets bit 1 (dep2) in the “dcenr” register (14h)
2	det3	Sets bit 2 (dep3) in the “dcenr” register (14h)
3	det4	Sets bit 3 (dep4) in the “dcenr” register (14h)
4	cls1	Sets bit 4 (cep1) in the “dcenr” register (14h)
5	cls2	Sets bit 5 (cep2) in the “dcenr” register (14h)
6	cls3	Sets bit 6 (cep3) in the “dcenr” register (14h)
7	cls4	Sets bit 7 (cep4) in the “dcenr” register (14h)

pwr (Address 19h): Power Enable Register.

This is a Set Only register; that is used to force the ports to power on or off, regardless of the status of the port.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
off4	off3	off2	off1	on4	on3	on2	on1

Bits	Symbol	Description
0	on1	Turn port 1 power on
1	on2	Turn port 2 power on
2	on3	Turn port 3 power on
3	on4	Turn port 4 power on
4	off1	Turn port 1 power off*
5	off2	Turn port 2 power off*
6	off3	Turn port 3 power off*
7	off4	Turn port 4 power off*

*Note: Setting this bit also clears the related detect and fault bits, the port status register and the detect and classification enable bits.

reset (Address 1Ah): Reset Register.

This is a Set Only register; that is used to clear all events and to reset the Ag6400 or individual ports.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
allclr	intclr	-	allrst	rst4	rst3	rst2	rst1

Bits	Symbol	Description
0	rst1	Reset port 1*
1	rst2	Reset port 2*
2	rst3	Reset port 3*
3	rst4	Reset port 4*
4	allrst	Reset the Ag6400*
5	-	Reserved
6	-	Reserved
7	allclr	Clear all event registers (02h to 0Bh)

*Note: When set, the following port bits are also cleared: Power Enable bits is the Power Status “pwsr” register (10h), the detect and fault event bits, the port status register and the detect and classification enable bits.

7.1.6 Timing Limit Registers

There are two timing limit registers that are used by the Ag6400:-

tlim12 (Address 1Eh): Port 1 & 2 Timing limitation Register.

This is a Read/Write register; used to set timer duration for ports 1 & 2. The port’s t_{LIM} timer counts up when the port is in current limit and resets when the port is not in current limit. If the timer expires then the port turns off and the t_{LIM} bit in the “tsr” register (08h) is set.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$t_{LIM2}[3:0]$				$t_{LIM1}[3:0]$			

Bits	Symbol	Description
3:0	t_{LIM1}	Timer duration of port 1 = 1.71ms (typ.) times the value of this field
7:4	t_{LIM2}	Timer duration of port 2 = 1.71ms (typ.) times the value of this field

tlim12 (Address 1Fh): Port 3 & 4 Timing limitation Register.

This is a Read/Write register; used to set timer duration for ports 3 & 4. The port's t_{LIM} timer counts up when the port is in current limit and resets when the port is not in current limit. If the timer expires then the port turns off and the t_{LIM} bit in the "tsr" register (08h) is set.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$t_{LIM4}[3:0]$				$t_{LIM3}[3:0]$			

Bits	Symbol	Description
3:0	t_{LIM3}	Timer duration of port 3 = 1.71ms (typ.) times the value of this field
7:4	t_{LIM4}	Timer duration of port 4 = 1.71ms (typ.) times the value of this field

7.1.7 Measurement Registers

There are sixteen measurement registers in the Ag6400:-

ip1lsb(Address 30h): Port 1 Current Measurement LSB Register.

This is a Read Only register; used to measure port 1 current.

Bits	Symbol	Description
7:0	ip1lsb	Port 1 Current LSB. LSB = 122.07 μ A

ip1msb(Address 31h): Port 1 Current Measurement MSB Register.

This is a Read Only register; used to measure port 1 current.

Bits	Symbol	Description
7:0	ip1msb	Port 1 Current MSB.

vp1lsb(Address 32h): Port 1 Voltage Measurement LSB Register.

This is a Read Only register; used to measure port 1 voltage.

Bits	Symbol	Description
7:0	vp1lsb	Port 1 Voltage LSB. LSB = 5.835mV

vp1msb(Address 33h): Port 1 Voltage Measurement MSB Register.

This is a Read Only register; used to measure port 1 voltage.

Bits	Symbol	Description
7:0	vp1msb	Port 1 Voltage MSB.

The following registers can be used to measure ports 2, 3 and 4; they follow the same format as shown for port 1.

ip2lsb(Address 34h): Port 2 Current Measurement LSB Register.

ip2msb(Address 35h): Port 2 Current Measurement MSB Register.

vp2lsb(Address 36h): Port 2 Voltage Measurement LSB Register.

vp2msb(Address 37h): Port 2 Voltage Measurement MSB Register.

ip3lsb(Address 38h): Port 3 Current Measurement LSB Register.

ip3msb(Address 39h): Port 3 Current Measurement MSB Register.

vp3lsb(Address 3Ah): Port 3 Voltage Measurement LSB Register.

vp3msb(Address 3Bh): Port 3 Voltage Measurement MSB Register.

ip4lsb(Address 3Ch): Port 4 Current Measurement LSB Register.

ip4msb(Address 3Dh): Port 4 Current Measurement MSB Register.

vp4lsb(Address 3Eh): Port 4 Voltage Measurement LSB Register.

vp4msb(Address 3Fh): Port 4 Voltage Measurement MSB Register.

7.1.8 Power Management Registers

There are seventeen Power Management Registers in the Ag6400:-

pen(Address 44h): Power Measurement Enable Register.

This is a Read/Write register; that enables the power registers (46h to 58h). The pen_N bits are automatically set in Hardware mode, but must be set in Software mode.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	-	-	pen4	pen3	pen2	pen1

Bits	Symbol	Description
0	pen1	Enables port 1 power registers (46h to 49h)
1	pen2	Enables port 2 power registers (4Bh to 4Eh)
2	pen3	Enables port 3 power registers (50h to 53h)
3	pen4	Enables port 4 power registers (55h to 58h)
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved

pm1 (Address 46h): Port 1 Power Mode Register.

This is a Read/Write register; that enables the power registers (46h to 58h). The pen_N bits are automatically set in Hardware mode, but must be set in Software mode.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	-	-	-	-	legen1	cl4en1

Bits	Symbol	Description
0	cl4en1	Enables the 2 event classification (class 4) on port 1
1	legen1	Enables detection of legacy PDs by sensing for large capacitance on port 1. When this bit is set a PD with a large common mode capacitance will be reported as a valid signature. This sets the detect[2:0] bits in the "psr1" register (0Ch) to "100" - Good (see Table 9).
2	-	Reserved
3	-	Reserved
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved

i_{CUT}1 (Address 47h): Port 1 Over-Current Cut-Off Register.

This is a Read/Write register; that sets the i_{CUT} limit for port 1. In Hardware mode the rdis bit is automatically set, but must be set in Software mode.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
rdis	cutdbl	i _{CUT} [5:0]					

Bits	Symbol	Description
0:5	i _{CUT}	When the cutdbl bit is set the LSB = 18.75mA (max = 1181mA) When the cutdbl bit is cleared the LSB = 37.5mA (max = 2363mA)
6	cutdbl	When this bit is cleared the i _{CUT} current is doubled
7	rdis	DC disconnect threshold, this bit MUST be set

i_{LIM}1(Address 48h): Port 1 Current Limit Register.

This is a Read/Write register; that sets the i_{LIM} limit for port 1.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
i _{LIM} [7:0]							

Bits	Symbol	Description
7:0	i _{LIM}	Port 1 current limit, see Table 7

pstat1 (Address 49h): Port 1 Class 4 Confirmation Register.

This is a Read/Write register; that enables the power registers (46h to 58h). The pen_N bits are automatically set in Hardware mode, but must be set in Software mode.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	-	-	-	-	-	cl4det1

Bits	Symbol	Description
0	cl4det1	Enable 2 event classification (Class 4) detection on port 1
1	-	Reserved
2	-	Reserved
3	-	Reserved
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved

The following registers are used to set ports 2, 3 and 4; they follow the same format as shown for port 1.

pm2 (Address 4Bh): Port 2 Power Mode Register.
i_{CUT}2 (Address 4Ch): Port 2 Over-Current Cut-Off Register.
i_{LIM}2(Address 4Dh): Port 2 Current Limit Register.
pstat2 (Address 4Eh): Port 2 Class 4 Confirmation Register.

pm3 (Address 50h): Port 3 Power Mode Register.
i_{CUT}3 (Address 51h): Port 3 Over-Current Cut-Off Register.
i_{LIM}3(Address 52h): Port 3 Current Limit Register.
pstat3 (Address 53h): Port 3 Class 4 Confirmation Register.

pm4 (Address 55h): Port 4 Power Mode Register.
i_{CUT}4 (Address 56h): Port 4 Over-Current Cut-Off Register.
i_{LIM}4(Address 57h): Port 4 Current Limit Register.
pstat4 (Address 58h): Port 4 Class 4 Confirmation Register.

7.2 System Software

This section describes a basic software control flows for a typical application. In the following examples, the Ag6400 MODE input is set to Logic 0, configuring the module in Software mode. The controller is connected to the Ag6400 as shown in Figure 8 and communicates via the I²C bus.

7.2.1 Initialisation

The Ag6400 initialisation sequence can be broken down into the steps shown in Table 15.

Step No.	Register Address	Register Name	Data Hex	Data Binary	Instruction
1	1Ah	reset	10	0001 0000	Reset the Ag6400
2	01h	intmask	F4	1111 0100	Configure the interrupt mask
3	1Ah	reset	80	1000 0000	Clear all interurupts
4	13h	disenr	0F	0000 1111	Enable DC disconnect sensing on all ports
5	44h	pen	0F	0000 1111	Enable power register
6	47h	i _{CUT} 1	D4	1101 0100	Set the ports cutoff current = 375mA for the detection cycle
7	4Ch	i _{CUT} 2			
8	51h	i _{CUT} 3			
9	56h	i _{CUT} 4			
10	48h	i _{LIM} 1	C0	1100 0000	Set the ports current limit = 850mA for the detection cycle (see Table 7)
11	4Dh	i _{LIM} 2			
12	52h	i _{LIM} 3			
13	57h	i _{LIM} 4			
14	46h	pm1	01	0000 0001	Enable the 2 event (Class 4) detection
15	4Bh	pm2			
16	50h	pm3			
17	55h	pm4			
18	12h	omr	AA	1010 1010	Set the Ag6400 to Software mode
19	14h	dcenr	FF	1111 1111	Enable signature detection and classification

Table 15: Initialisation Sequence

7.2.2 Detection – Signature and Classification

After the Ag6400 has been initialised, the module will recycle looking for a PD to be connected to one of the ports.

Table 16 shows the step required to check the port status and how to respond when a PD is detected.

Step No.	Register Address	Register Name	Data Hex	Data Binary	Instruction
1	00h	int	read	read	Read the interrupt register and continue if the class bit is set.
2	05h	det_cor	read	read	Read and clear this register to determine which port has flagged the interrupt
3	0Ch	psr1	read	read	Read the class results from the port that flagged the interrupt
	0Dh	psr2			
	0Eh	psr3			
	0Fh	psr4			
4	47h	i _{CUT} 1	xx	xxxx xxxx	Set the port cut-off current corresponding to the class result (on the port that flagged the interrupt), see Table 2
	4Ch	i _{CUT} 2			
	51h	i _{CUT} 3			
	56h	i _{CUT} 4			
5	48h	i _{LIM} 1	xx	xxxx xxxx	Set the port current limit corresponding to the class result (on the port that flagged the interrupt), see Table 2
	4Dh	i _{LIM} 2			
	52h	i _{LIM} 3			
	57h	i _{LIM} 4			
6	19h	pwr	xx	0000 xxxx	Turn on the appropriate port in the Power Enable register

Table 16: PD Detection Sequence

7.2.3 PD Disconnected

If a PD is disconnected from a power the Ag6400 will detect this and remove the power. All that is required is some basic maintenance, to clear interrupts and record which port has been disconnected (e.g. if the ports are being measured for power management).

Table 17 shows the step required to clear a port if the PD have been disconnected.

Step No.	Register Address	Register Name	Data Hex	Data Binary	Instruction
1	03h	per_cor	read	read	Read and clear the Power Event register
2	07h	fer_cor	read	read	Read and clear the Fault Event register

Table 17: PD Disconnected

8. Protection

The Ag6400 has built-in Tranzorb diodes on the V_{EE} supply and all four output ports.

9. Electrical Characteristics

9.1 Absolute Maximum Ratings¹

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{EE}	0.3	-80	V
		V_{DD}	-0.3	5.5	V
2	Inputs	V_{INPUTS}	-0.3	$V_{DD} + 0.3$	V
3	Storage Temperature	T_S	-40	+100	°C

Note 1: Exceeding the above ratings may cause permanent damage to the product. Functional operation under these conditions is not implied. Maximum ratings assume free airflow.

9.2 Recommended Operating Conditions

	Parameter	Symbol	Min	Typ	Max	Units
1	Input Supply Voltage	$V_{EE (Type1)}$	-45		-57	V
		$V_{EE (Type2)}$	-50		-57	V
		V_{DD}	3.0	3.3	3.6	V
2	Under Voltage Lockout	UVLO	20	25	30	V
3	Operating Temperature	T_{OP}	-40	25	+85	$T_a / ^\circ C$

9.3 Electrical Characteristics

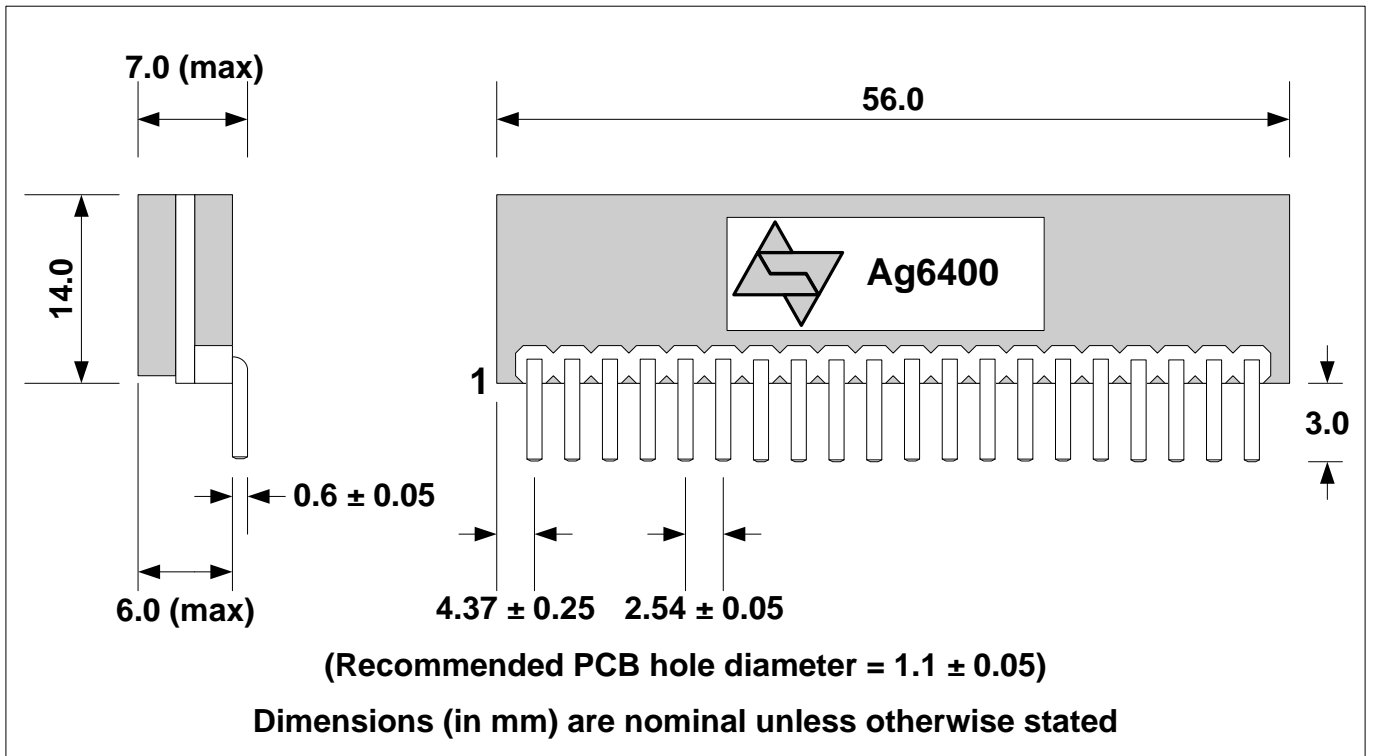
	Parameter	Sym	Min	Typ	Max	Units	Condition
1	Idle V_{EE} Supply Current	I_{EE}		-2.4	-5	mA	No Output Port Connected
2	Idle V_{DD} Supply Current	I_{DD}		1.1	3	mA	No Output Port Connected
Signature							
3	Detection Current – Force Current	I_{SIG1}	220	240	260	μ A	$V_{OUTn} = 9V$ $V_{OUTn} = 3.5V$
		I_{SIG2}	140	160	180	μ A	
4	Detection Voltage – Force Voltage	V_{SIG1}	7	8	9	V	
		V_{SIG2}	3	4	5	V	
5	Minimum Valid Signature	R_{SIG1}	15.5	17	18.5	k Ω	
6	Maximum Valid Signature	R_{SIG2}	27.5	29	32	k Ω	
Classification							
7	Classification Voltage	V_{CLASS}	16		20.5	V	
8	Classification Threshold Current	I_{CLASS}	5.5	6.5	7.5	mA	Class 0 – 1 Class 1 – 2 Class 2 – 3 Class 3 – 4 Class 4 – Overcurrent
			13.5	14.5	15.5	mA	
			21.5	23	24.5	mA	
			31.5	33	34.9	mA	
			45.2	48	50.8	mA	
9	Classification Mark Voltage	V_{MARK}	7.5	9	10	V	
Digital Inputs							
10	Digital Input Logic 0	V_{IL}			0.8	V	
11	Digital Input Logic 1	V_{IH}	2.2			V	
12	Input Pull-Up Resistance	R_{PU}		50		k Ω	ADn
Digital Outputs							
13	Digital Output Logic 0	V_{OL}			0.4	V	@ 3mA
					0.7	V	@ 5mA
14	Output Pull-Down Resistance	R_{PD}		50		k Ω	MODE and MID

9.4 Timing Characteristics

	Parameter	Sym	Min	Typ	Max	Units	Condition
General							
1	Detection Time	t_{DET}	270	290	310	mS	
2	Detection Delay	t_{DETDLY}	300		470	mS	
3	1 st Class Event Duration	t_{CLE1}	11	12	13	mS	
4	1 st Mark Event Duration	t_{ME1}	6.8	8.6	10.3	mS	
5	2 nd Class Event Duration	t_{CLE2}	11	12	13	mS	
6	2 nd Mark Event Duration	t_{ME2}	19	22		mS	
7	3 rd Class Event Duration	t_{CLE3}			0.1	mS	
8	Power On Delay in Software Mode	t_{PON}			60	mS	
9	Fault Delay (from I_{CUT} to Next Detect Cycle)		1			S	
10	Midspan Mode Detection Backoff		2.3			S	
I²C Bus¹							
11	Bus Free Time	t_1	480			nS	
12	Start Hold Time	t_2	240			nS	
13	SCL Low Time	t_3	480			nS	
14	SCL High Time	t_4	240			nS	
15	Data Hold Time	t_5	60		120	nS nS	Data In Data Out
16	Data Set-up Time	t_6	80			nS	
17	Start Set-up Time	t_7	240			nS	
18	Stop Set-up Time	t_8	240			nS	
19	Rise Time	t_r			120	nS	
20	Fall Time	t_f			60	nS	

Note 1: Values measured between V_{IL} (Max) and V_{IH} (Min)

10. Package



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