



N-channel Power MOSFET

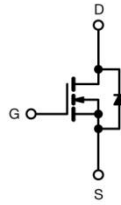
PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	700
$R_{DS(on)}$ max. at 25°C (Ω)	$V_{GS}=10V$ 1.1
Q_g max. (nC)	45
Q_{gs} (nC)	7
Q_{gd} (nC)	15
Configuration	single

Features

- $I_D=10A(V_{GS}=10V)$
- Ultra Low Gate Charge
- Improved dv/dt Capability
- 100% Avalanche Tested
- RoHS compliant



TO-220F



Schematic diagram

Applications

- Switching Mode Power Supplies (SMPS)
- PWM Motor Controls
- DC to DC Converters
- LED Lighting
- Bridge Circuits

ORDERING INFORMATION	
Device	SPC10N65G
Device Package	TO-220F
Marking	10N65G

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain to Source Voltage	V_{DSS}	650	V
Continuous Drain Current (@ $T_C=25^\circ C$)	I_D	10 ⁽¹⁾	A
Continuous Drain Current (@ $T_C=100^\circ C$)		6.0 ⁽¹⁾	A
Drain current pulsed ⁽²⁾	I_{DM}	40 ⁽¹⁾	A
Gate to Source Voltage	V_{GS}	± 30	V
Single pulsed Avalanche Energy ⁽³⁾	E_{AS}	400	mJ
Peak diode Recovery dv/dt ⁽⁴⁾	dv/dt	6	V/ns
Total power dissipation (@ $T_C=25^\circ C$)	P_D	40	W
Derating Factor above 25°C		0.32	W/°C
Operating Junction Temperature & Storage Temperature	T_{STG}, T_J	-55 to + 150	°C
Maximum lead temperature for soldering purpose	T_L	260	°C
Mounting torque ⁽⁵⁾		0.4~0.6	N.m

Notes

1. Drain current is limited by maximum junction temperature.
2. Repetitive rating : pulse width limited by junction temperature.
3. $L = 8mH, I_{AS} = 10A, V_{DD} = 50V, R_G=25\Omega$, Starting at $T_J = 25^\circ C$
4. $I_{SD} \leq 10A, di/dt = 100A/us, V_{DD} \leq BV_{DSS}$, Starting at $T_J = 25^\circ C$
5. Mounting consideration for TO220 Fullpack:

M3 screw plus flat washer is suggested, free of burr between devices and contact area, the devices are to be mounted to a hole not larger than 3.6mm in contact diameter (chamfer included).



THERMAL CHARACTERISTICS			
Parameter	Symbol	Value	Unit
Thermal resistance, Junction to case	R_{thjc}	3.1	°C/W
Thermal resistance, Junction to ambient	R_{thja}	48	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise specified)						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain to source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	650	--	--	V
Breakdown voltage temperature coefficient	$\Delta BV_{DSS} / \Delta T_J$	$I_D=250\mu A$, referenced to $25^{\circ}C$	--	0.51	--	V/°C
Drain to source leakage current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$	--	--	1	μA
		$V_{DS}=520V, T_C=125^{\circ}C$	--	--	50	μA
Gate to source leakage current, forward	I_{GSS}	$V_{GS}=30V, V_{DS}=0V$	--	--	100	nA
Gate to source leakage current, reverse		$V_{GS}=-30V, V_{DS}=0V$	--	--	-100	nA
On Characteristics						
Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	--	4	V
Drain to source on state resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5A$	--	0.85	1.1	Ω
Forward Transconductance	G_{fs}	$V_{DS}=30V, I_D=5A$	--	7	--	S
Dynamic Characteristics						
Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V, f=1MHz$	--	1200	--	pF
Output capacitance	C_{oss}		--	125	--	
Reverse transfer capacitance	C_{riss}		--	21	--	
Turn on delay time	$t_{d(on)}$	$V_{DS}=380V, I_D=10A, R_G=25\Omega$	--	15	--	ns
Rising time	t_r		--	45	--	
Turn off delay time	$t_{d(off)}$		--	90	--	
Fall time	t_f		--	30	--	
Total gate charge	Q_g	$V_{DS}=520V, V_{GS}=10V, I_D=10A$	--	38	--	nC
Gate-source charge	Q_{gs}		--	7	--	
Gate-drain charge	Q_{gd}		--	15	--	

SOURCE TO DRAIN DIODE RATINGS CHARACTERISTICS						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous source current	I_S	Integral reverse p-n Junction diode in the MOSFET	--	--	10	A
Pulsed source current	I_{SM}		--	--	40	A
Diode forward voltage drop.	V_{SD}	$I_S=10A, V_{GS}=0V$	--	--	1.2	V
Reverse recovery time	T_{rr}	$I_S=10A, V_{GS}=0V, di_f/dt=100A/\mu s$	--	502	--	ns
Reverse recovery Charge	Q_{rr}		--	13	--	μC



Fig1. Output characteristics

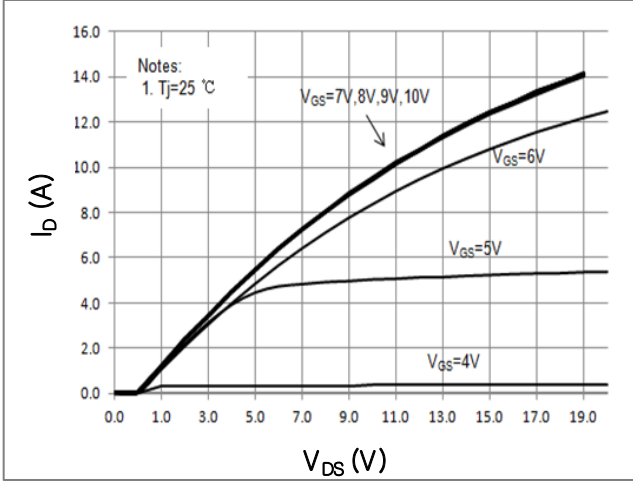


Fig2. Drain-source on-state resistance

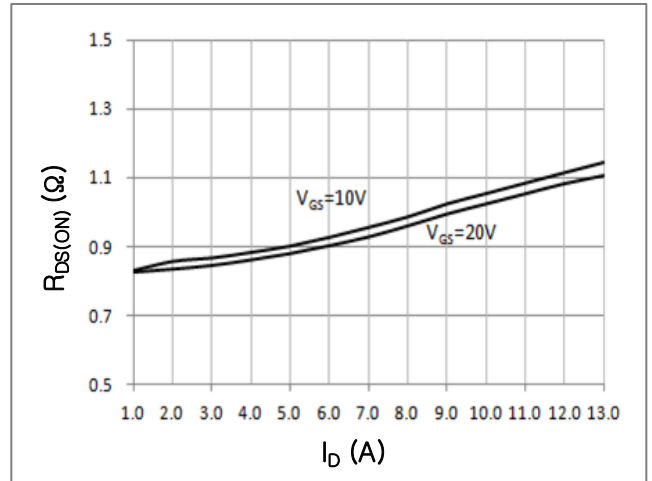


Fig3. Gate charge characteristics

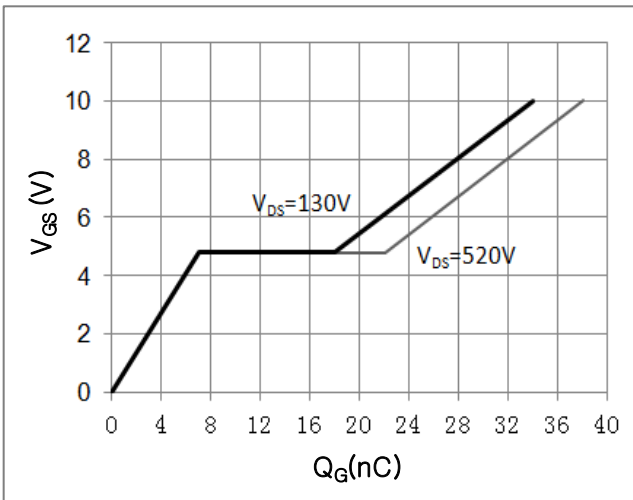


Fig 4. Capacitance Characteristics

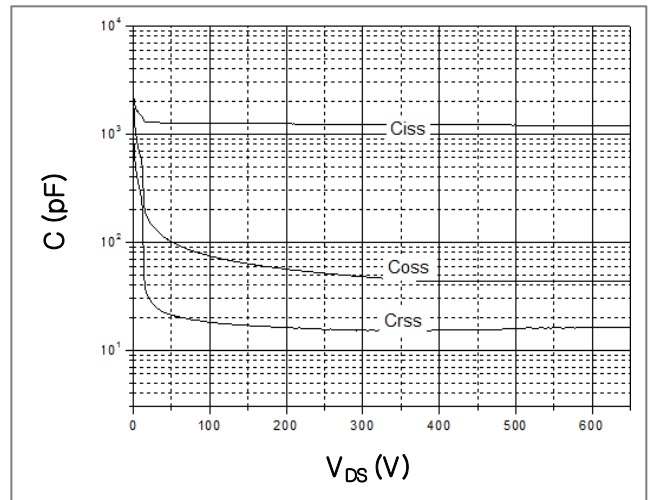


Fig 5. $R_{DS(ON)}$ vs junction temperature

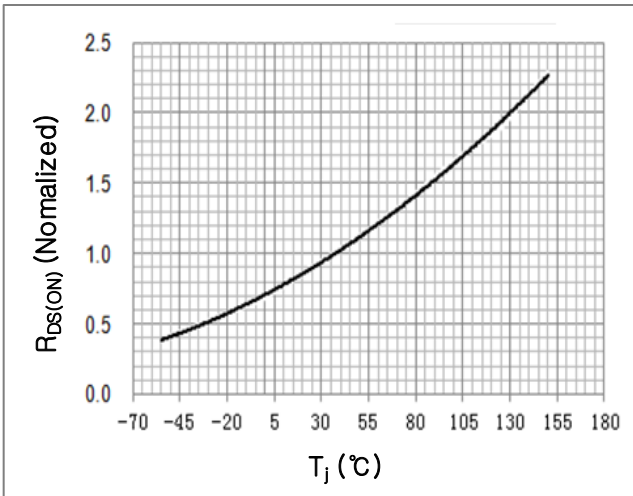


Fig 6. BV_{DSS} vs junction temperature

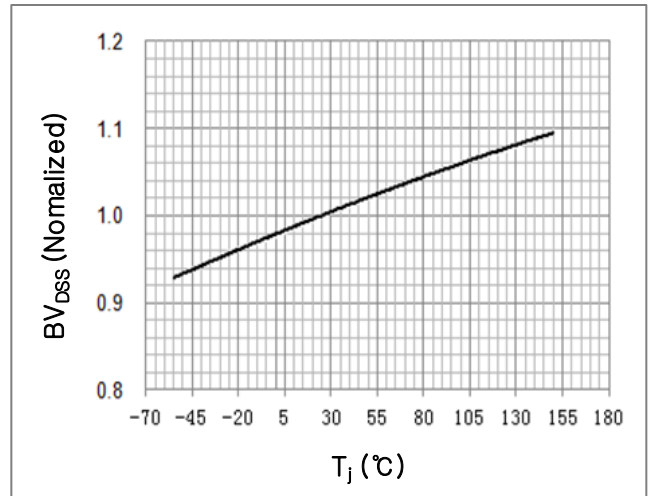


Fig 7 . Safe operating area

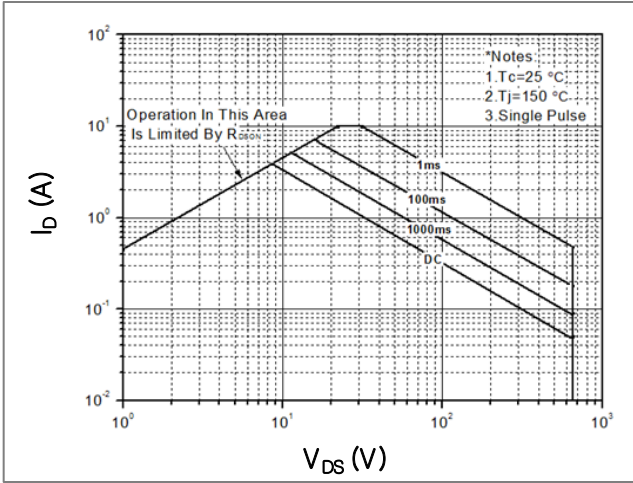


Fig 8 . Transient thermal impedance

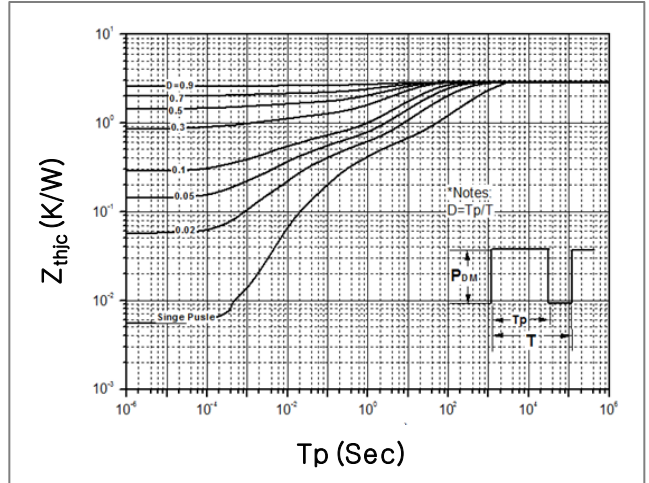


Fig 9. Forward characteristics of reverse diode

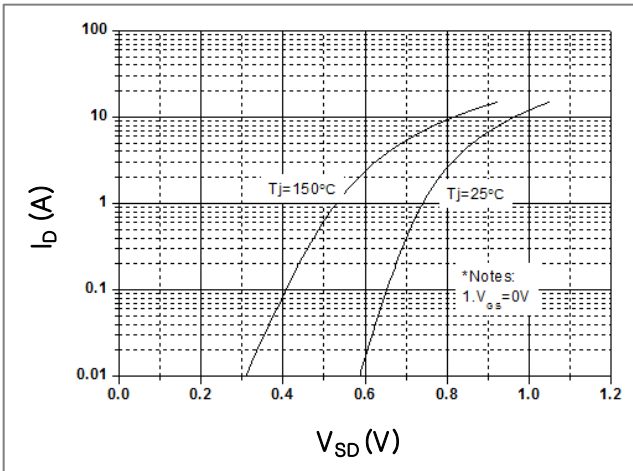


Fig 10. Gate charge test circuit & waveform

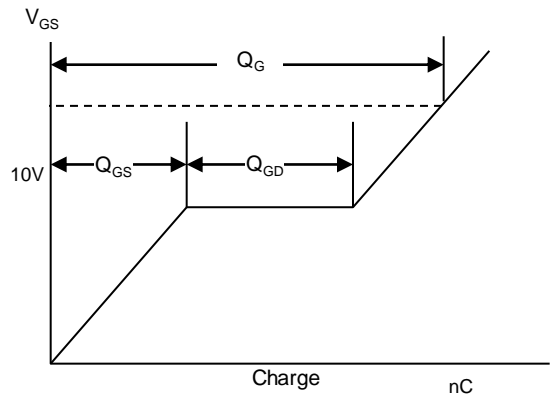
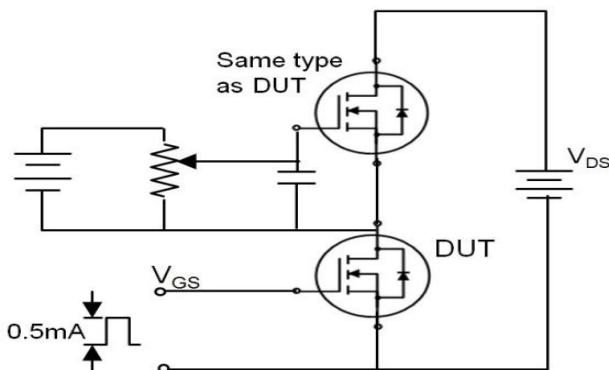


Fig 11. Switching time test circuit & waveform

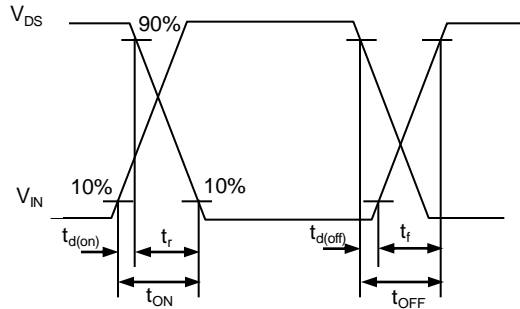
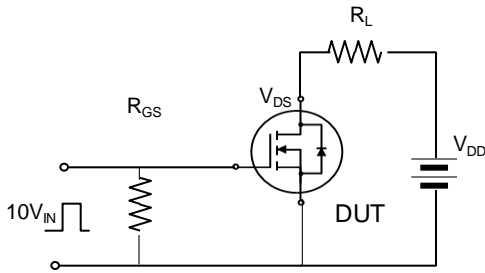


Fig 12. Unclamped Inductive switching test circuit & waveform

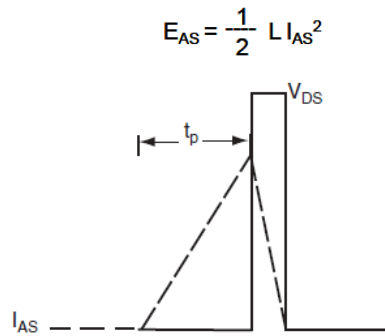
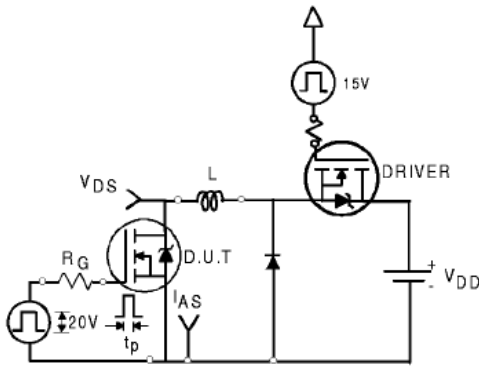
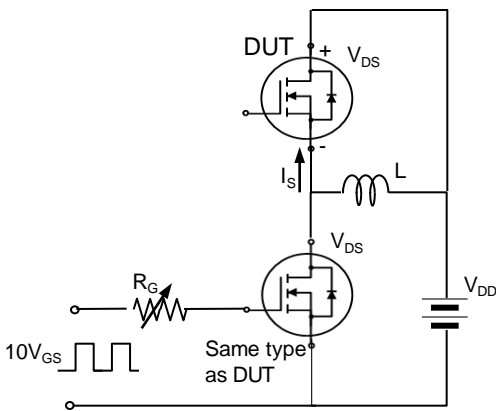
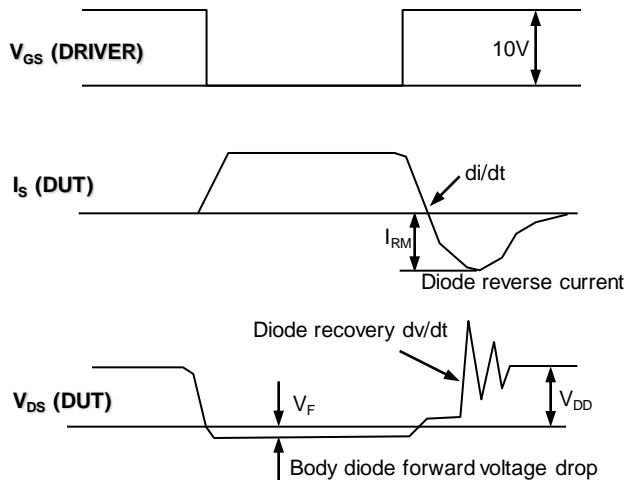


Fig 13. Peak diode recovery dv/dt test circuit & waveform



*. dv/dt controlled by RG
*. IS controlled by pulse period





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