



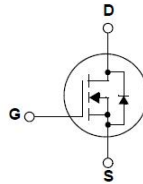
N-channel Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ typ. at 25 °C (Ω)	$V_{GS}=10V$	0.64
Q_g max. (nC)	31.5	
Q_{gs} (nC)	12	
Q_{gd} (nC)	6.5	
Configuration	single	

Features

- I_D 9 A ($V_{GS}=10V$)
- Ultra Low Gate Charge
- Improved dv/dt Capability
- 100% Avalanche Tested
- ROHS compliant



Applications

- Switching Mode Power Supplies (SMPS)
- Power Factor Correction (PFC)
- Uninterruptible Power Supply (UPS)
- LED Lighting
- Notebook and Desktop

ORDERING INFORMATION

Device	SPC9N50G
Device Package	TO-220F
Marking	9N50G

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limit			Unit
		SPC9N50G			
Drain to Source Voltage	V_{DSS}	500			V
Continuous Drain Current (@ $T_C=25^\circ\text{C}$)	I_D	9			A
Continuous Drain Current (@ $T_C=100^\circ\text{C}$)		4.5			A
Drain current pulsed (note 1)	I_{DM}	32			A
Gate to Source Voltage	V_{GS}	30			V
Single pulsed Avalanche Energy (note 2)	E_{AS}	285			mJ
Peak diode Recovery dv/dt (note 3)	dv/dt	4.5			V/ns
Total power dissipation (@ $T_C=25^\circ\text{C}$)	P_D	36	122	122	
Derating Factor above 25°C		0.28	1.33	1.28	
Operating Junction Temperature & Storage Temperature	T_{STG}, T_J	-55 to + 150			°C
Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	T_L	300			°C

Notes

1. Repetitive rating : pulse width limited by junction temperature.
2. $L = 15\text{mH}$, $I_{AS} = 8\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 8\text{A}$, $di/dt = 100\text{A/us}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$



THERMAL CHARACTERISTICS			
Parameter	Symbol	Value	Unit
		SPC9N50G	
Thermal resistance, Junction to case	R_{thjc}	3.52	°C/W
Thermal resistance, Junction to ambient	R_{thja}	62.5	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain to source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	500			V
Breakdown voltage temperature coefficient	$\Delta BV_{DSS} / \Delta T_J$	$I_D=250\mu A$, referenced to 25°C		0.51		V/°C
Drain to source leakage current	I_{DSS}	$V_{DS}=500V, V_{GS}=0V$			1	μA
		$V_{DS}=400V, T_C=125^\circ\text{C}$			50	μA
Gate to source leakage current, forward	I_{GSS}	$V_{GS}=25V, V_{DS}=0V$			100	nA
Gate to source leakage current, reverse		$V_{GS}=-25V, V_{DS}=0V$			-100	nA
On Characteristics						
Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
Drain to source on state resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=4.0A$		0.64	0.77	Ω
Forward Transconductance	G_{fs}	$V_{DS}=30V, I_D=4.0A$		5.0		Ω
Dynamic Characteristics						
Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$		1271		pF
Output capacitance	C_{oss}			143		
Reverse transfer capacitance	C_{rss}			1		
Turn on delay time	$t_{d(on)}$	$V_{DS}=250V, I_D=8A, R_G=25\Omega$		27.5		ns
Rising time	t_r			25		
Turn off delay time	$t_{d(off)}$			127.5		
Fall time	t_f			35.5		
Total gate charge	Q_g	$V_{DS}=440V, V_{GS}=10V, I_D=8A$		31.5		nC
Gate-source charge	Q_{gs}			12		
Gate-drain charge	Q_{gd}			6.5		

SOURCE TO DRAIN DIODE RATINGS CHARACTERISTICS						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous source current	I_S	Integral reverse p-n Junction diode in the MOSFET			8	A
Pulsed source current	I_{SM}				32	A
Diode forward voltage drop.	V_{SD}	$I_S=8A, V_{GS}=0V$			1.4	V
Reverse recovery time	T_{rr}	$I_S=8A, V_{GS}=0V, di/dt=100A/\mu s$		567.5		ns
Reverse recovery Charge	Q_{rr}				4	



Typical Characteristics

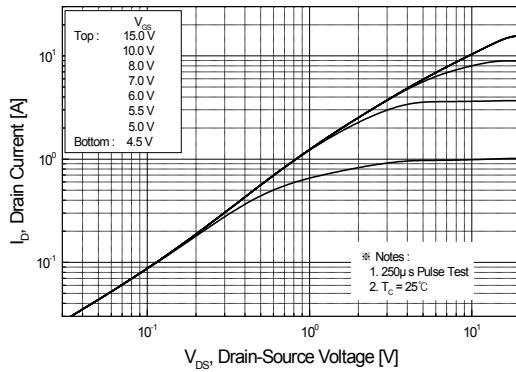


Figure 1. On-Region Characteristics

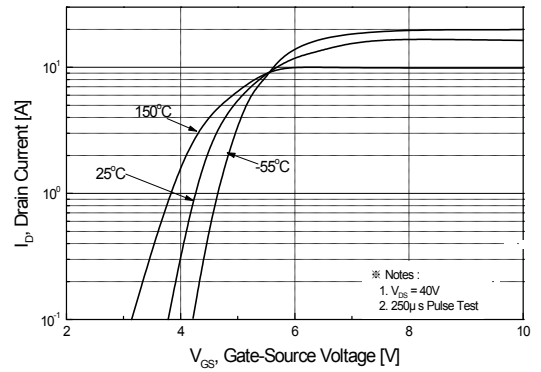


Figure 2. Transfer Characteristics

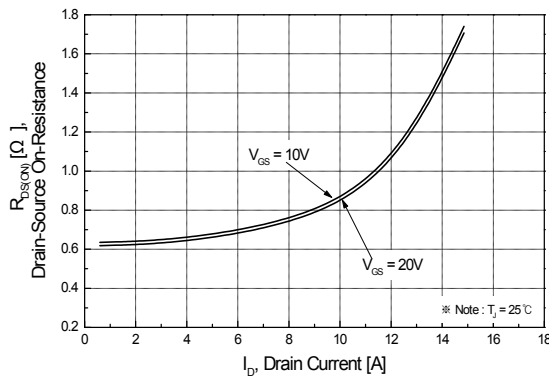


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

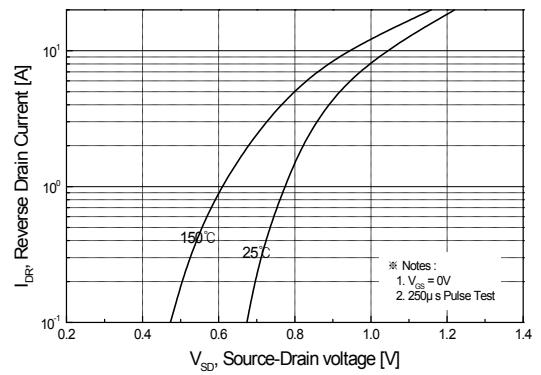


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

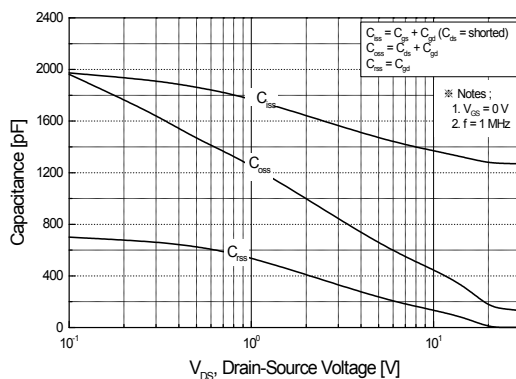


Figure 5. Capacitance Characteristics

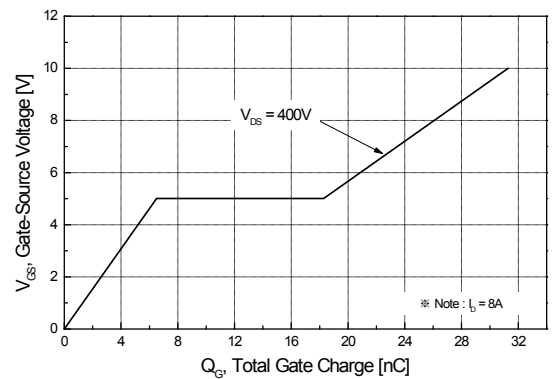


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

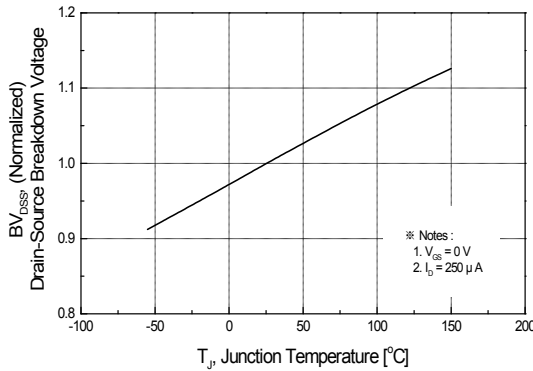


Figure 7. Breakdown Voltage Variation vs Temperature

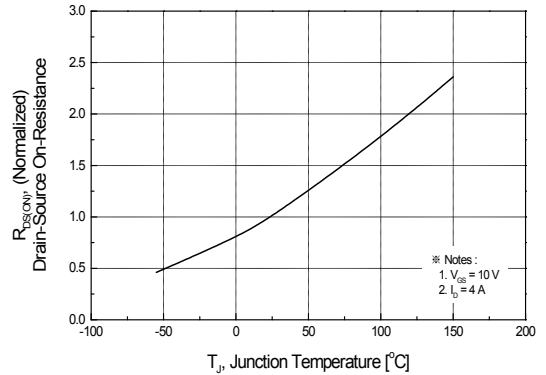


Figure 8. On-Resistance Variation vs Temperature

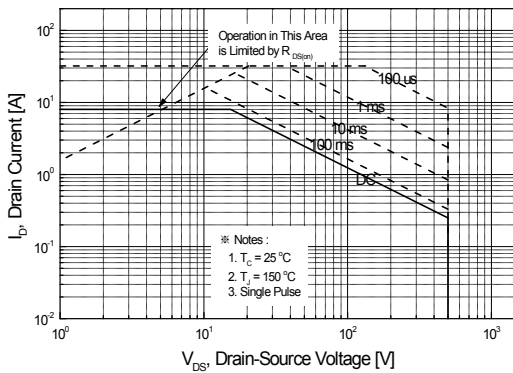


Figure 9-1. Maximum Safe Operating Area for SLP840C

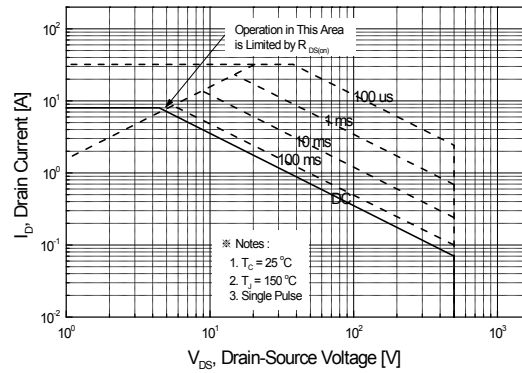


Figure 9-2. Maximum Voltage Safe Operating Area for SLF840C

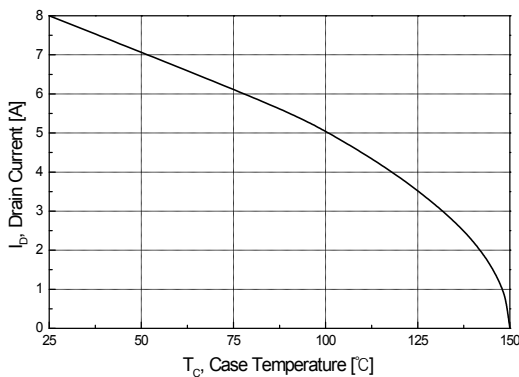


Figure 10. Maximum Drain Current vs Case Temperature

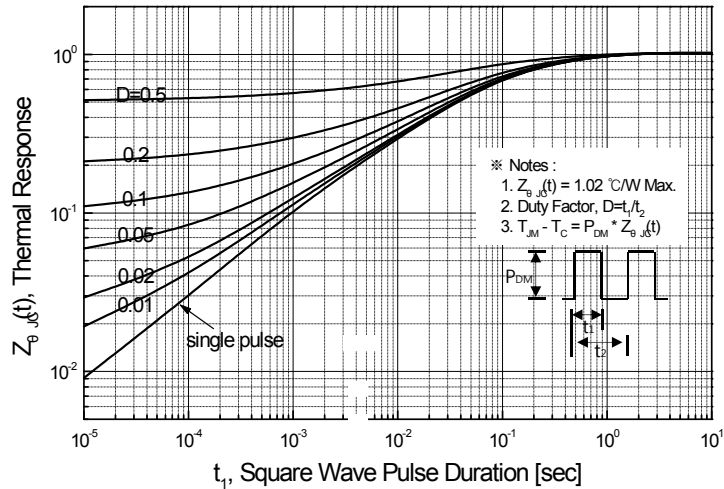


Figure 11-1. Transient Thermal Response Curve for SLP840C

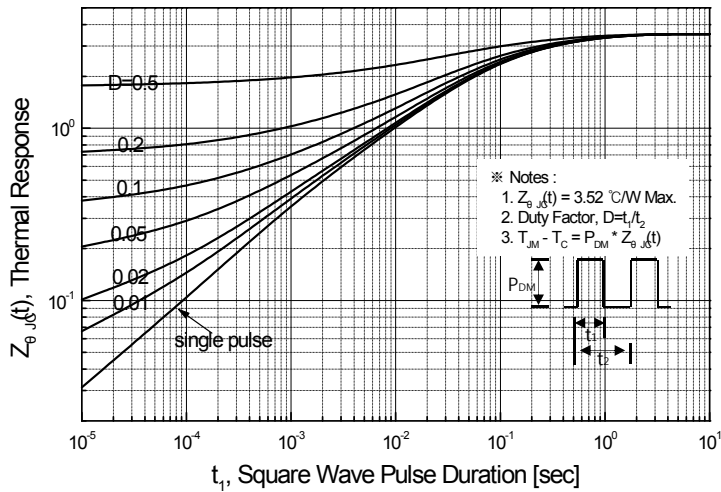


Figure 11-2. Transient Thermal Response Curve for SLF840C

Gate Charge Test Circuit & Waveform

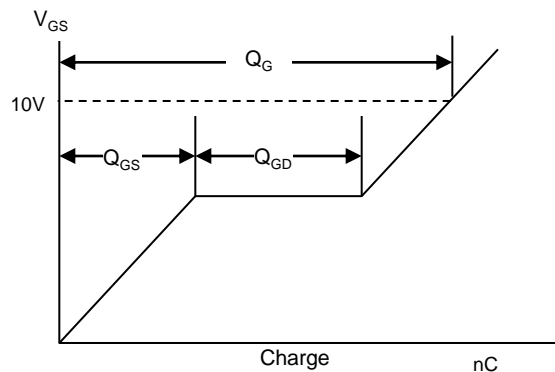
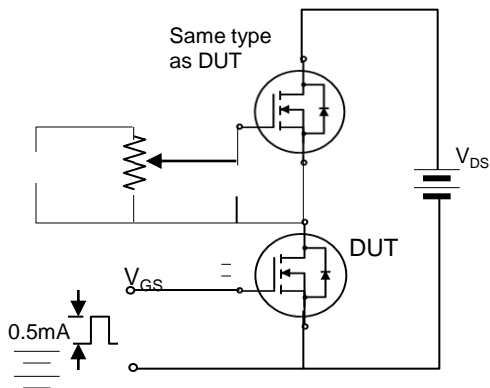


Fig 13. Switching time test circuit & waveform

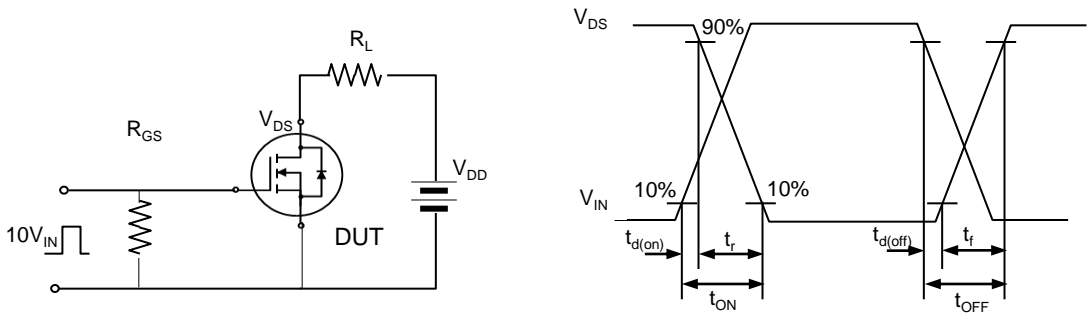


Fig 14. Unclamped Inductive switching test circuit & waveform

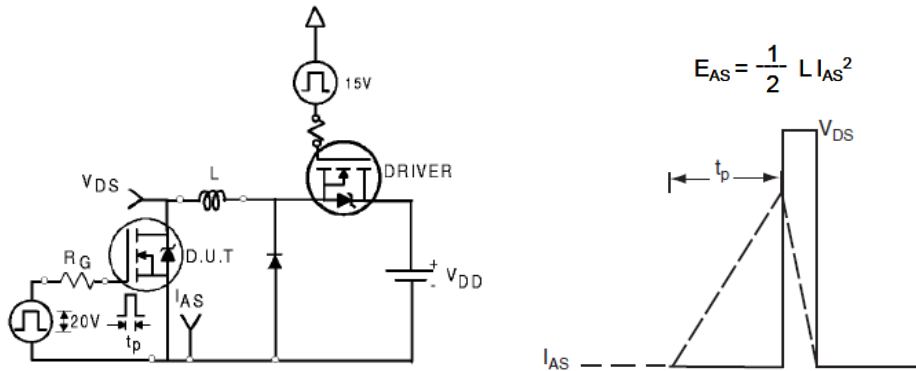
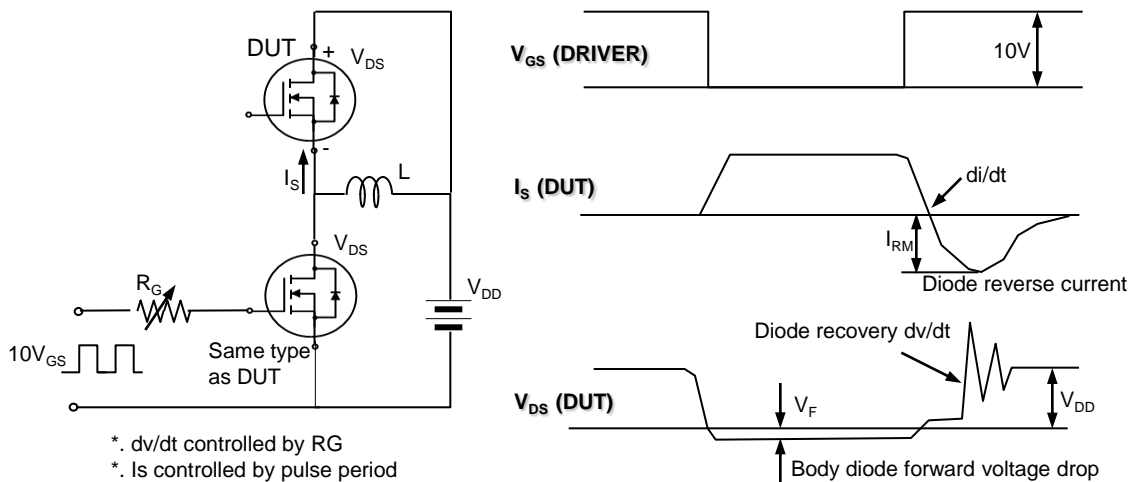


Fig 15. Peak diode recovery dv/dt test circuit & waveform





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