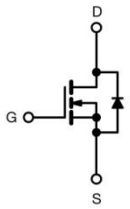
N-channel Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ max. at 25°C (Ω)	V_{GS}=10V	1.3
Q_g max. (nC)	42	
Q_{gs} (nC)	6	
Q_{gd} (nC)	12	
Configuration	single	

Features

- I_D=7A(Vgs=10V)
- Ultra Low Gate Charge
- Improved dv/dt Capability
- 100% Avalanche Tested
- RoHS compliant

TO-252



Schematic diagram

Applications

- Switching Mode Power Supplies (SMPS)
- PWM Motor Controls
- DC to DC Converters
- LED Lighting
- Bridge Circuits

ORDERING INFORMATION	
Device	SPD7N65G
Device Package	TO-252
Marking	7N65G

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain to Source Voltage	V_{DSS}	650	V
Continuous Drain Current (@T_C=25°C)	I_D	7	A
Continuous Drain Current (@T_C=100°C)		4.5	A
Drain current pulsed (2)	I_{DM}	28	A
Gate to Source Voltage	V_{GS}	30	V
Single pulsed Avalanche Energy (3)	E_{AS}	367	mJ
Peak diode Recovery dv/dt (4)	dv/dt	6	V/ns
Total power dissipation (@T_C=25°C)	P_D	160	W
Derating Factor above 25°C		1.28	W/°C
Operating Junction Temperature & Storage Temperature	T_{STG}, T_J	-55 to + 150	°C
Maximum lead temperature for soldering purpose	T_L	260	°C

Notes
1. Drain current is limited by maximum junction temperature.
2. Repetitive rating : pulse width limited by junction temperature.
3. L = 15mH, I_{AS} = 7A, V_{DD} = 50V, R_G=25Ω, Starting at T_J = 25°C
4. I_{SD} ≤ 7A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Starting at T_J =25°C

THERMAL CHARACTERISTICS			
Parameter	**Symbol**	**Value**	**Unit**
Thermal resistance, Junction to case	R_{thjc}	0.78	°C/W
Thermal resistance, Junction to ambient	R_{thja}	83	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Off Characteristics						
Drain to source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650	--	--	V
Breakdown voltage temperature coefficient	ΔBV_{DSS} / ΔTJ	I_D=250uA, referenced to 25°C	--	0.51	--	V/°C
Drain to source leakage current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		V_{DS}=520V, T_C=125°C	--	--	50	uA
Gate to source leakage current, forward	I_{GSS}	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
Gate to source leakage current, reverse		V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
On Characteristics						
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	2	--	4	V
Drain to source on state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D =3.5A	--	1.05	1.3	Ω
Forward Transconductance	Gfs	V_{DS} = 30 V, I_D = 3.5 A	--	5.2	--	S
Dynamic Characteristics						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	--	1100	--	pF
Output capacitance	C_{oss}		--	110	--	
Reverse transfer capacitance	C_{rss}		--	15	--	
Turn on delay time	$t_{d(on)}$	V_{DS}=380V, I_D=7A , R_G=25Ω	--	17	--	ns
Rising time	tr		--	33	--	
Turn off delay time	$t_{d(off)}$		--	82	--	
Fall time	t_f		--	41	--	
Total gate charge	Q_g	V_{DS}=520V, V_{GS}=10V, I_D=7A	--	37	--	nC
Gate-source charge	Q_{gs}		--	6	--	
Gate-drain charge	Q_{gd}		--	12	--	

SOURCE TO DRAIN DIODE RATINGS CHARACTERISTICS						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Continuous source current	I_S	Integral reverse p-n Junction diode in the MOSFET	--	--	7	A
Pulsed source current	I_{SM}		--	--	28	A
Diode forward voltage drop.	V_{SD}	I_S=7A, V_{GS}=0V	--	--	1.2	V
Reverse recovery time	T_{rr}	I_S=7A, V_{GS}=0V, dI_F/dt=100A/us	--	450	--	ns
Reverse recovery Charge	Qrr		--	9.1	--	uC

Fig1. Output characteristics

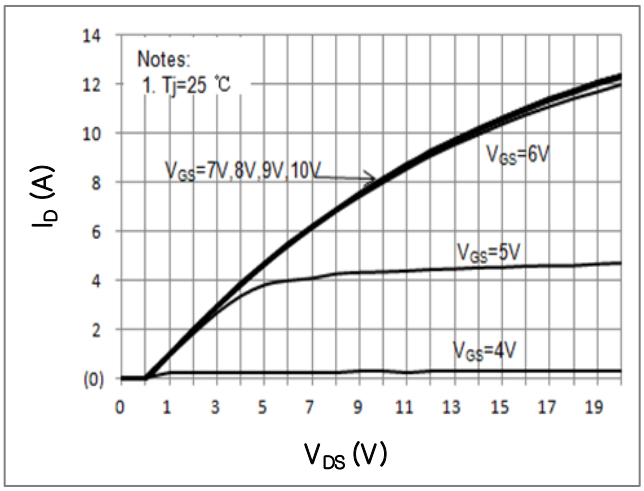


Fig2. Drain-source on-state resistance

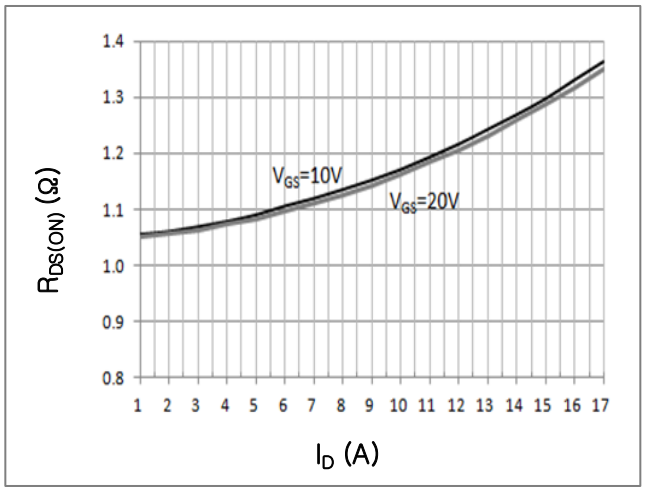


Fig3. Gate charge characteristics

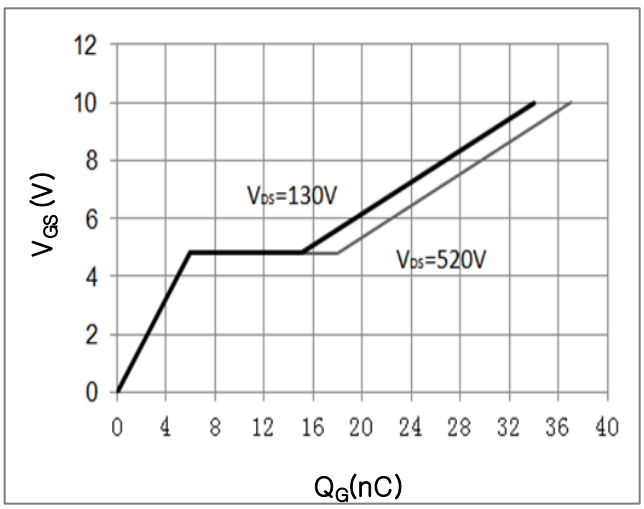


Fig 4. Capacitance Characteristics

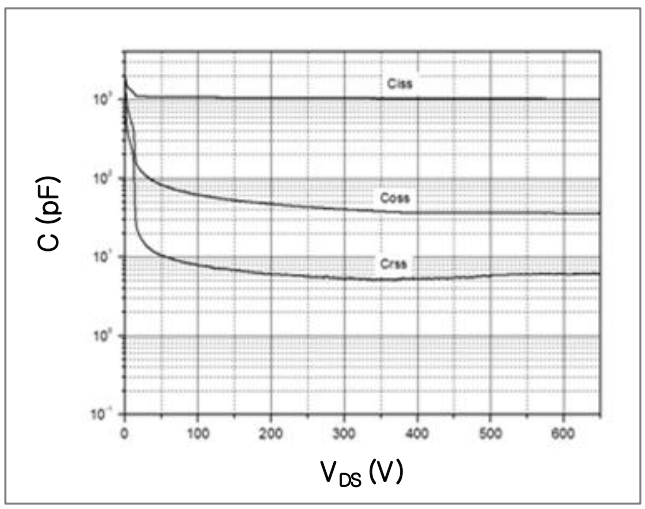


Fig 5. $R_{DS(ON)}$ vs junction temperature

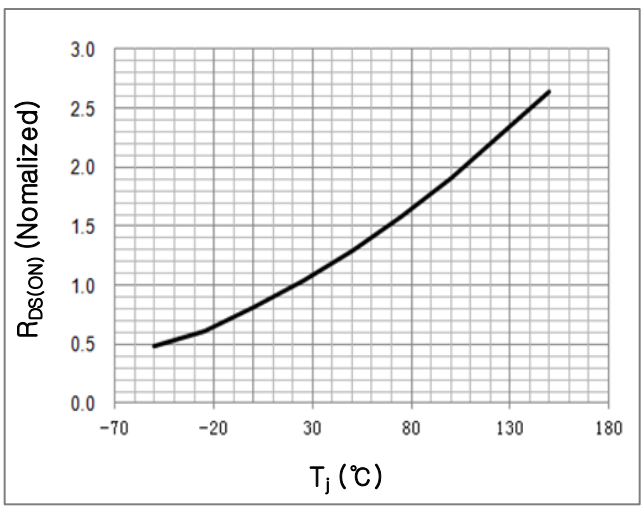


Fig 6. BV_{DSS} vs junction temperature

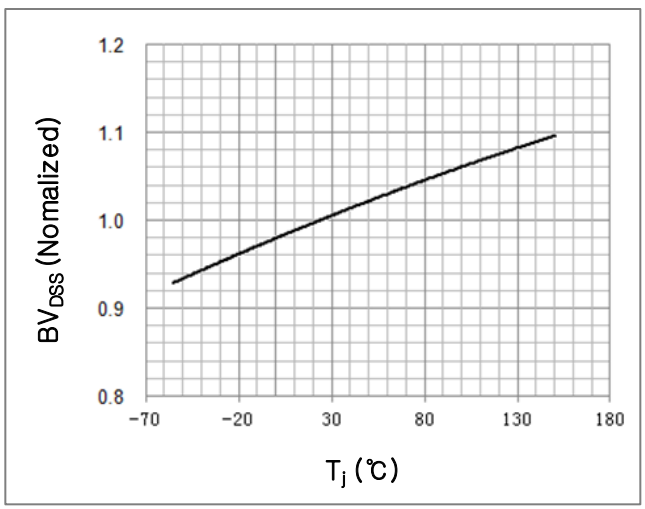


Fig 7 . Safe operating area

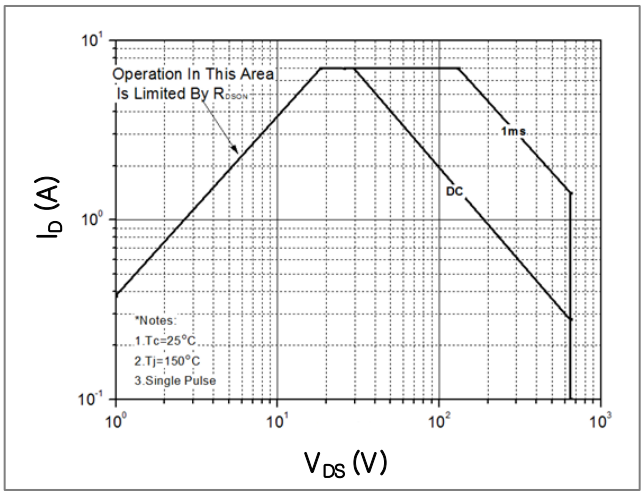


Fig 8. Transient thermal impedance

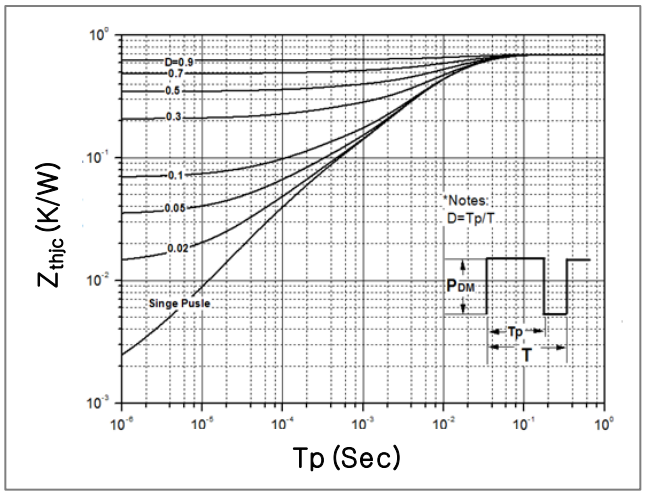


Fig 9. Forward characteristics of reverse diode

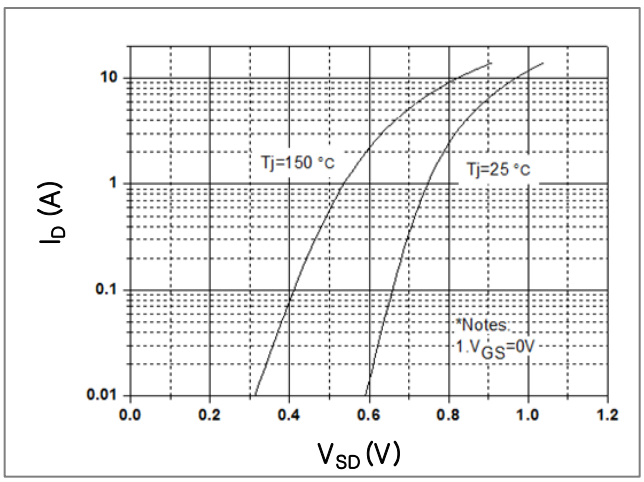
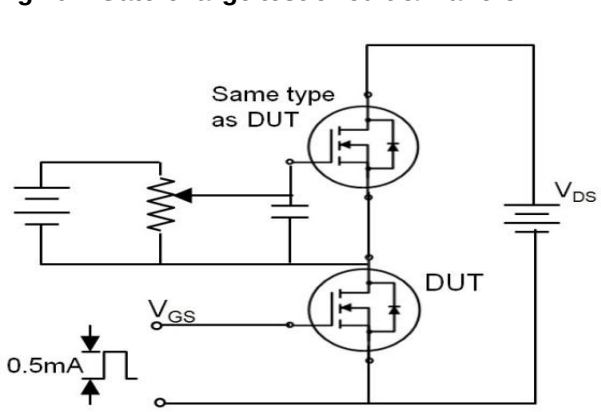


Fig 10. Gate charge test circuit & waveform



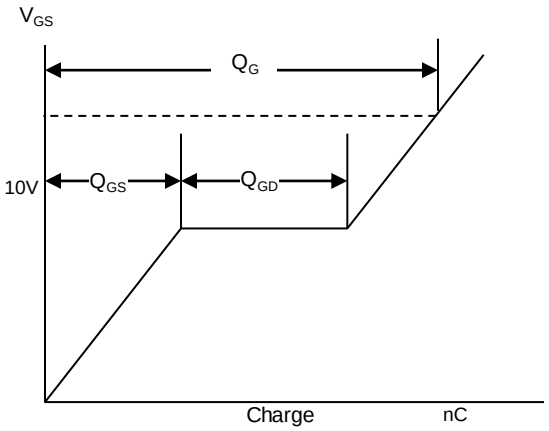


Fig 11. Switching time test circuit & waveform

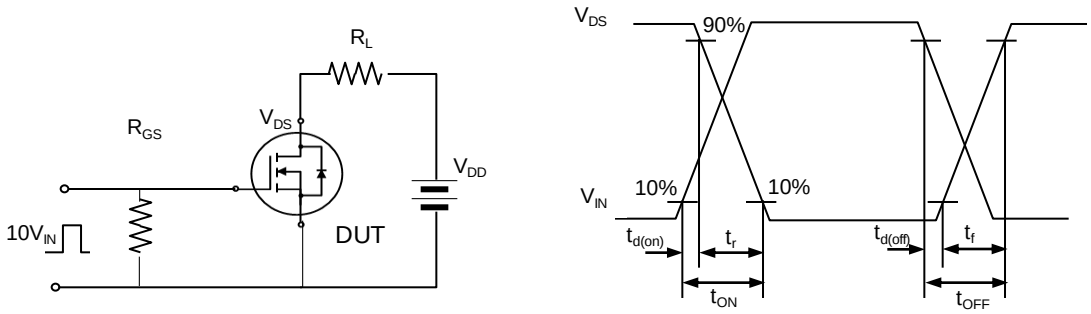


Fig 12. Unclamped Inductive switching test circuit & waveform

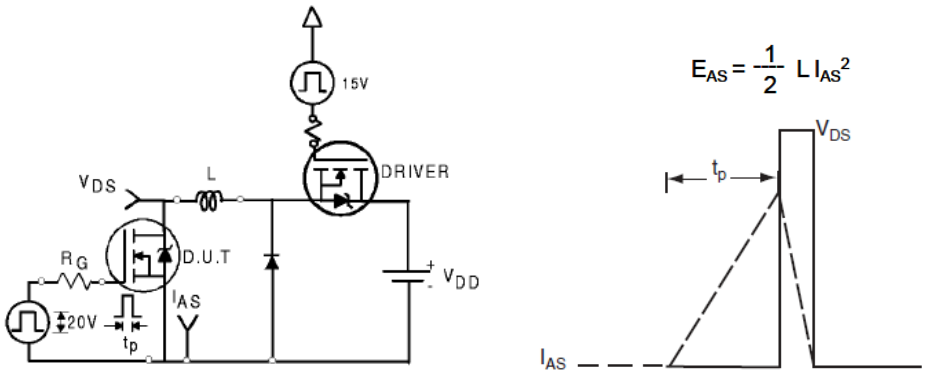
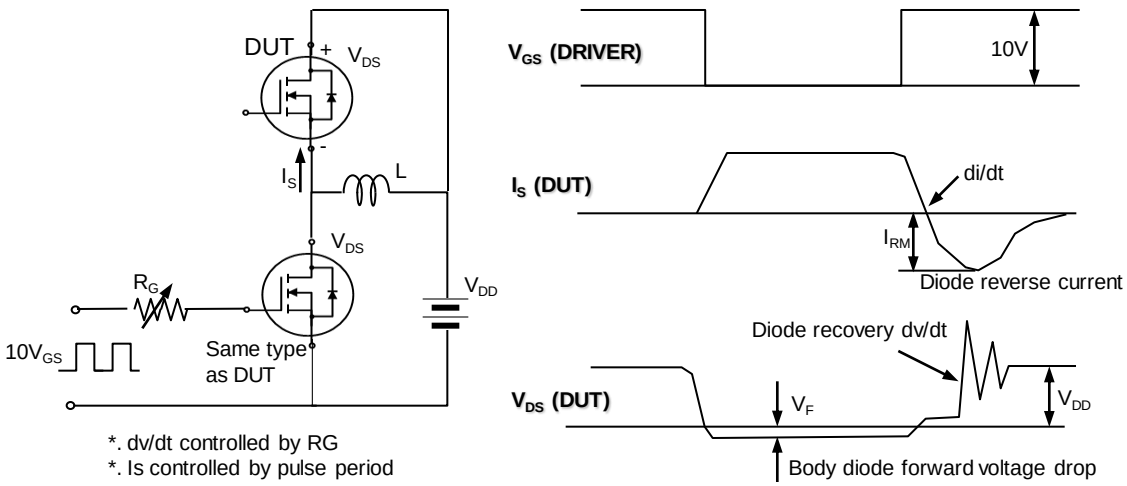


Fig 13. Peak diode recovery dv/dt test circuit & waveform



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