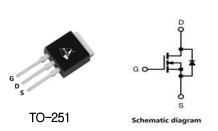


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N-channel Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	700			
R _{DS(on)} max. at 25°C (Ω)	V _{GS} =10V	1.3		
Q _g max. (nC)	42	1		
Q _{gs} (nC)	6			
Q _{gd} (nC)	12			
Configuration	single			



Features

- ID=7A(Vgs=10V)
- Ultra Low Gate Charge
- Improved dv/dt Capability
- 100% Avalanche Tested
- RoHS compliant

Applications

- Switching Mode Power Supplies (SMPS)
- PWM Motor Controls
- DC to DC Converters
- LED Lighting
- Bridge Circuits

ORDERING INFORMATION				
Device	SPE7N65G			
Device Package	TO-251			
Marking	7N65G			

ABSOLUTE MAXIMUM RATINGS (T _C = 25°C, unless otherwise noted)					
Parameter	Symbol	Limit	Unit		
Drain to Source Voltage	V _{DSS}	650	V		
Continuous Drain Current (@T _C =25°C)		7	А		
Continuous Drain Current (@T _C =100°C)	I _D	4.5	А		
Drain current pulsed (2)	I _{DM}	28	А		
Gate to Source Voltage	V _{GS}	30	V		
Single pulsed Avalanche Energy (3)	E _{AS}	367	mJ		
Peak diode Recovery dv/dt (4)	dv/dt	6	V/ns		
Total power dissipation (@T _C =25°C)		166	W		
Derating Factor above 25°C	P _D	1.33	W/ºC		
Operating Junction Temperature & Storage Temperature	T _{STG} , T _J	-55 to + 150	°C		
Maximum lead temperature for soldering purpose	TL	260	°C		
Mounting torque (5)		0.4~0.6	N.m		

Notes

- 1. Drain current is limited by maximum junction temperature.
- 2. Repetitive rating : pulse width limited by junction temperature.
- 3. L = 15mH, I_{AS} = 7A, V_{DD} = 50V, R_{G} =25 Ω , Starting at T_{J} = 25 $^{\circ}$ C
- I_{SD} ≤ 7A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Starting at T_J =25°C
 Mounting consideration for TO220 Fullpack:

M3 screw plus flat washer is suggested, free of burr between devices and contact area, the devices are to be mounted to a hole not larger than 3.6mm in contact diameter (chamfer included).



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THERMAL CHARACTERISTICS				
Parameter	Symbol	Value	Unit	
Thermal resistance, Junction to case	R _{thjc}	0.75	°C/W	
Thermal resistance, Junction to ambient	R _{thja}	82	°C/W	

ELECTRICAL CHARACTERISTICS (T _C = 25°C unless otherwise specified)							
Parameter	Symbol	Test conditions	Min.	Тур.	Max.	Unit	
Off Characteristics							
Drain to source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	650			V	
Breakdown voltage temperature coefficient	ΔBV _{DSS} / ΔTJ	I _D =250uA, referenced to 25°C		0.51		V/°C	
Drain to source leakage current	I _{DSS}	V _{DS} =650V, V _{GS} =0V			1	uA	
Drain to source leakage current		V _{DS} =520V, T _C =125°C			50	uA	
Gate to source leakage current, forward	I _{GSS}	V_{GS} =30V, V_{DS} =0V			100	nA	
Gate to source leakage current, reverse	IGSS	V_{GS} =-30V, V_{DS} =0V			-100	nA	
On Characteristics							
Gate threshold voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250uA	2		4	V	
Drain to source on state resistance	R _{DS(ON)}	V _{GS} =10V, I _D =3.5A		1.05	1.3	Ω	
Forward Transconductance	Gfs	$V_{DS} = 30 \text{ V}, I_{D} = 3.5 \text{ A}$		5.2		S	
Dynamic Characteristics							
Input capacitance	C _{iss}			1100			
Output capacitance	Coss	V_{GS} =0V, V_{DS} =25V, f=1MHz		110		pF	
Reverse transfer capacitance	C _{rss}			15			
Turn on delay time	t _{d(on)}			17			
Rising time	tr	\/ -290\/ -7A D -25O		33			
Turn off delay time	t _{d(off)}	$-V_{DS}$ =380V, I_{D} =7A , R_{G} =25 Ω		82		ns	
Fall time	t _f			41			
Total gate charge	Q_g			37			
Gate-source charge	Q _{gs}	V _{DS} =520V, V _{GS} =10V, I _D =7A	1	6		nC	
Gate-drain charge	Q_{gd}			12			

SOURCE TO DRAIN DIODE RATINGS CHARACTERISTICS							
Parameter	Symbol	Test conditions	Min.	Тур.	Max.	Unit	
Continuous source current	Is	Integral reverse p-n Junction L diode in the MOSFET			7	Α	
Pulsed source current	I _{SM}				28	Α	
Diode forward voltage drop.	V _{SD}	I _S =7A, V _{GS} =0V			1.2	٧	
Reverse recovery time	T _{rr}	I _S =7A, V _{GS} =0V, dI _F /dt=100A/us		450		ns	
Reverse recovery Charge	Qrr			9.1		uC	

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Fig1. Output characteristics

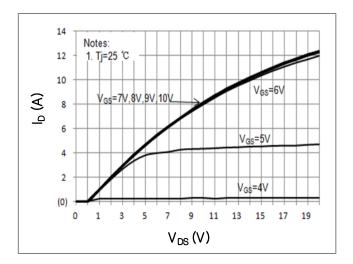


Fig3. Gate charge characteristics

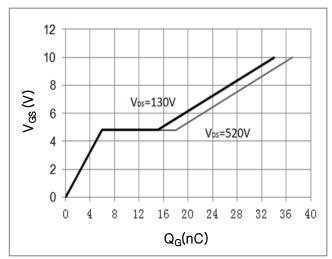


Fig 5. RDS(ON) vs junction temperature

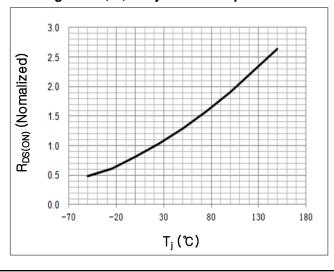


Fig2. Drain-source on-state resistance

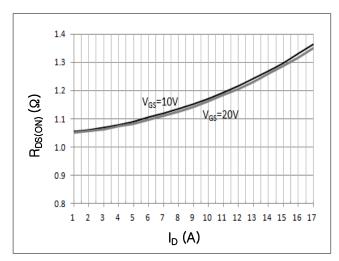


Fig 4. Capacitance Characteristics

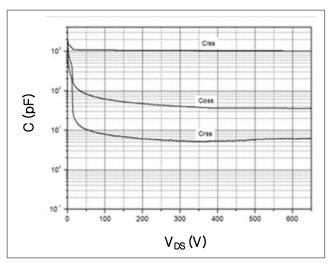
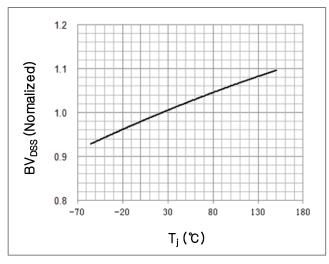


Fig 6. BVDss vs junction temperature



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Fig 7. Safe operating area

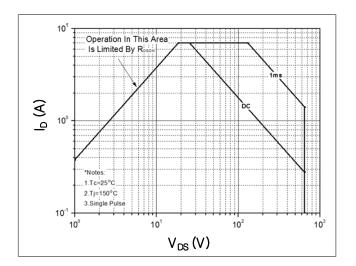


Fig 8. Transient thermal impedance

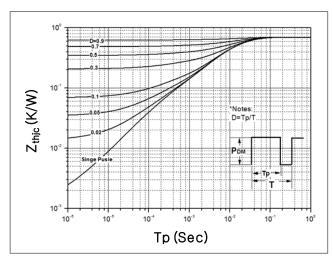


Fig 9. Forward characteristics of reverse diode

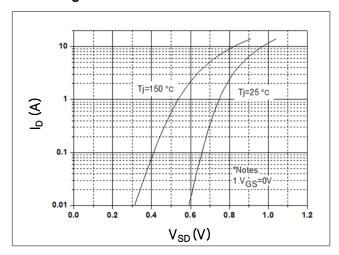
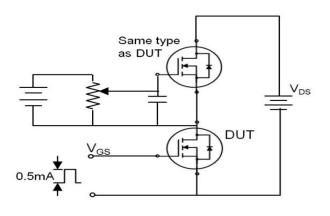


Fig 10. Gate charge test circuit & waveform



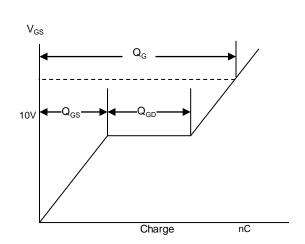




Fig 11. Switching time test circuit & waveform

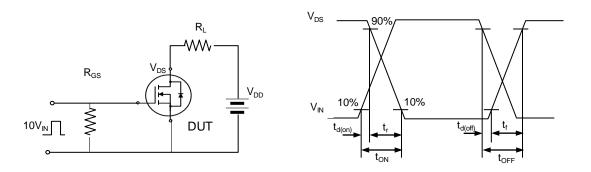


Fig 12. Unclamped Inductive switching test circuit & waveform

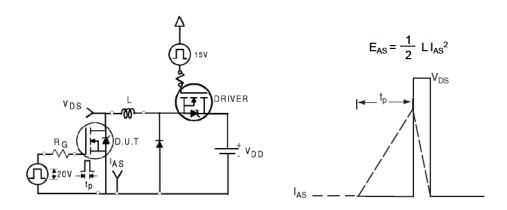
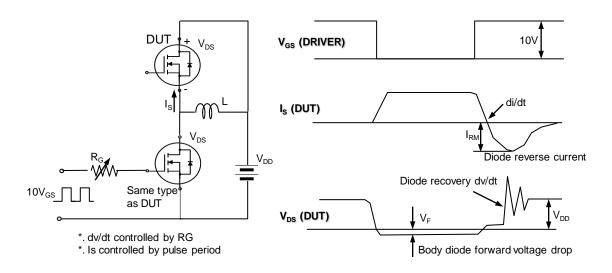


Fig 13. Peak diode recovery dv/dt test circuit & waveform





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