SDM021G10K2D

100V SGT N-Channel MOSFETs

Rev A.0

Feature

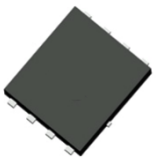
- Low $R_{DS(ON)}$
- Low Gate Charge
- High current Capability
- Green product (RoHS compliant), lead free
- 100% UIS Tested,100% Rg Tested
- AEC-Q101 qualified

Product Summary

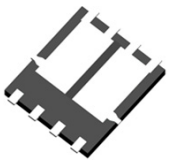
V_{DS}	100	V
$V_{GS(th)\_Typ}$	2.0	V
$R_{DS(ON)\_Typ}$ (at V_{GS} =10V)	17	mΩ
I_D (at V_{GS} =10V)	31	A

Type	Package	Marking	Outline	Media	Quantity (pcs)
SDM021G10K2D	PDFN5x6-8L-D	M021G10D	Tape	13”Reel	5000

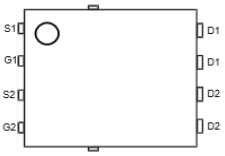
Top View



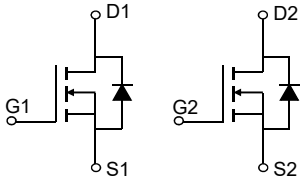
Bottom View



Pin Configuration
Top View



Chip-1 & Chip-2



Absolute Maximum Ratings (Rating at T_C=25°C unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current(1)	T_C=25°C	I_D	31	A
	T_C=100°C		19	
Maximum Body-Diode Continuous Current		I_S	39	A
Pulsed Drain Current (2)		I_{DM}	93	A
Avalanche Energy (3)		E_{AS}	29	mJ
Avalanche Current(3)		I_{AS}	24	A
Power Dissipation(4)	T_C=25°C	P_D	39	W
	T_C=100°C		16	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (Rating at T_C=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS} =0V	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS} =0V	-	-	1	μA
		T_J=55°C	-	-	5	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS} =±20V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1.2	2.0	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A	-	17	21	mΩ
		V_{GS}=4.5V, I_D=15A	-	22	29	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V	-	0.68	1.0	V
DYNAMIC PARAMETERS(5)						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	771	-	pF
C_{oss}	Output Capacitance		-	173	-	pF
C_{rss}	Reverse Transfer Capacitance		-	5.3	-	pF
R_g	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	1.9	-	Ω
SWITCHING PARAMETERS(5)						
Q_g(10V)	Total Gate Charge	V_{GS}=0 to 10V, V_{DS}=50V, I_D=20A	-	12.9	-	nC
Q_g(4.5V)	Total Gate Charge		-	6.9	-	nC
Q_{gs}	Gate Source Charge		-	2.1	-	nC
Q_{gd}	Gate Drain Charge		-	3.5	-	nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=50V, R_L=2.5Ω, R_G=6Ω	-	4.5	-	ns
t_r	Turn-On Rise Time		-	5.3	-	ns
$t_{D(off)}$	Turn-Off Delay Time		-	16.9	-	ns
t_f	Turn-Off Fall Time		-	8.9	-	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=15A, di/dt=100A/μs	-	41	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=15A, di/dt=100A/μs	-	31	-	nC

Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal resistance from junction to Ambient	55	70	°C /W
$R_{\theta JC}$	Thermal resistance from junction to Case	2.5	3.2	°C /W

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under T_{J_Max} = 150°C.
3. This single-pulse measurement was taken under the following condition [L = 100μH, V_{GS} = 10V, V_{DS} = 50V] while its value is limited byT_{J_Max} = 150°C.
4. The power dissipation P_D is based on T_{J_Max} = 150°C.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics

Figure 1: Saturation Characteristics

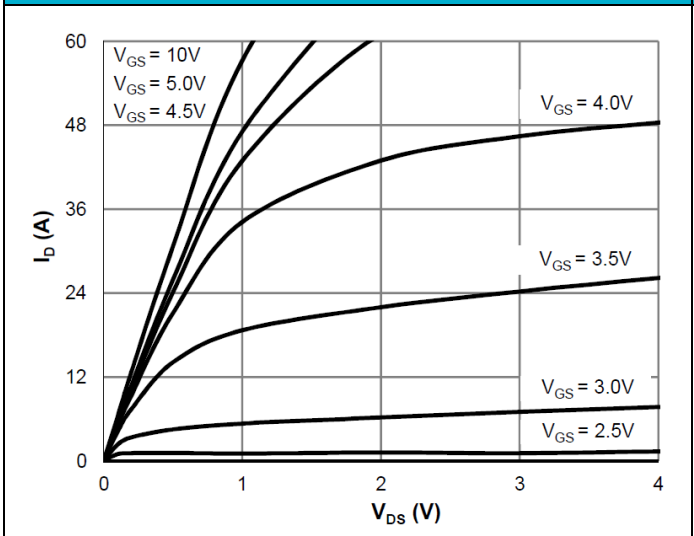


Figure 2: Transfer Characteristics

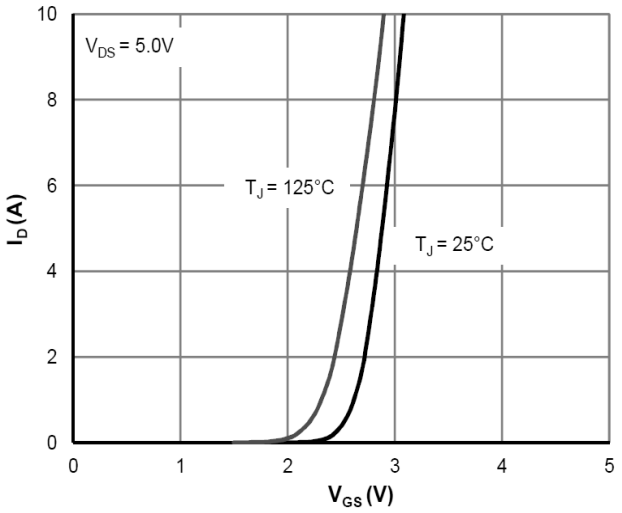


Figure 3: On-resistance vs. Drain Current

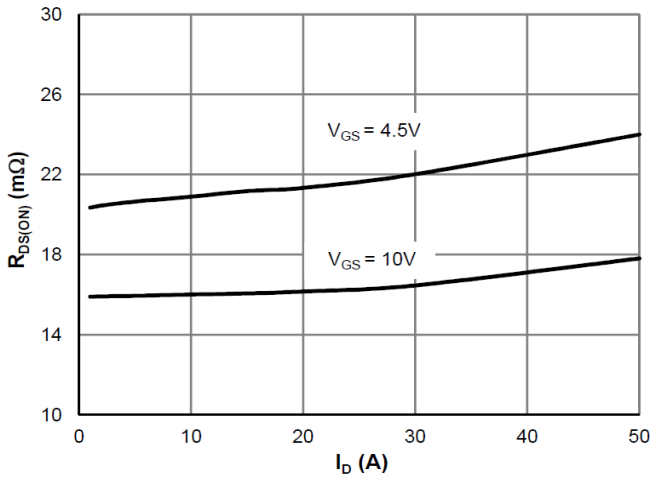


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

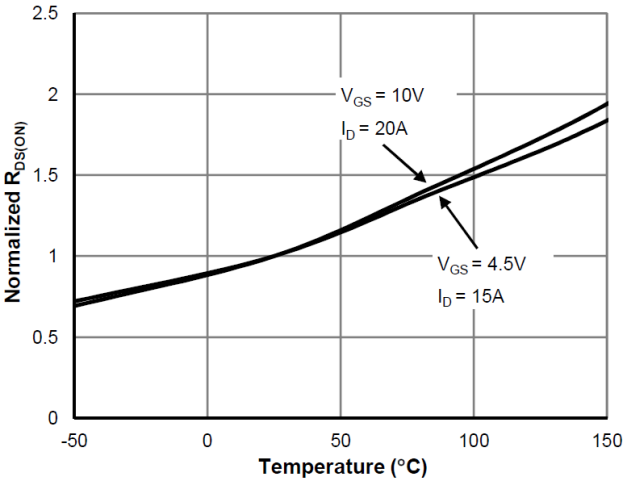


Figure 5: Rds(ON) vs. V_{GS}

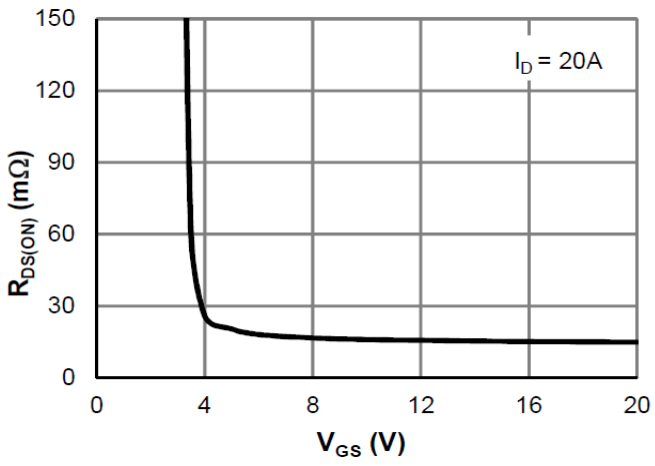
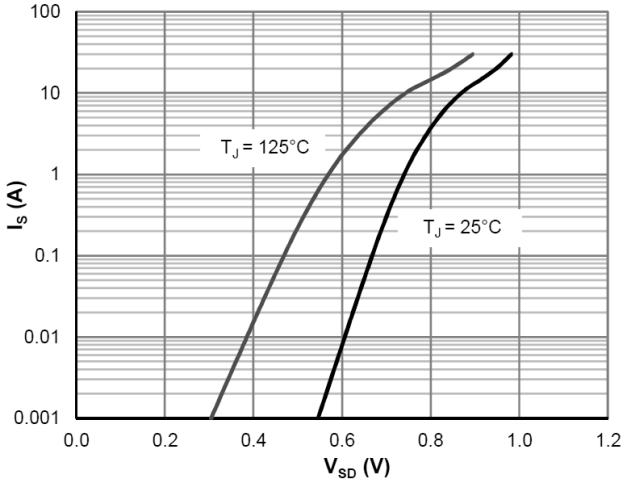


Figure 6: Body Diode Characteristics



Typical Electrical and Thermal Characteristics

Figure 7 Gate-Charge characteristics

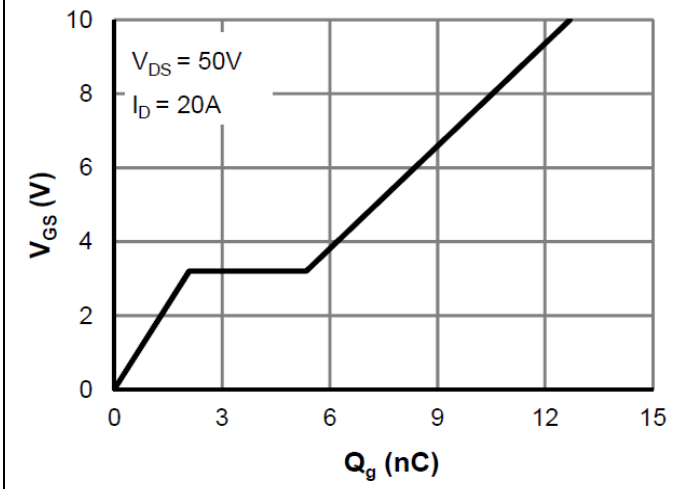


Figure 8: Capacitance characteristics

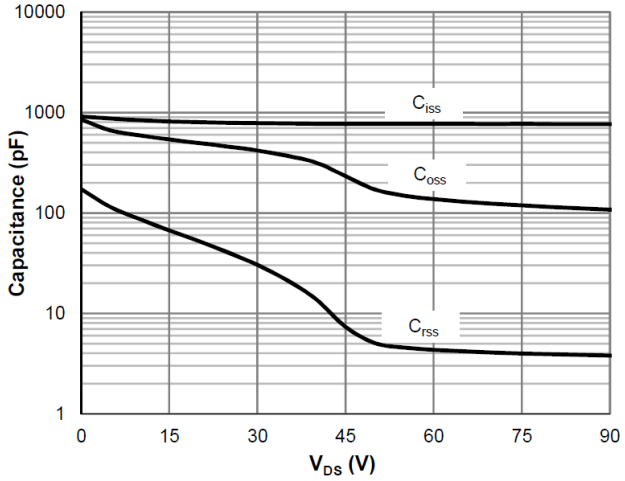


Figure 9: Current De-rating

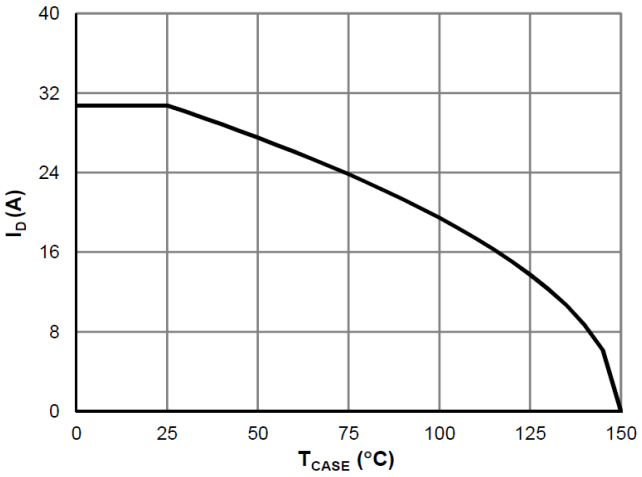


Figure 10: Power De-rating

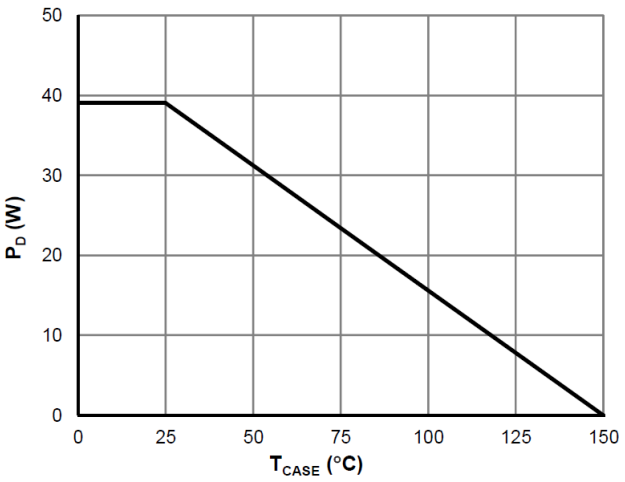


Figure 11: Maximum Safe Operating Area

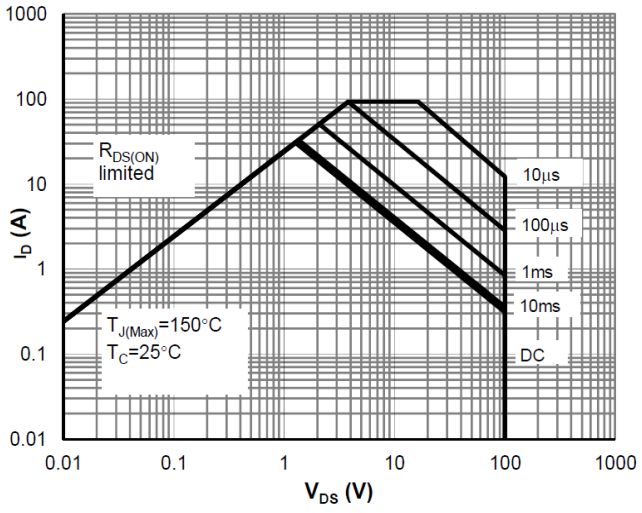
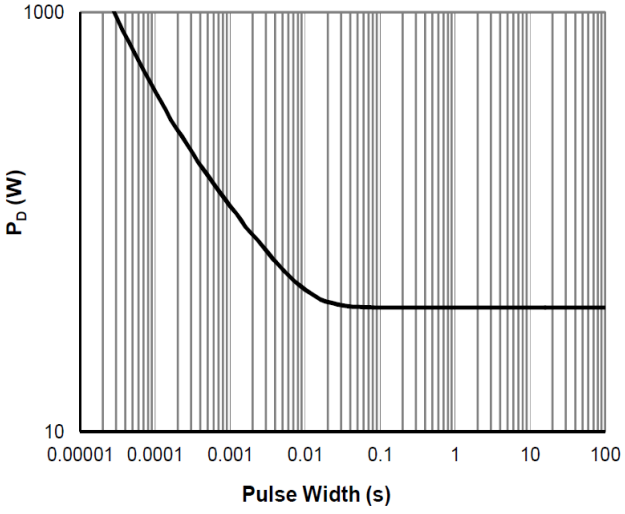
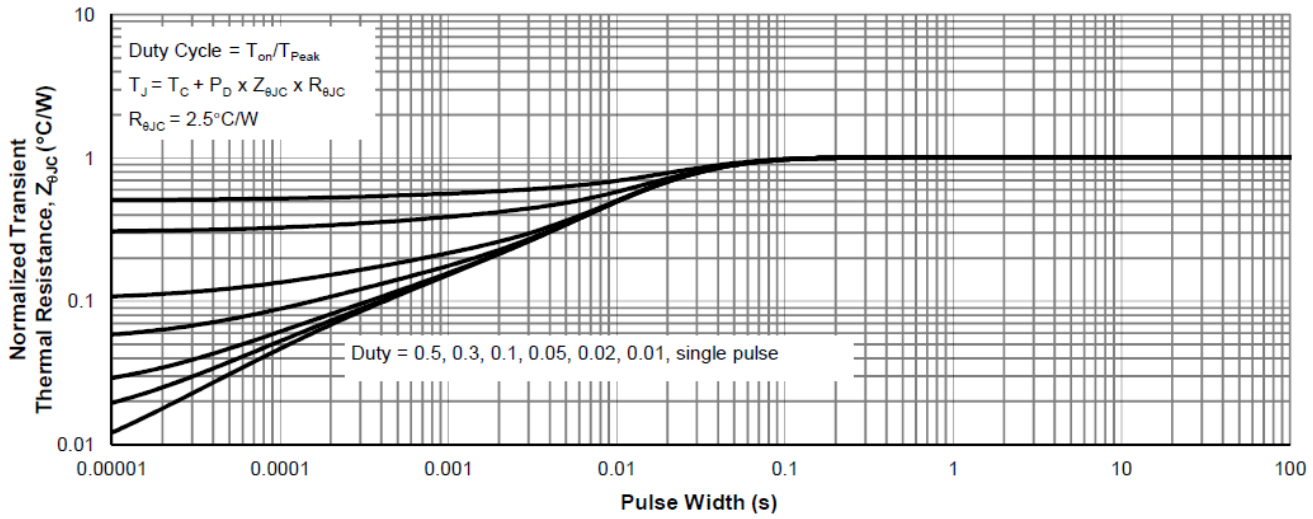


Figure 12: Single Pulse Power Rating, Junction-to-Case



Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance



Test Circuit

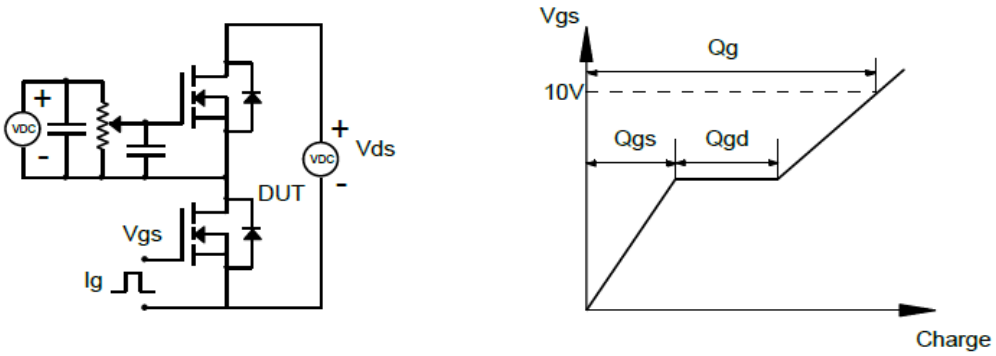


Figure1: Gate Charge Test Circuit & Waveforms

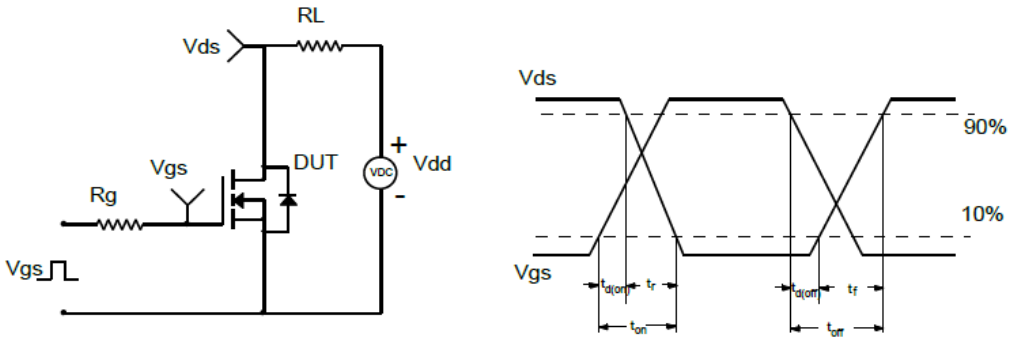


Figure2: Resistive Switching Test Circuit & Waveforms

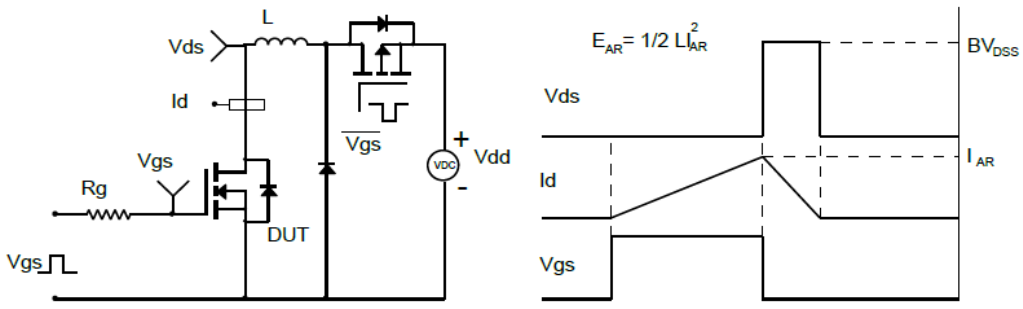


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

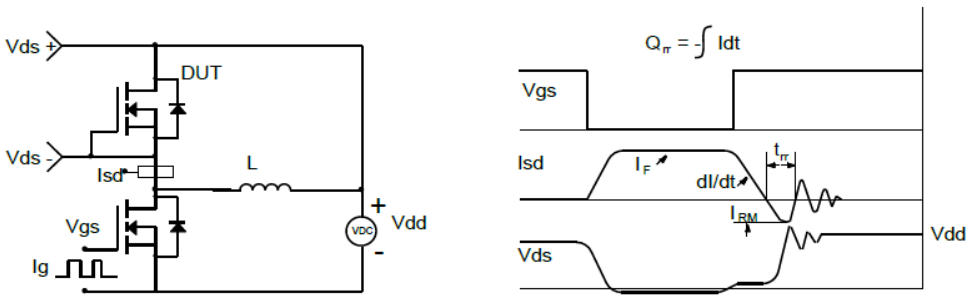
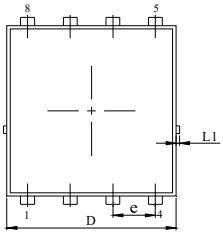
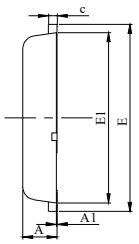


Figure4: Diode Recovery Test Circuit & Waveforms

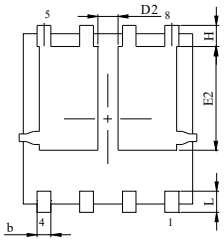
PDFN5x6-8L-D Package Information



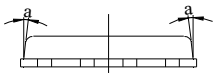
Top View



Side View



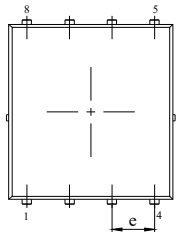
Bottom View



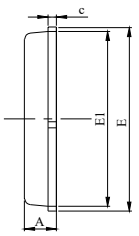
Front View

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.10
b	0.31	0.41	0.51
c	0.23	-	0.33
D	4.95	5.05	5.15
D1	4.00	4.10	4.20
D2	0.50	0.60	0.70
E	6.05	6.15	6.25
E1	5.50	5.60	5.70
E2	3.31	3.41	3.51
e	1.27BSC		
H	0.60	0.70	0.80
L	0.50	0.70	0.80
L1	-	-	0.125
a	-	-	12°

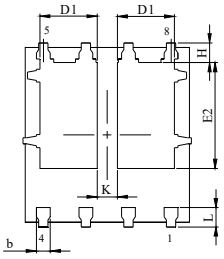
Type-B Package Outline



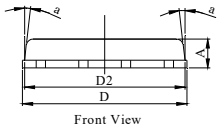
Top View



Side View



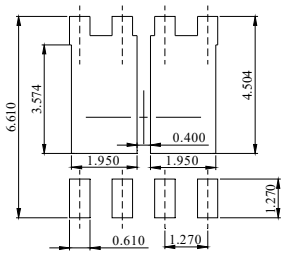
Bottom View



Front View

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.20	0.30	0.40
c	0.21	0.25	0.34
D	4.90	5.00	5.10
D1	1.60	1.70	1.80
D2	4.80	4.90	5.00
E	5.90	6.00	6.10
E1	5.65	5.75	5.85
E2	3.37	3.48	3.58
e	1.27BSC		
H	0.55	0.65	0.75
L	0.55	0.65	0.75
K	0.50	0.60	0.70
a	0°	--	12°

Recommended Soldering Footprint



DIMENSIONS:MILLIMETERS