# SDM028N02QBD

## 20V Dual N-Channel MOSFETs

Rev A.0

### Feature

- Low $R_{DS(ON)}$
- Low Gate Charge
- High current Capability
- Green product (RoHS compliant), lead free
- 100% UIS Tested

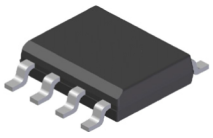
### Product Summary

| | | |
|---|---|---|
| $V_{DS}$ | 20 | V |
| $V_{GS(th)\_Typ}$ | 0.75 | V |
| $R_{DS(ON)\_Typ}$ (at $V_{GS}$ =4.5V) | 21 | mΩ |
| $I_D$ (at $V_{GS}$ =4.5V) (1) | 6 | A |

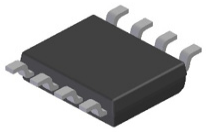
| Type | Package | Marking | Outline | Media | Quantity (pcs) |
|---|---|---|---|---|---|
| SDM028N02QBD | SOP-8 | 9926B | Tape | 13” Reel | 4000 |

SOP-8

Top View

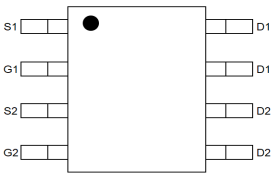


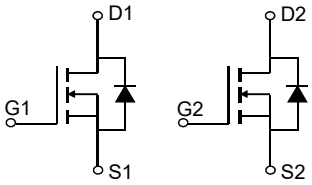
Bottom View



Pin Configuration

Top View




Chip-1 & Chip-2

### Absolute Maximum Ratings (Rating at $T_A$=25°C unless otherwise noted)

| Parameter | | Symbol | Maximum | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±12 | V |
| Continuous Drain Current (1) | $T_A$=25°C | $I_D$ | 6 | A |
| | $T_A$=100°C | | 4 | |
| Pulsed Drain Current (2) | | $I_{DM}$ | 24 | A |
| Maximum Body-Diode Continuous Current | | $I_S$ | 6 | A |
| Avalanche Energy (3) | | $E_{AS}$ | 7.5 | mJ |
| Power Dissipation (4) | $T_A$=25°C | $P_D$ | 1.7 | W |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to +150 | °C |

## Electrical Characteristics (Rating at $T_J$=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250μA, $V_{GS}$ =0V | 20 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=20V, $V_{GS}$ =0V | - | - | 1 | μA |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{DS}$=0V, $V_{GS}$ =±12V | - | - | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$= $V_{GS}$, $I_D$=250μA | 0.5 | 0.75 | 1 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=4.5V, $I_D$=6A | - | 21 | 27 | mΩ |
| | | $V_{GS}$=2.5V, $I_D$=5A | - | 25 | 33 | mΩ |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=6A, $V_{GS}$=0V | - | - | 1.2 | V |
| **DYNAMIC PARAMETERS** (5) | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=10V, f=1MHz | - | 457 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 65 | - | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 57 | - | pF |
| **SWITCHING PARAMETERS** (5) | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=0 to 4.5V, $V_{DS}$=10V, $I_D$=2A | - | 6.1 | - | nC |
| $Q_{gs}$ | Gate Source Charge | | - | 1.1 | - | nC |
| $Q_{gd}$ | Gate Drain Charge | | - | 1.7 | - | nC |
| $t_{D(on)}$ | Turn-On Delay Time | $V_{GS}$=4.5V, $V_{DS}$=10V, $I_D$=2A, $R_{GEN}$=3Ω | - | 4.1 | - | ns |
| $t_r$ | Turn-On Rise Time | | - | 13.1 | - | ns |
| $t_{D(off)}$ | Turn-Off Delay Time | | - | 67 | - | ns |
| $t_f$ | Turn-Off Fall Time | | - | 35 | - | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=2A, di/dt=60A/μs | - | 6.1 | - | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=2A, di/dt=60A/μs | - | 0.9 | - | nC |

## Thermal Resistances

| Symbol | Parameter | Typ | Max | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance from junction to Ambient | - | 75 | °C /W |

**Notes:**

1. Computed continuous current assumes the condition of $T_{J\_Max}$ while the actual continuous depends on the thermal & electro-mechanical application board design.

2. This single-pulse measurement was taken under $T_{J\_Max}$=150°C.

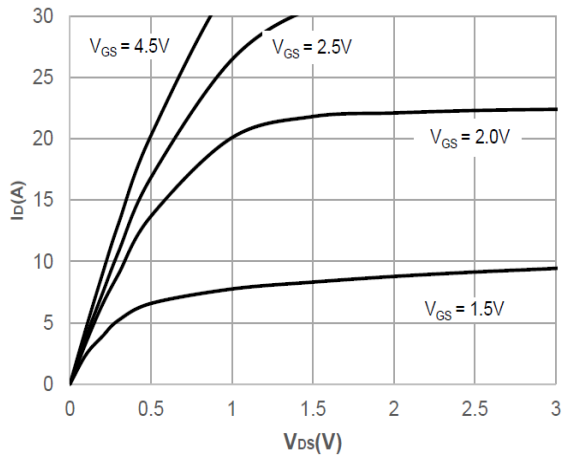
3. This single-pulse measurement was taken under the following condition [L=0.5mH, $V_{GS}$=10V, $V_{DS}$=10V] while its value is limited by $T_{J\_Max}$=150°C.

4. The power dissipation $P_D$ is based on $T_{J\_Max}$=150°C.

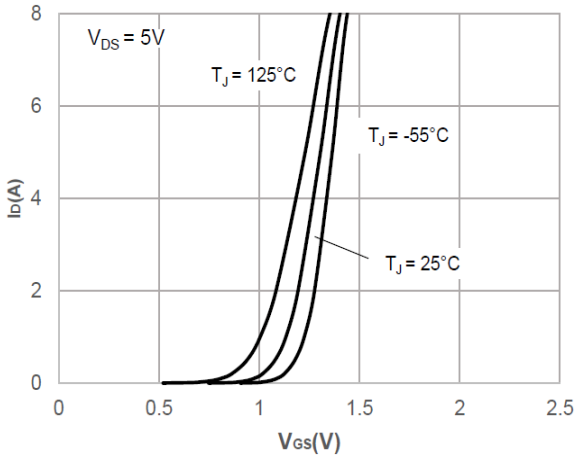
5. This value is guaranteed by design hence it is not included in the production test.

## Typical Electrical and Thermal Characteristics

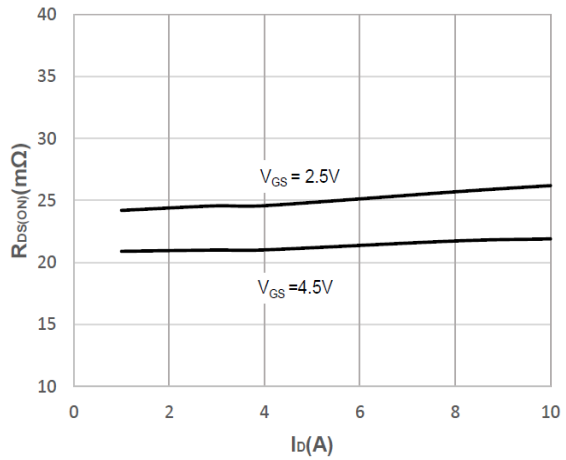
### Figure 1: Saturation Characteristics



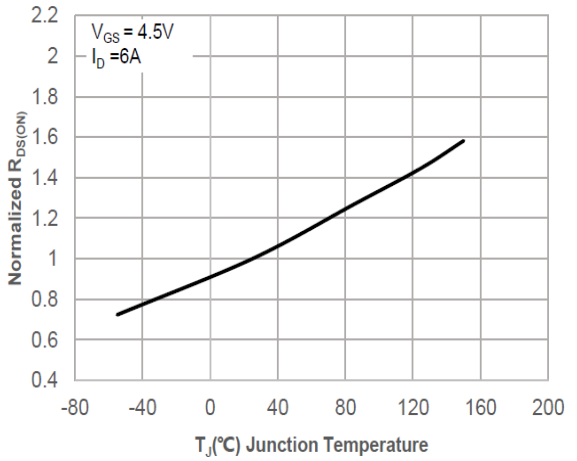

### Figure 2: Transfer Characteristics



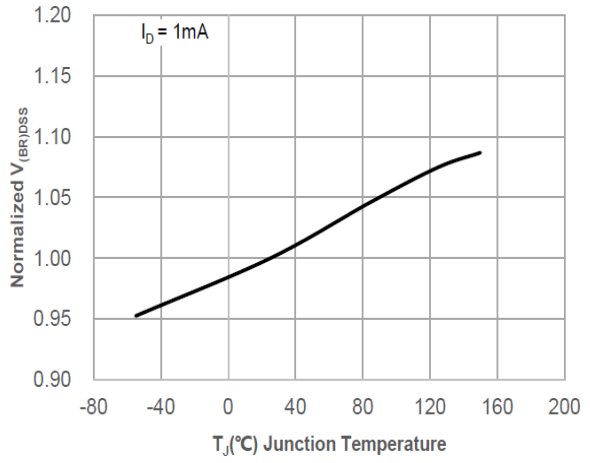

### Figure 3: $R_{DS(ON)}$ vs. Drain Current



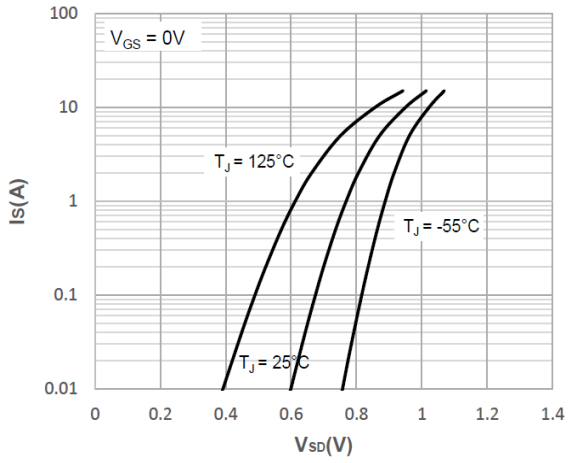

### Figure 4: $R_{DS(ON)}$ vs. Junction Temperature




### Figure 5: BVDSS vs. Junction Temperature




### Figure 6: Body-Diode Characteristics



## Typical Electrical and Thermal Characteristics

Figure 7: Gate-Charge characteristics

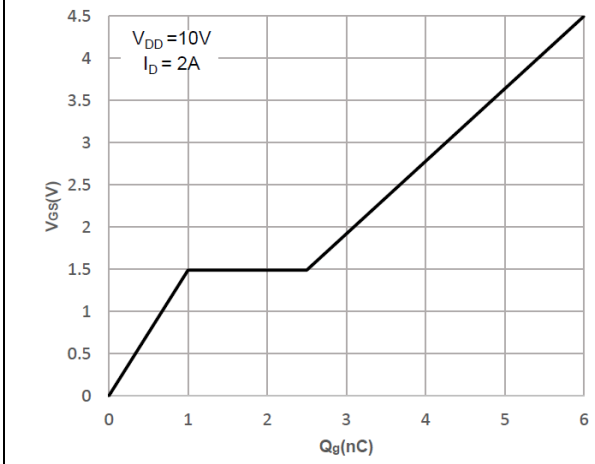



Figure 8: Capacitance characteristics

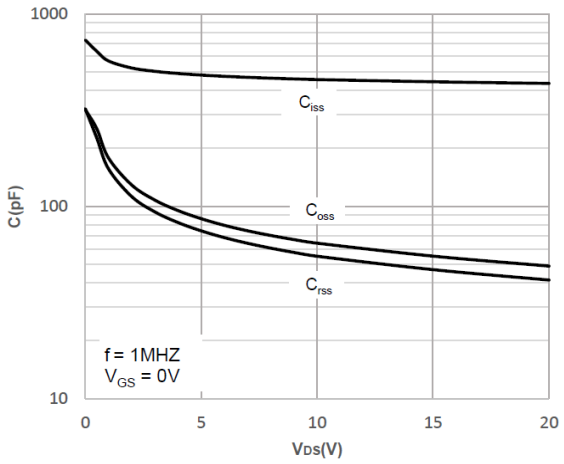



Figure 9: Current De-rating

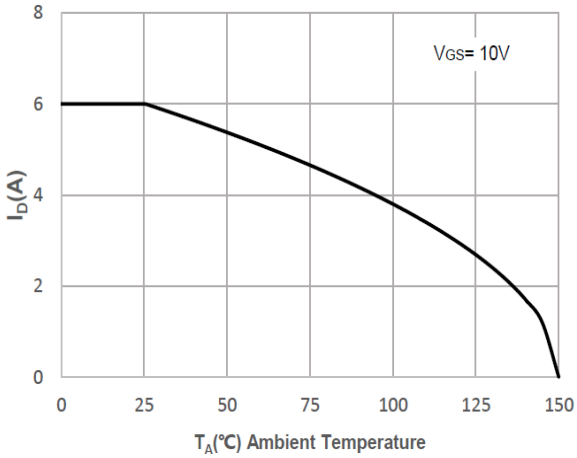



Figure 10: Maximum Safe Operating Area

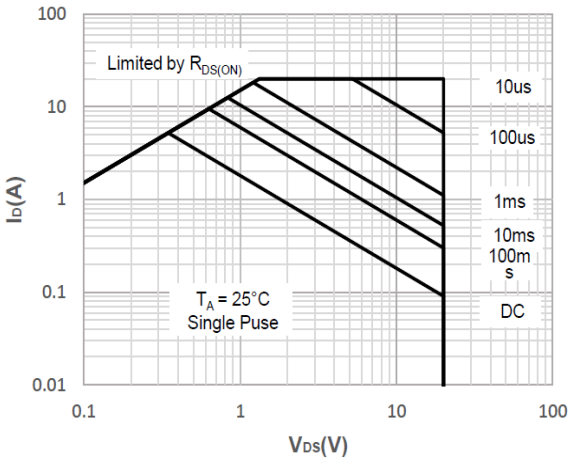



Figure 11: Peak Current Capacity

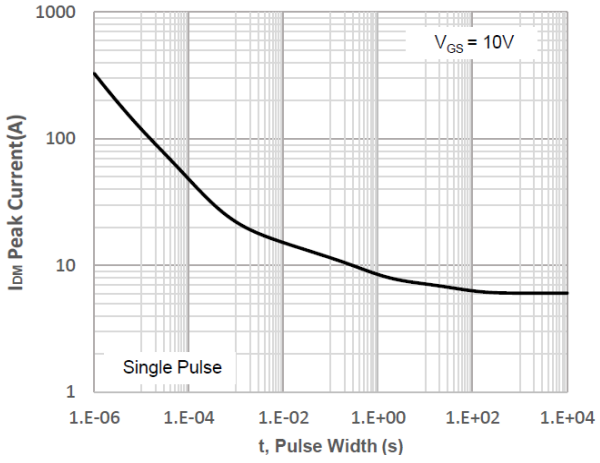
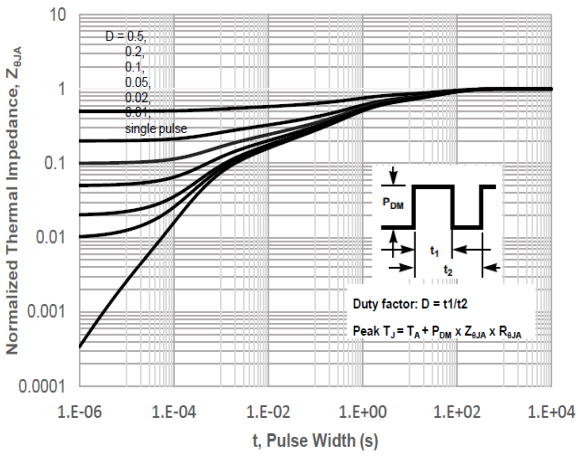



Figure 12: Normalized Maximum Transient Thermal Impedance



## Test Circuit

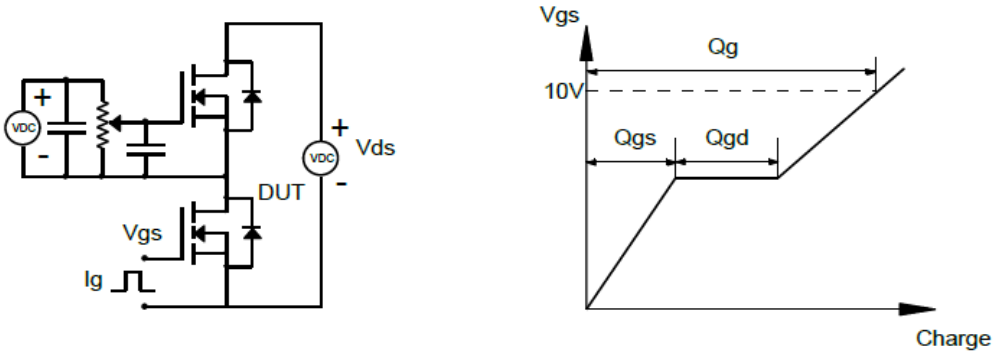



Figure1: Gate Charge Test Circuit & Waveforms

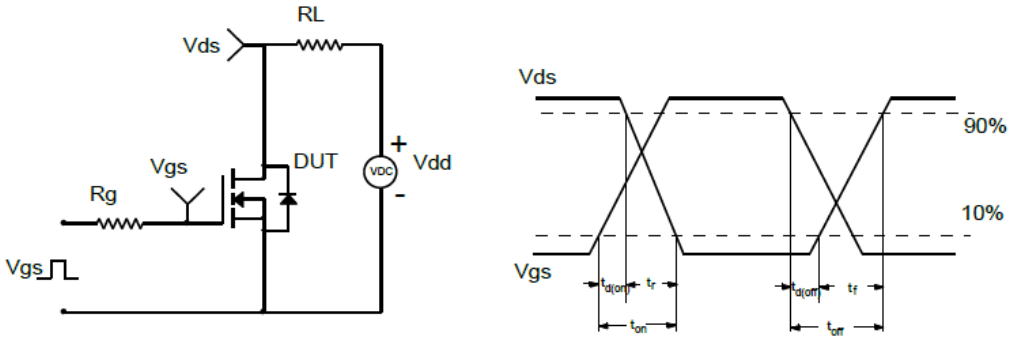



Figure2: Resistive Switching Test Circuit & Waveforms

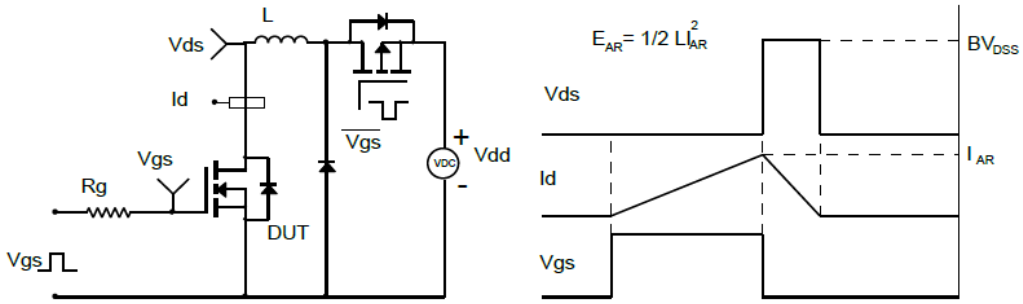



Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

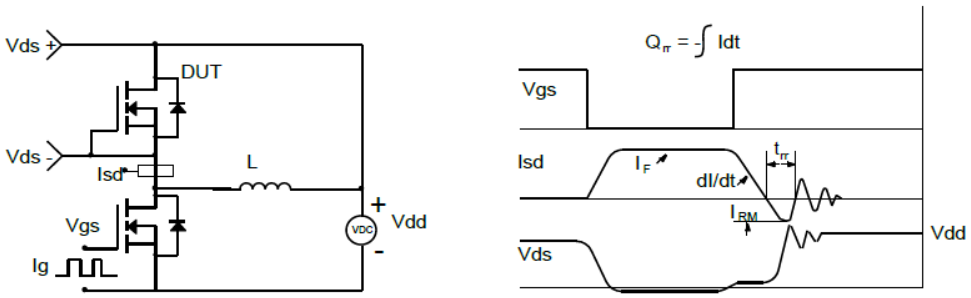
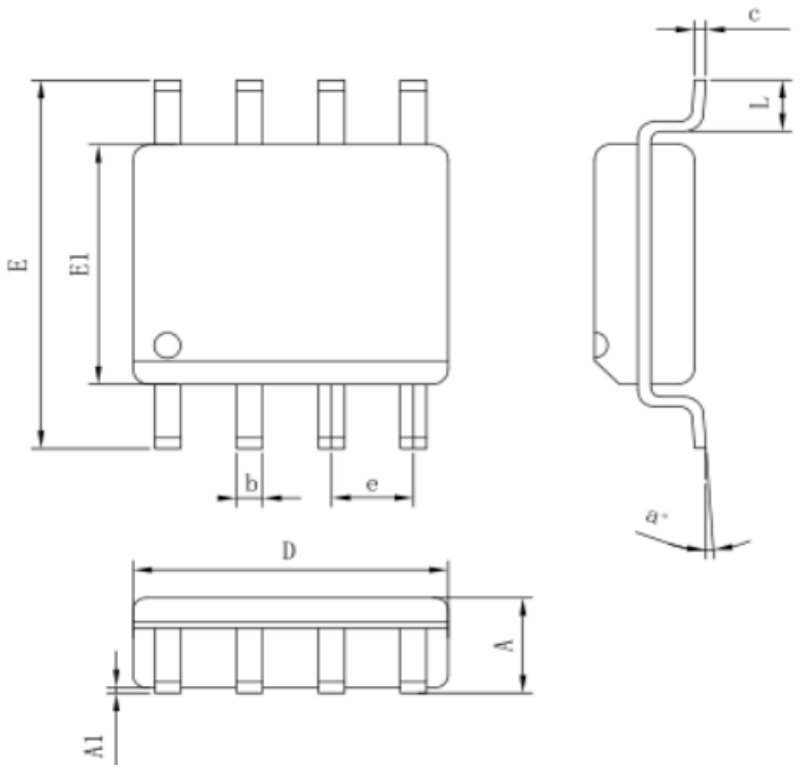



Figure4: Diode Recovery Test Circuit & Waveforms

## SOP-8 Package Information




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | -- | 1.75 |
| A1 | 0.10 | -- | 0.23 |
| b | 0.35 | -- | 0.48 |
| c | 0.19 | -- | 0.25 |
| D | 4.70 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.70 | 3.90 | 4.10 |
| e | 1.27BSC | | |
| L | 0.50 | -- | 0.80 |
| a° | 0° | -- | 8° |