

SDM029N06D

60V N-Channel MOSFETs

Rev A.1

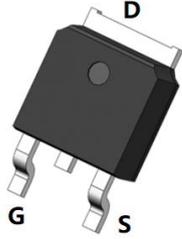
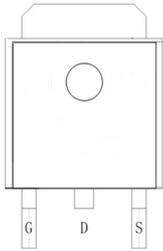
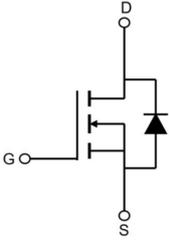
Feature

- ✧ Excellent $R_{DS(ON)}$
- ✧ Low Gate Charge
- ✧ High current Capability
- ✧ Green product (RoHS compliant), lead free
- ✧ 100% UIS Tested
- ✧ AEC-Q101 qualified

Product Summary

V_{DS}	60	V
$V_{GS(th_Typ)}$	1.6	V
$R_{DS(ON)_Typ}$ (at $V_{GS} = 10V$)	25	m Ω
I_D (at $V_{GS} = 10V$)	30	A

Type	Package	Marking	Outline	Media	Quantity (pcs)
SDM029N06D	TO-252	M029N06	Tape	13" Reel	2500

 <p>TO-252 top view</p>	 <p>pin Assignment</p>	 <p>Schematic Diagram</p>
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Absolute Maximum Ratings (Rating at $T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ C$	30
		$T_C=100^\circ C$	19
Maximum Body-Diode Continuous Current	I_S	30	A
Avalanche Energy ⁽¹⁾	E_{AS}	44	mJ
Power Dissipation	P_D	$T_C=25^\circ C$	37
		$T_C=100^\circ C$	15
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Electrical Characteristics (Rating at $T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 25\text{V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.1	1.6	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ⁽³⁾	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	-	25	29	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=15\text{A}$	-	28	40	
V_{SD}	Diode Forward Voltage	$I_S=20\text{A}$, $V_{GS}=0\text{V}$	-	-	1.2	V
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=30\text{V}$, $f=1\text{MHz}$	1019	1429	1929	pF
C_{oss}	Output Capacitance		45	65	87	pF
C_{rss}	Reverse Transfer Capacitance		37	53	71	pF
R_g	Gate Resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	-	2.4	-	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=0$ to 10V , $V_{DS}=30\text{V}$, $I_D=20\text{A}$	19	27	37	nC
Q_{gs}	Gate Source Charge		3.9	5.7	7.9	nC
Q_{gd}	Gate Drain Charge		3.7	4.9	6.7	nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DD}=30\text{V}$, $I_D=20\text{A}$, $R_{GEN}=3\Omega$	-	5.9	-	ns
t_r	Turn-On Rise Time		-	13	-	ns
$t_{D(off)}$	Turn-Off Delay Time		-	25	-	ns
t_f	Turn-Off Fall Time		-	3.9	-	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	15	21	29	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	27	-	nC

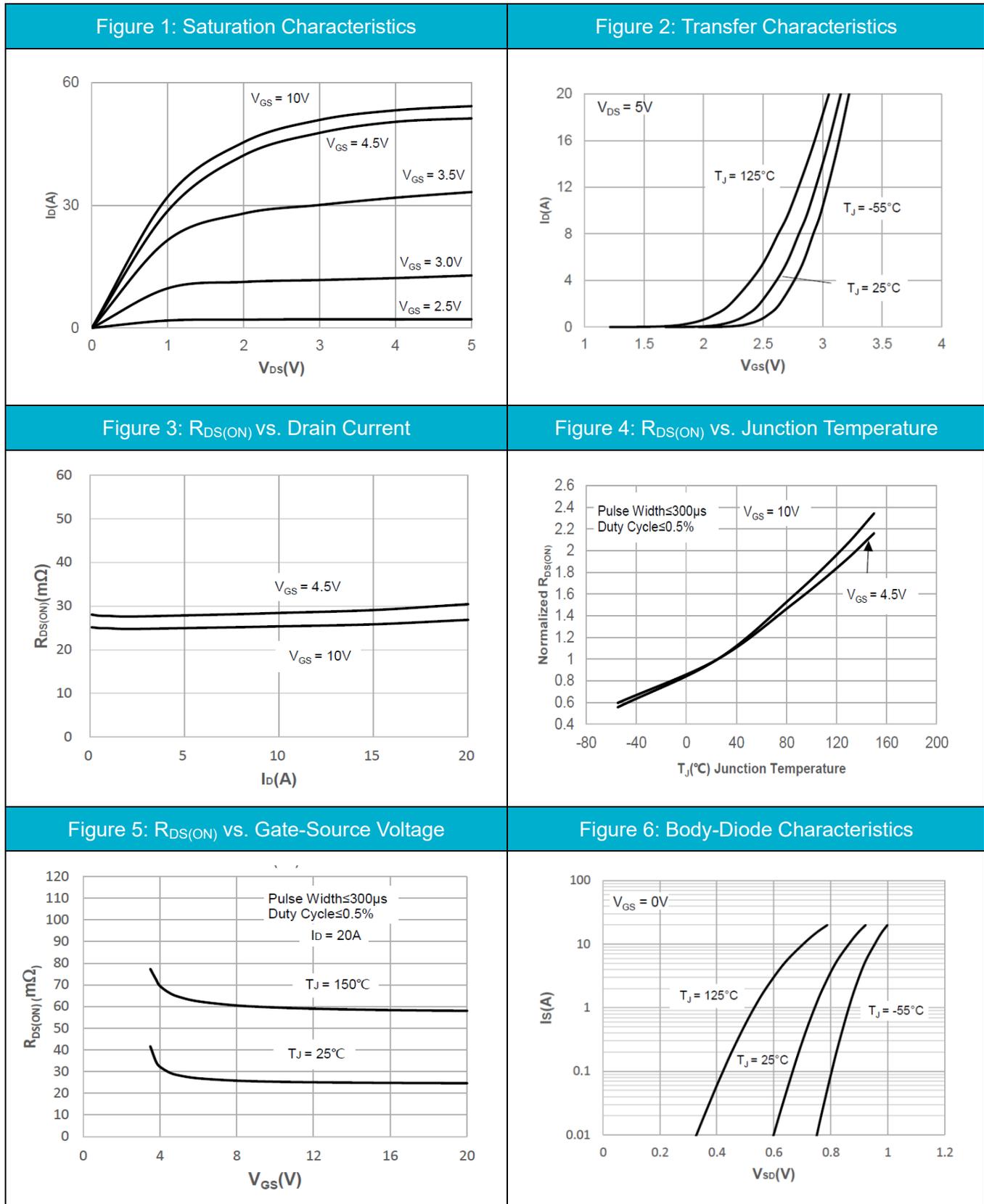
Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal resistance from junction to case	-	3.4	$^{\circ}\text{C} / \text{W}$
$R_{\theta JA}$	Thermal resistance from junction to Ambient ⁽²⁾	-	39	$^{\circ}\text{C} / \text{W}$

Notes:

1. E_{AS} condition: Starting $T_J=25^{\circ}\text{C}$, $V_{DD}=30\text{V}$, $V_G=10\text{V}$, $R_G=25\text{ohm}$, $L=0.5\text{mH}$, $I_{AS}=10.92\text{A}$, $V_{DD}=0\text{V}$ during time in avalanche.
2. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.
3. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Electrical and Thermal Characteristics



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Figure 7: Gate-Charge characteristics

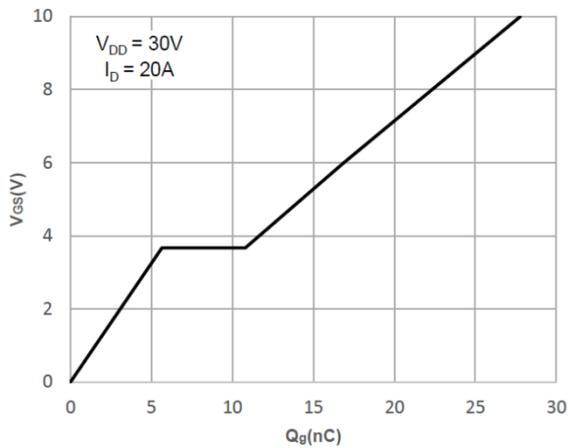


Figure 8: Capacitance characteristics

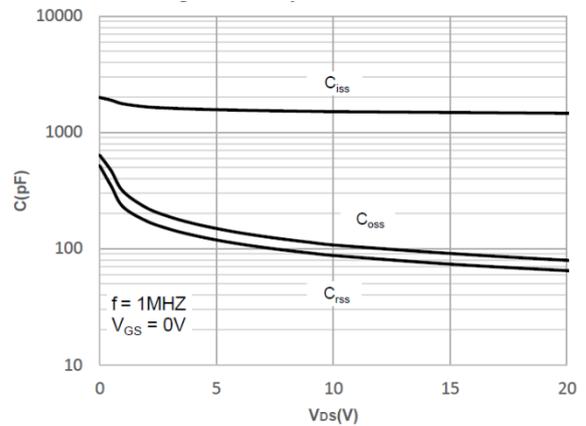


Figure 9: Current De-rating

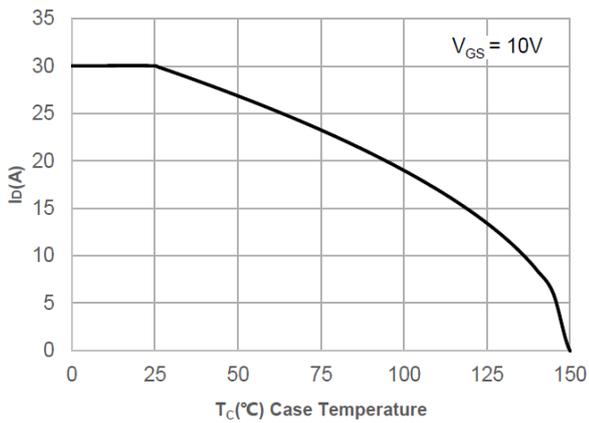


Figure 10: Power De-rating

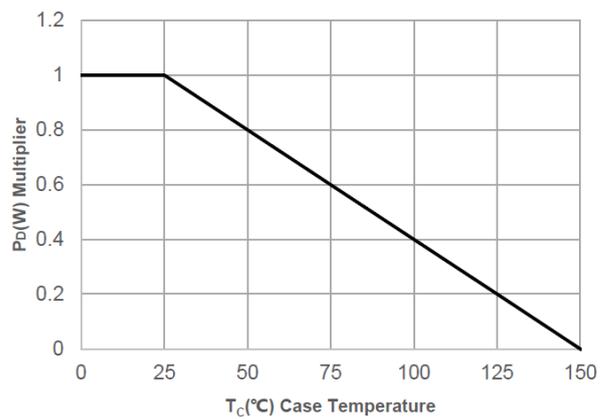


Figure 11: Maximum Safe Operating Area

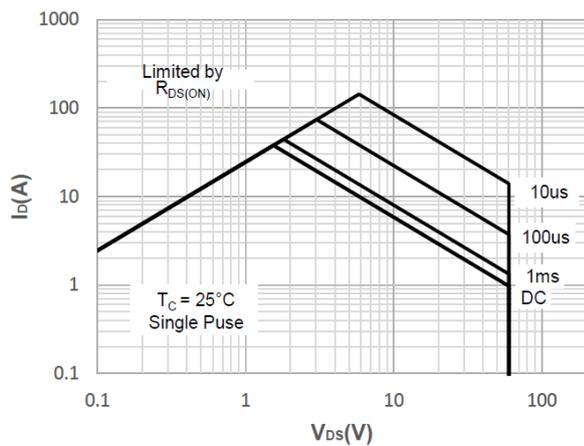
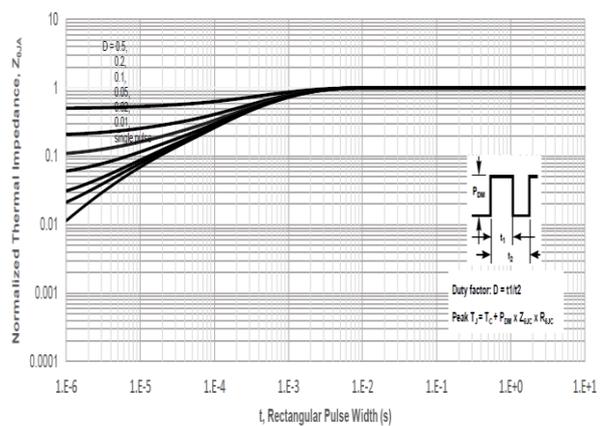


Figure 12: Normalized Maximum Transient Thermal Impedance



Test Circuit

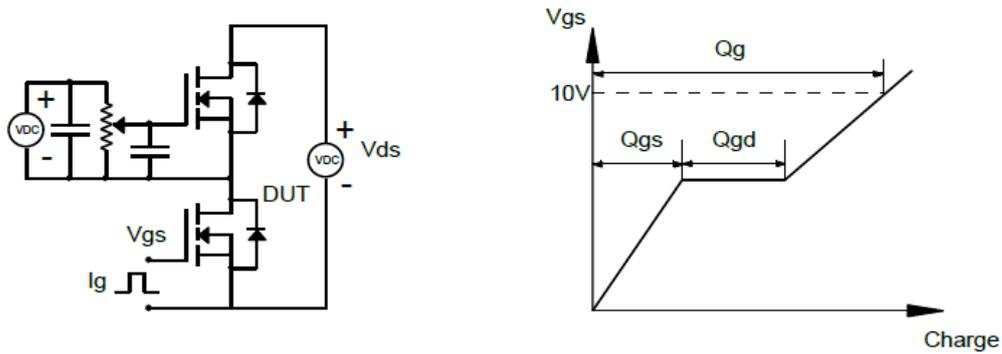


Figure1: Gate Charge Test Circuit & Waveforms

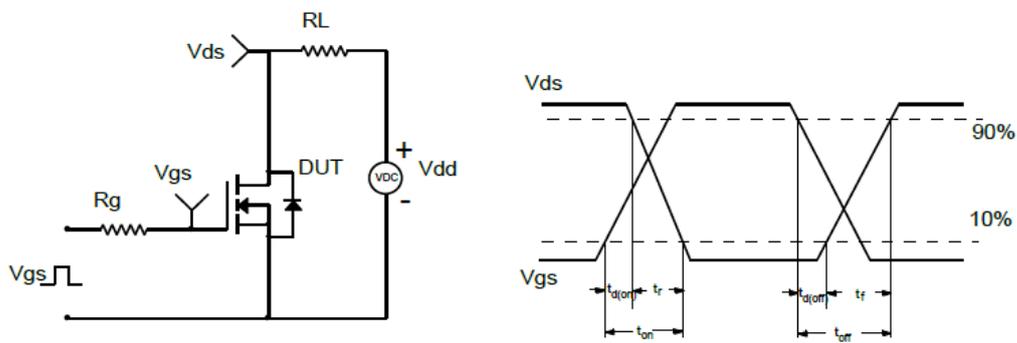


Figure2: Resistive Switching Test Circuit & Waveforms

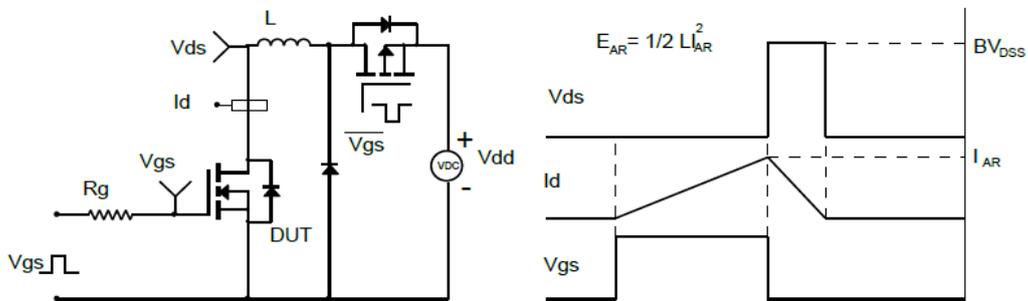


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

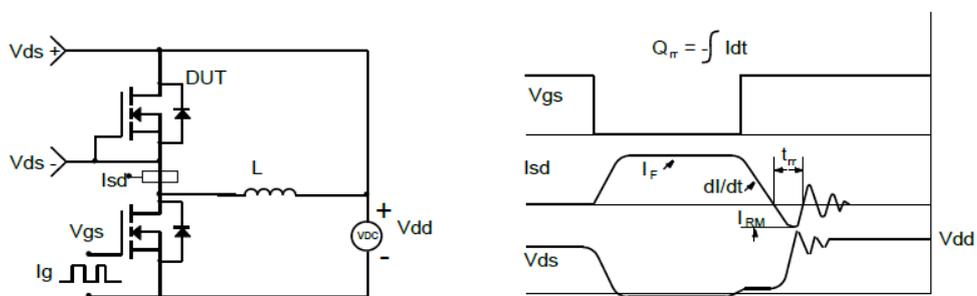
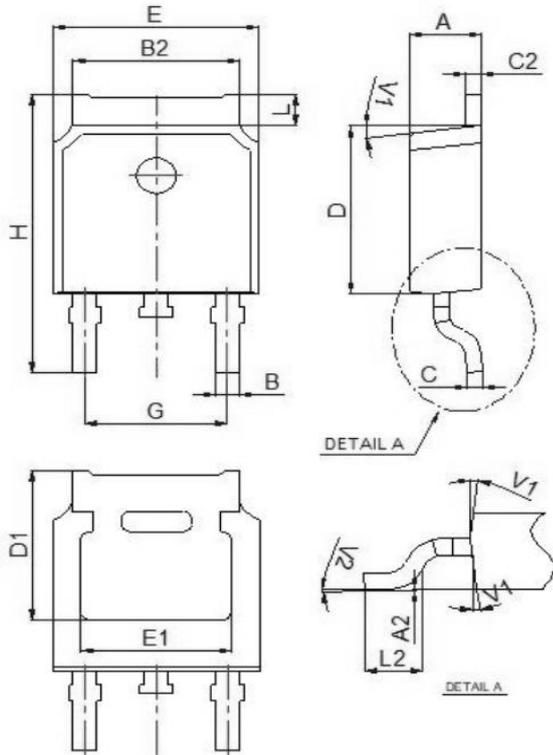


Figure4: Diode Recovery Test Circuit & Waveforms

TO-252 Package Information



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°