

SDM34AG10K

100V SGT N-Channel MOSFETs

Rev A.0

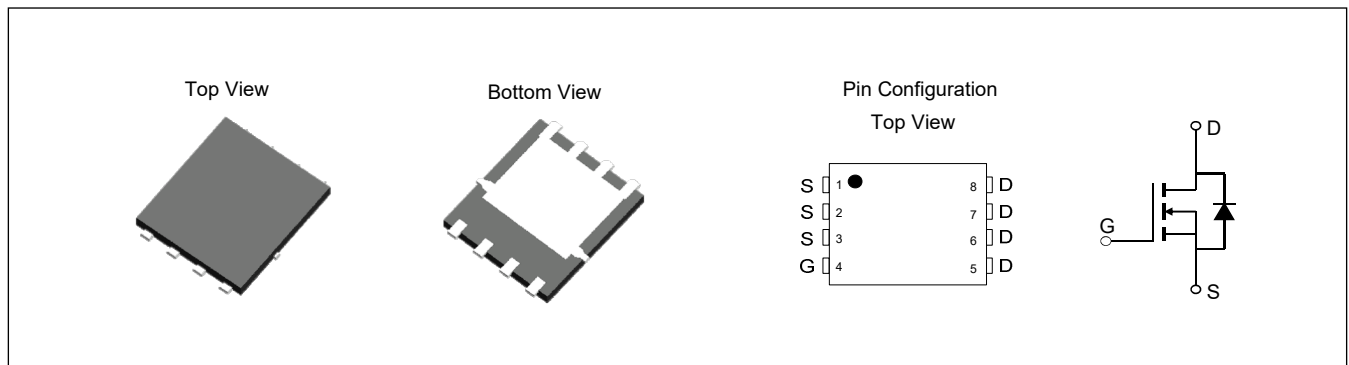
Feature

- ✧ Ultra-low $R_{DS(ON)}$
- ✧ Low Gate Charge
- ✧ High current Capability
- ✧ Enhanced body diode performance.
- ✧ Green product (RoHS compliant), lead free
- ✧ 100% UIS Tested, 100% Rg Tested

Product Summary

V_{DS}	100	V
$V_{GS(th)_{Typ}}$	1.6	V
$R_{DS(ON)_{Typ}}$ (at $V_{GS} = 10V$)	2.8	m Ω
I_D (at $V_{GS} = 10V$) ⁽¹⁾	135	A

Type	Package	Marking	Outline	Media	Quantity (pcs)
SDM34AG10K	PDFN5x6-8L	M34AG10	Tape	13" Reel	5000



Absolute Maximum Ratings (Rating at $T_J = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ⁽¹⁾	$T_C = 25^\circ C$	I_D	135	A
	$T_C = 100^\circ C$		85	
Pulsed Drain Current ⁽²⁾		I_{DM}	483	A
Continuous Drain Current ⁽⁶⁾	$T_C = 25^\circ C$	I_D	100	A
Avalanche Current ⁽³⁾		I_{AS}	72	A
Avalanche Energy ⁽³⁾		E_{AS}	259	mJ
Power Dissipation ⁽⁴⁾	$T_C = 25^\circ C$	P_D	114	W
	$T_C = 100^\circ C$		45	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ C$

Electrical Characteristics (Rating at $T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$	-	-	1	μA
			-	-	5	
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.2	1.6	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	-	2.8	3.4	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=15\text{A}$	-	3.4	4.3	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$	-	109	-	S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$	-	0.7	1.0	V
I_S	Maximum Body-Diode Continuous Current		-	-	114	A
DYNAMIC PARAMETERS ⁽⁵⁾						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=50\text{V}$, $f=1\text{MHz}$	-	4647	-	pF
C_{oss}	Output Capacitance		-	1215	-	pF
C_{rss}	Reverse Transfer Capacitance		-	5.9	-	pF
R_g	Gate Resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	-	2.5	-	Ω
SWITCHING PARAMETERS ⁽⁵⁾						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=0\sim 10\text{V}$, $V_{DS}=50\text{V}$, $I_D=20\text{A}$	-	79	-	nC
$Q_g(4.5\text{V})$	Total Gate Charge		-	57	-	nC
Q_{gs}	Gate Source Charge		-	11.3	-	nC
Q_{gd}	Gate Drain Charge		-	27	-	nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $R_L=2.5\Omega$, $R_{GEN}=6\Omega$	-	10.1	-	ns
t_r	Turn-On Rise Time		-	23	-	ns
$t_{D(off)}$	Turn-Off Delay Time		-	85	-	ns
t_f	Turn-Off Fall Time		-	63	-	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	85	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	217	-	nC

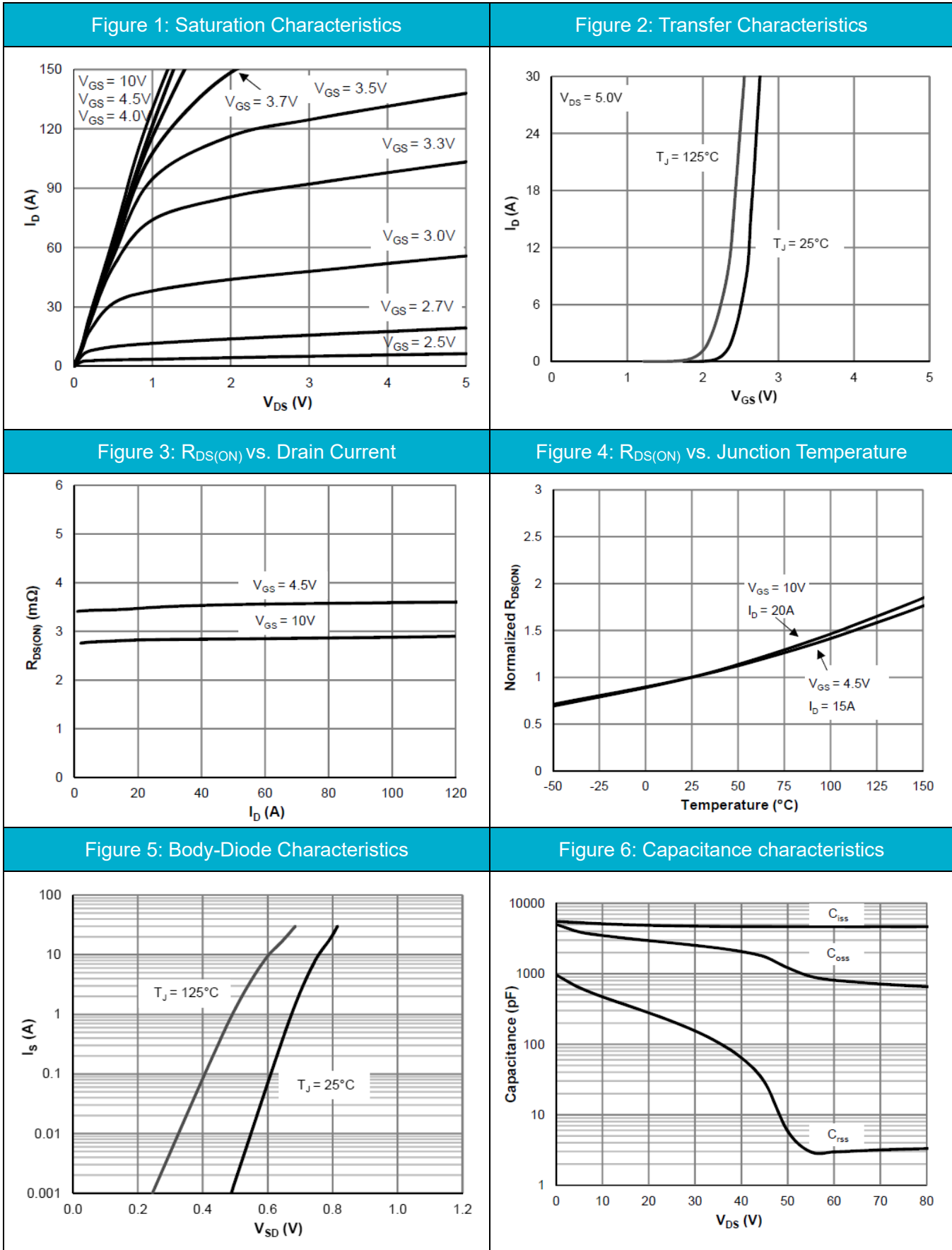
Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal resistance from junction to case	0.8	1.1	$^{\circ}\text{C} / \text{W}$
$R_{\theta JA}$	Thermal resistance from junction to ambient	48	58	$^{\circ}\text{C} / \text{W}$

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under $T_{J_Max}=150^{\circ}\text{C}$.
3. This single-pulse measurement was taken under the following condition [$L=100\mu\text{H}$, $V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$] while its value is limited by $T_{J_Max}=150^{\circ}\text{C}$.
4. The power dissipation P_D is based on $T_{J_Max}=150^{\circ}\text{C}$.
5. This value is guaranteed by design hence it is not included in the production test.
6. Continuous current rating is limited by the package used.

Typical Electrical and Thermal Characteristics



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Figure 7: Current De-rating **Figure 8: Power De-rating**

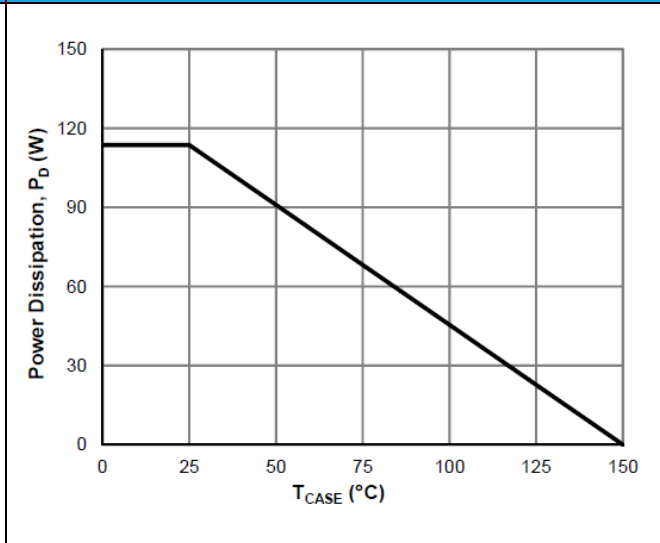
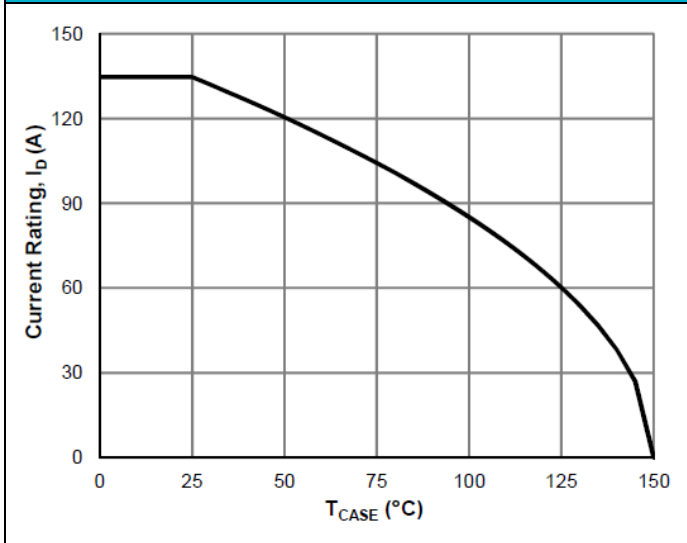


Figure 9: Maximum Safe Operating Area

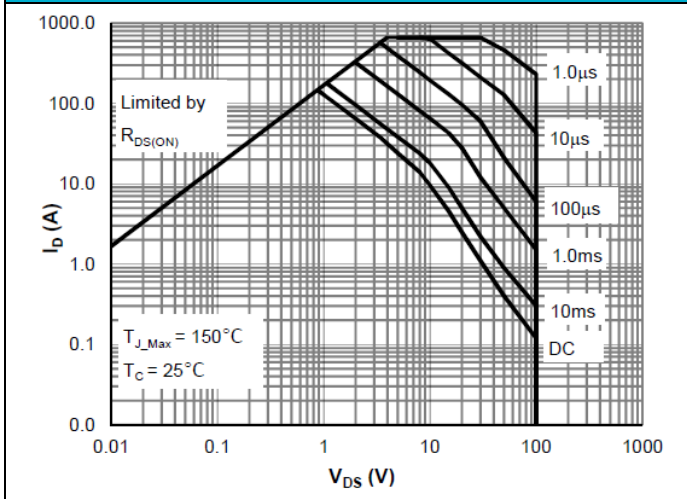


Figure 10: Single Pulse Power Rating, Junction-to-Case

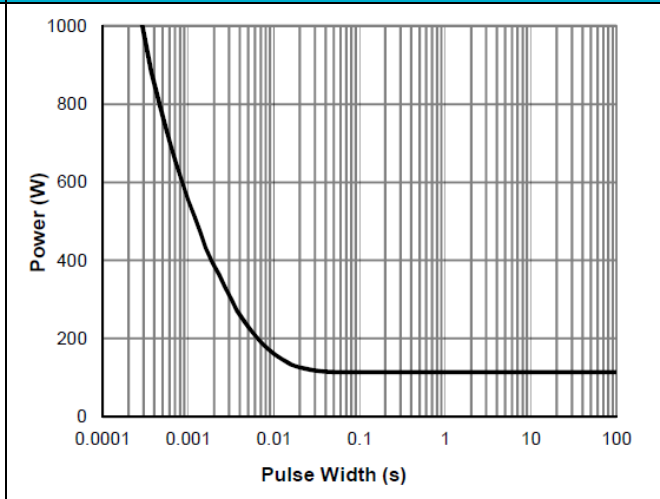
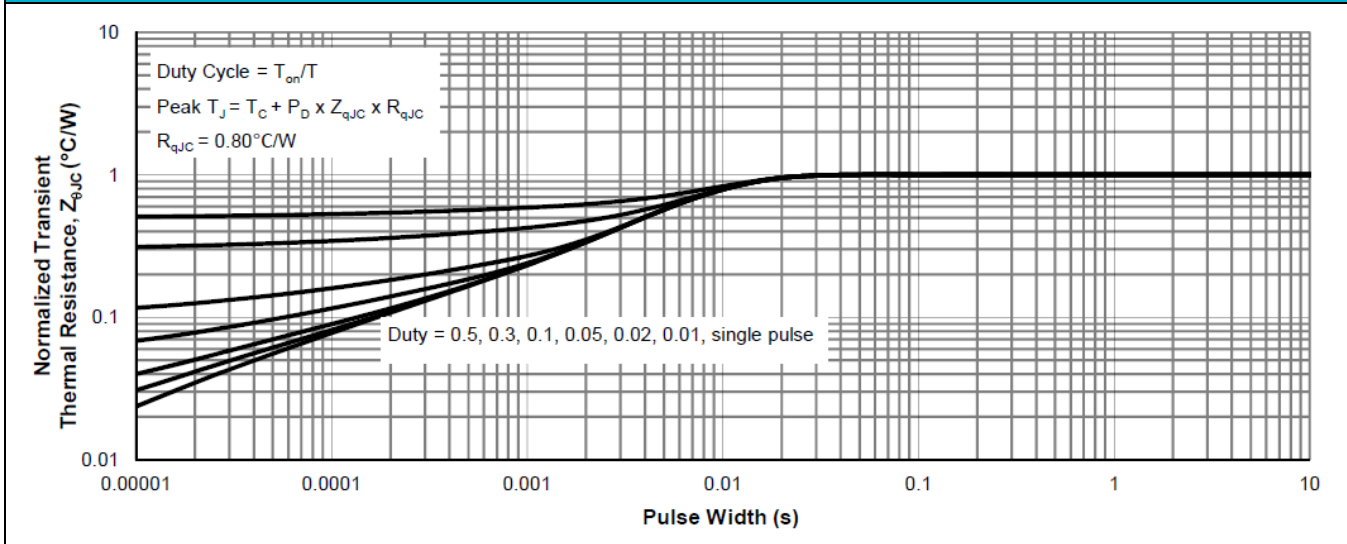


Figure 11: Normalized Maximum Transient Thermal Impedance



Test Circuit

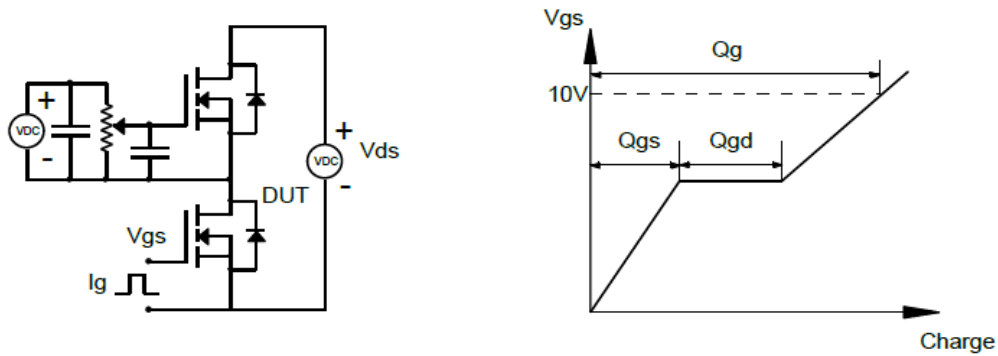


Figure1: Gate Charge Test Circuit & Waveforms

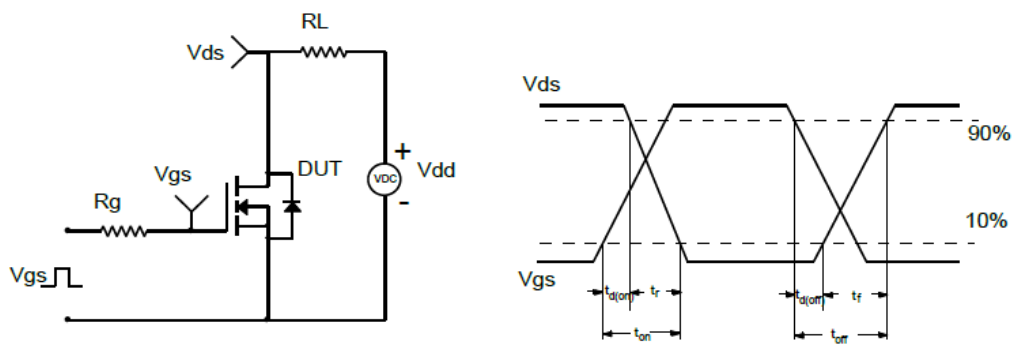


Figure2: Resistive Switching Test Circuit & Waveforms

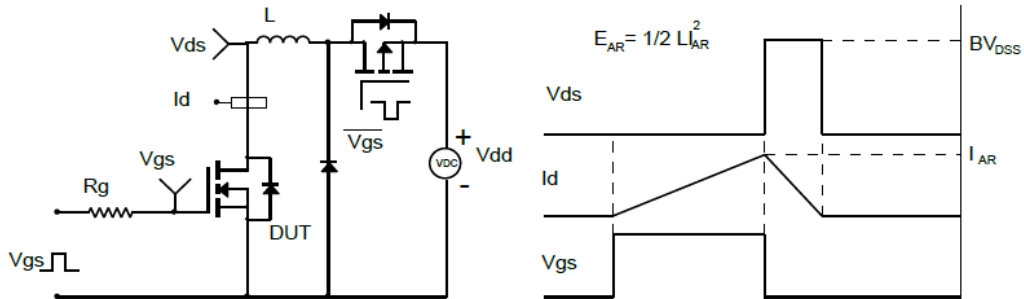


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

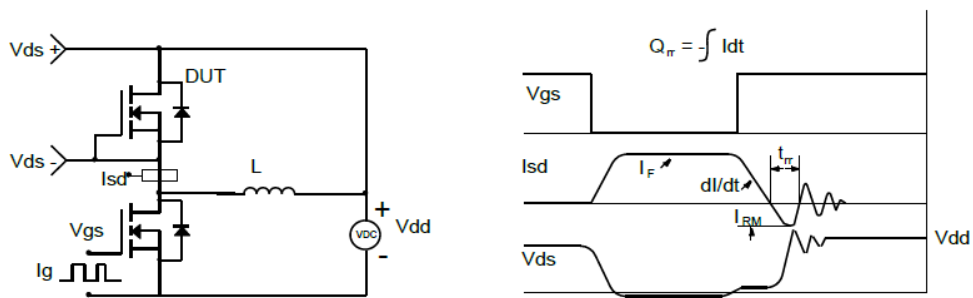
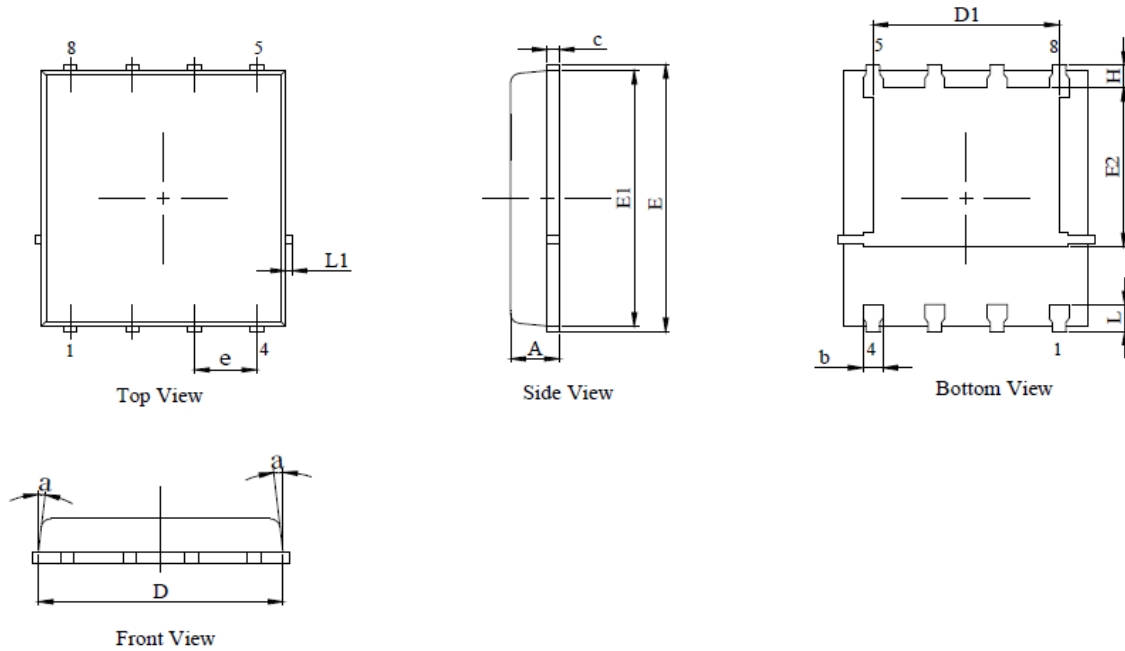


Figure4: Diode Recovery Test Circuit & Waveforms

PDFN5x6-8L Package Information

Package Outline

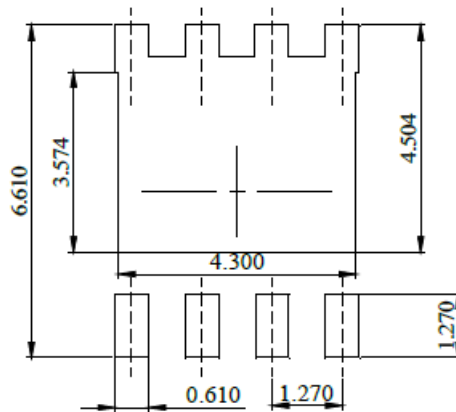


NOTES:

1. Dimension and tolerance per ASME Y14.5M, 1994.
2. All dimensions in millimeter (angle in degree).
3. Dimensions D and E1 do not include mold flash protrusions or gate burrs.

DIM.	MILLIMETER	
	MIN.	MAX.
A	0.90	1.20
b	0.33	0.51
c	0.23	0.33
D	4.80	5.40
D1	3.61	4.25
E	5.90	6.30
E1	5.55	5.95
E2	3.35	3.95
e	1.27 BSC	
H	0.41	0.80
L	0.51	0.80
L1	-	0.15
a	0°	12°

Recommend Footprint



DIMENSIONS: MILLIMETERS

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