SDM51AG04KV

40V SGT N-Channel MOSFETs

Rev A.0

Feature

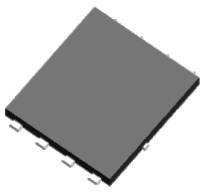
- Low $R_{DS(ON)}$
- Low Gate Charge
- High current Capability
- Green product (RoHS compliant), lead free
- 100% UIS Tested, 100% Rg Tested
- AEC- Q101 qualified

Product Summary

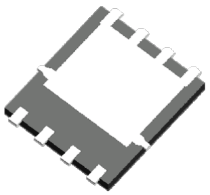
V_{DS}	40	V
$V_{GS(th)\_Typ}$	2.8	V
$R_{DS(ON)\_Typ}$ (at V_{GS} =10V)	4.1	mΩ
I_D (at V_{GS} =10V) (1)	86	A

Type	Package	Marking	Outline	Media	Quantity (pcs)
SDM51AG04KV	PDFN5X6-8L	M51AG04V	Tape	13” Reel	5000

Top View

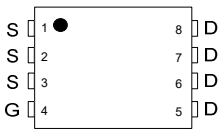


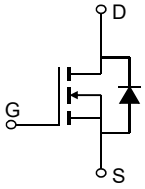
Bottom View



Pin Configuration

Top View





Absolute Maximum Ratings (Rating at T_J=25°C unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current(1)	T_C=25°C	I_D	86	A
	T_C=100°C		54	
Pulsed Drain Current (2)		I_{DM}	344	A
Maximum Body-Diode Continuous Current		I_S	63	A
Avalanche Energy (3)		E_{AS}	96	mJ
Power Dissipation (4)	T_C=25°C	P_D	63	W
	T_C=100°C		25	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (Rating at T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS} =0V	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS} =0V	-	-	1	μA
		T_J=55°C	-	-	5	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS} =±20V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	2.2	2.8	3.4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A	-	4.1	5.1	mΩ
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V	-	0.68	1.0	V
DYNAMIC PARAMETERS (5)						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz	-	1029	-	pF
C_{oss}	Output Capacitance		-	663	-	pF
C_{rss}	Reverse Transfer Capacitance		-	107	-	pF
R_g	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	2.5	-	Ω
SWITCHING PARAMETERS (5)						
Q_g(10V)	Total Gate Charge	V_{GS}=0 to 10V, V_{DS}=20V, I_D=20A	-	15.1	-	nC
Q_g(6V)	Total Gate Charge		-	9.7	-	nC
Q_{gs}	Gate Source Charge		-	5.1	-	nC
Q_{gd}	Gate Drain Charge		-	3.1	-	nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=20V, R_L=1Ω, R_{GEN}=6Ω	-	8.7	-	ns
t_r	Turn-On Rise Time		-	31	-	ns
$t_{D(off)}$	Turn-Off Delay Time		-	16.3	-	ns
t_f	Turn-Off Fall Time		-	6.9	-	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=100A/μs	-	25	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=100A/μs	-	9.7	-	nC

Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal resistance from junction to Ambient	58	67	°C /W
$R_{\theta JC}$	Thermal resistance from junction to Case	2	2.3	°C /W

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under T_{J_Max} = 150°C.
3. E_{AS} of 96 mJ is based on starting T_J = 25°C,L = 3.0mH, I_{AS} = 8.0A, V_{GS} = 10V, V_{DD} = 20V; 100% test at L = 0.1mH, I_{AS} = 27A.
4. The power dissipation P_D is based on T_{J_Max} = 150°C.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics

Figure 1: Saturation Characteristics

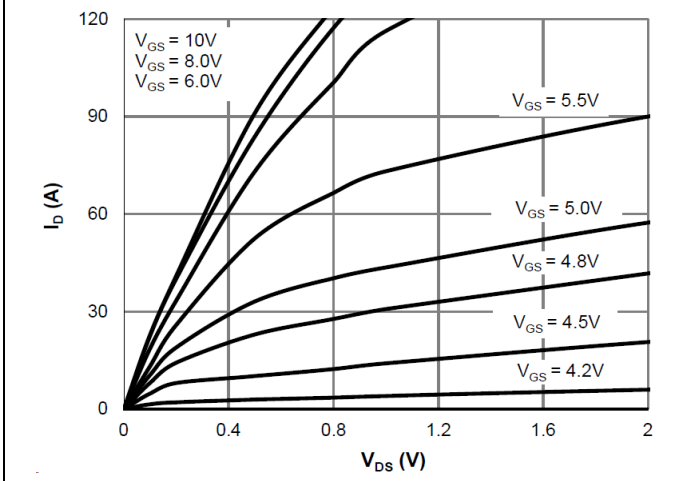


Figure 2: Transfer Characteristics

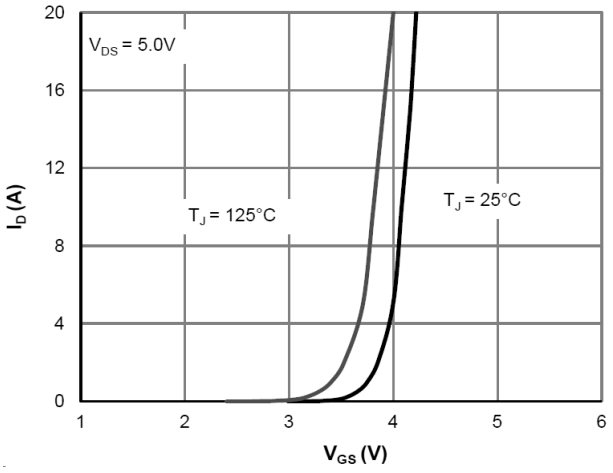


Figure 3: $R_{DS(ON)}$ vs. Drain Current

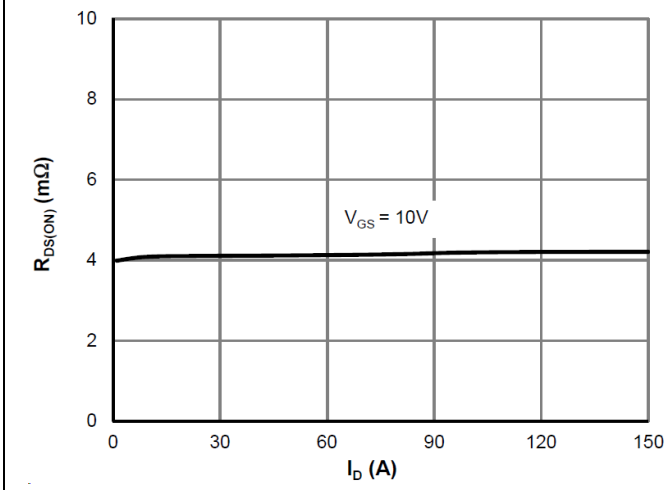


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

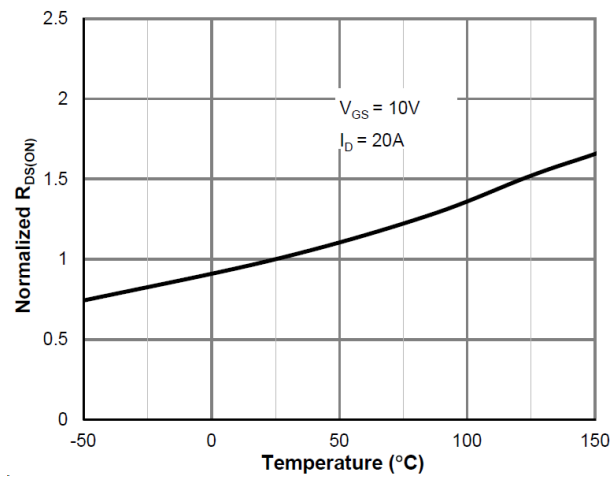


Figure 5: $R_{DS(ON)}$ vs. Gate-Source Voltage

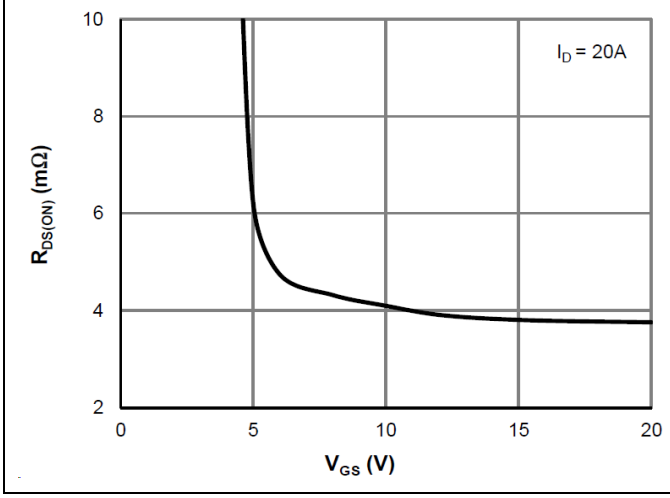
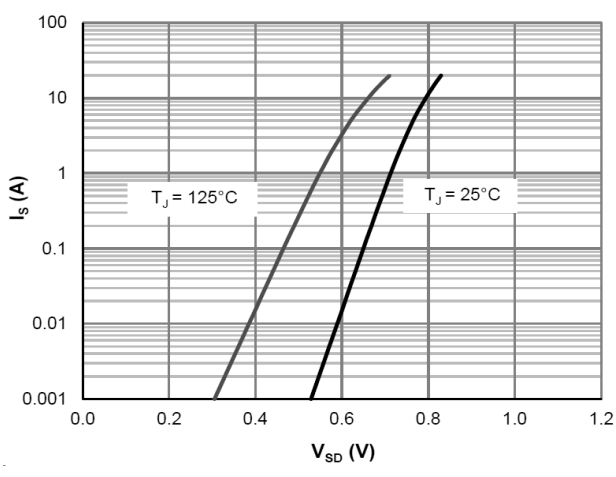


Figure 6: Body-Diode Characteristics



Typical Electrical and Thermal Characteristics

Figure 7: Gate-Charge characteristics

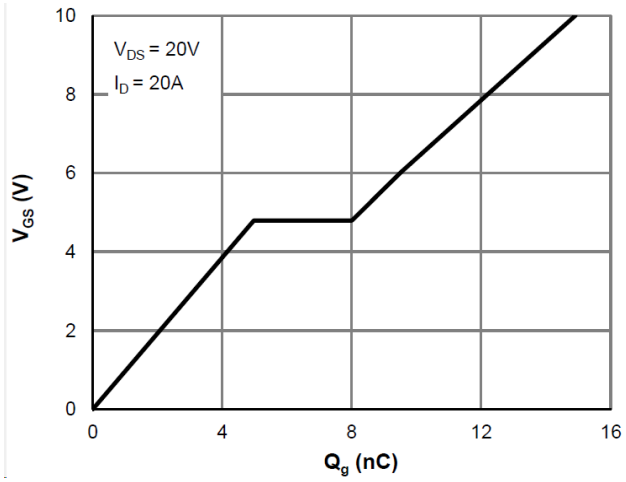


Figure 8: Capacitance characteristics

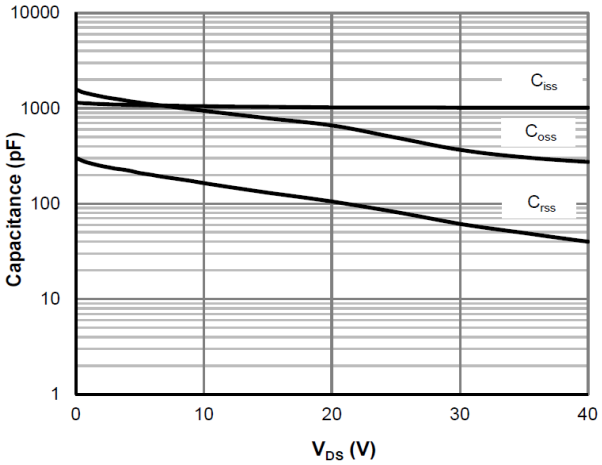


Figure 9: Current De-rating

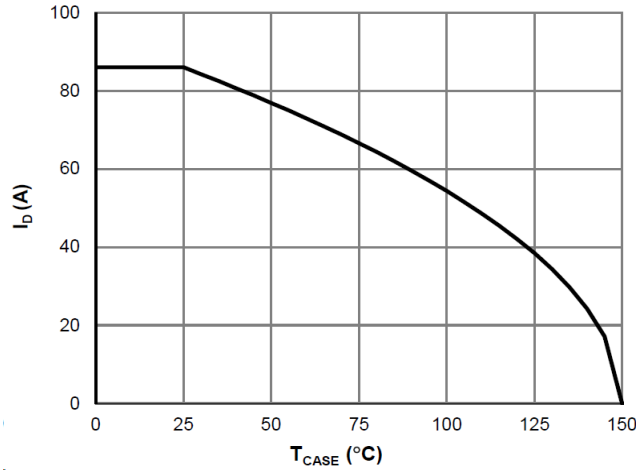


Figure 10: Power De-rating

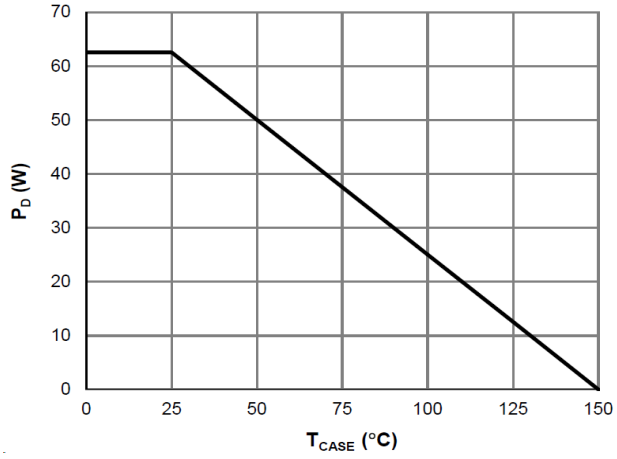


Figure 11: Maximum Safe Operating Area

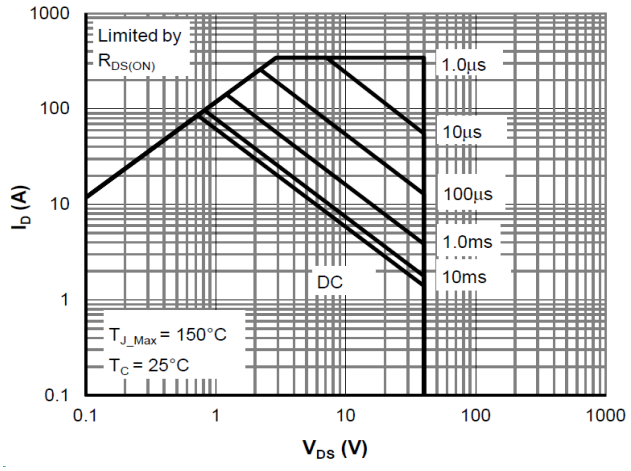
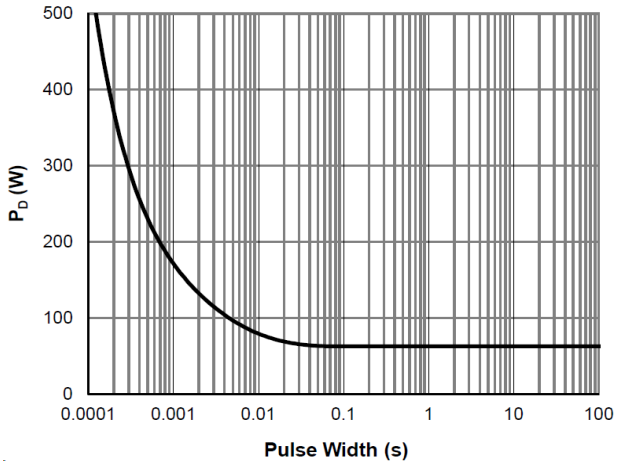
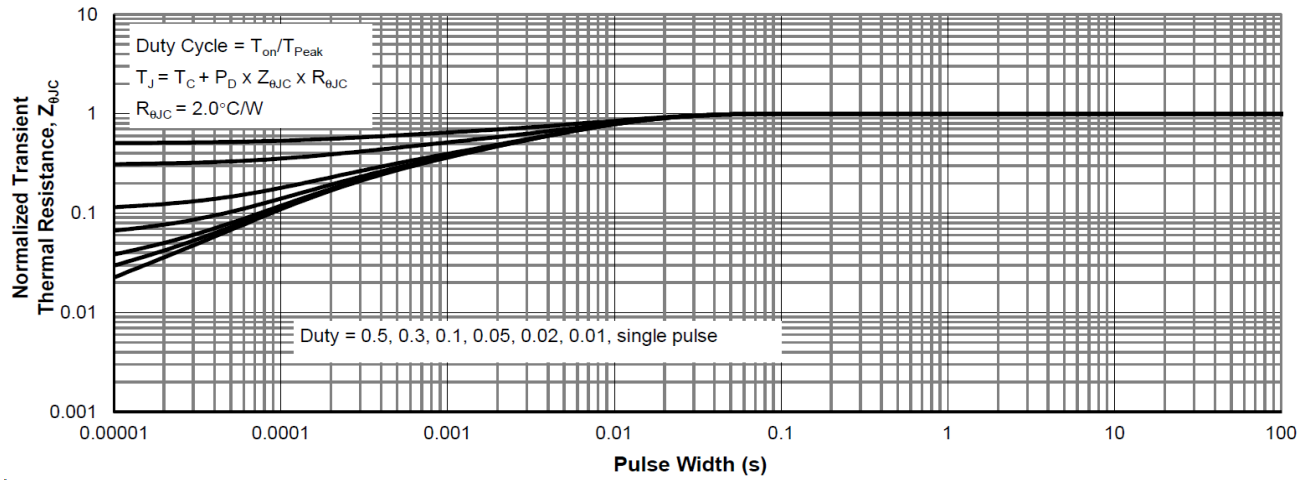


Figure 12: Single Pulse Power Rating, Junction-to-Case



Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance



Test Circuit

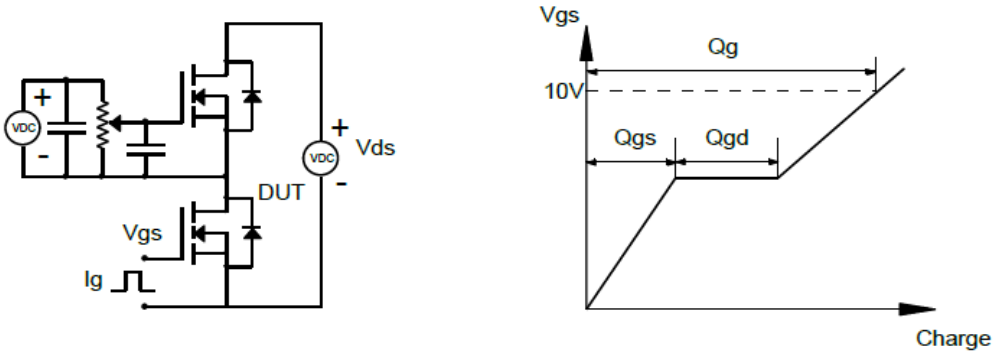


Figure1: Gate Charge Test Circuit & Waveforms

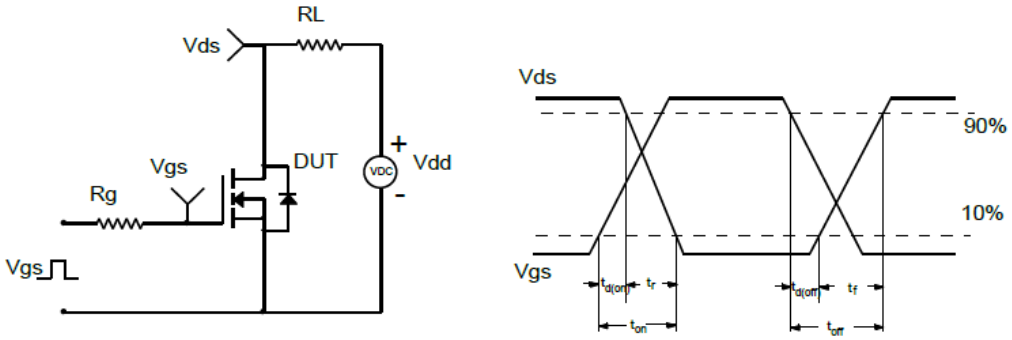


Figure2: Resistive Switching Test Circuit & Waveforms

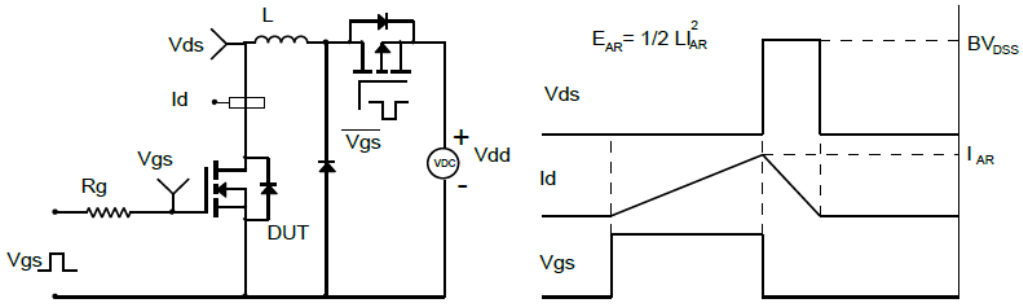


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

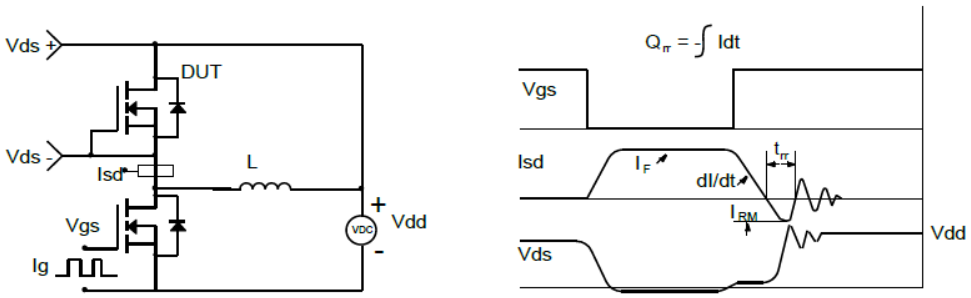
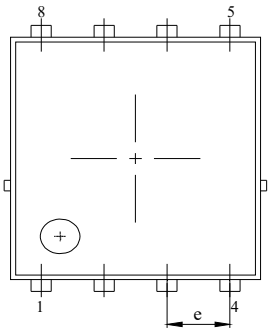
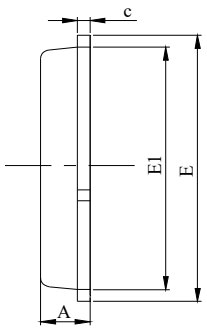


Figure4: Diode Recovery Test Circuit & Waveforms

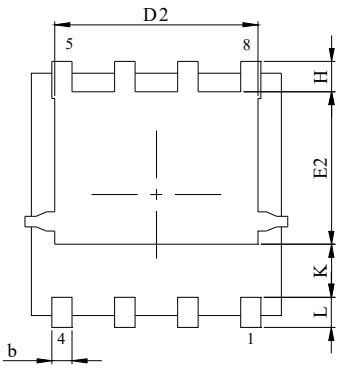
PDFN5x6-8L Package Information



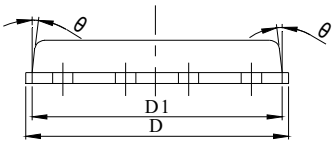
Top View



Side View



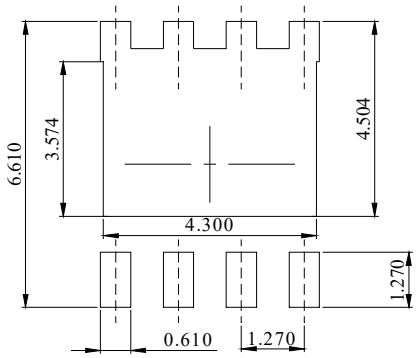
Bottom View



Front View

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.31	0.41	0.51
c	0.20	0.25	0.30
D	5.00	5.20	5.40
D1	4.95	5.05	5.15
D2	4.00	4.10	4.20
E	6.05	6.15	6.25
E1	5.50	5.60	5.70
E2	3.42	3.53	3.63
e		1.27BSC	
H	0.60	0.70	0.80
L	0.50	0.70	0.80
K		1.23 REF	
θ	-	-	10°

Recommended Soldering Footprint



DIMENSIONS:MILLIMETERS