

SDM56AG04LV

40V SGT N-Channel MOSFETs

Rev B.0

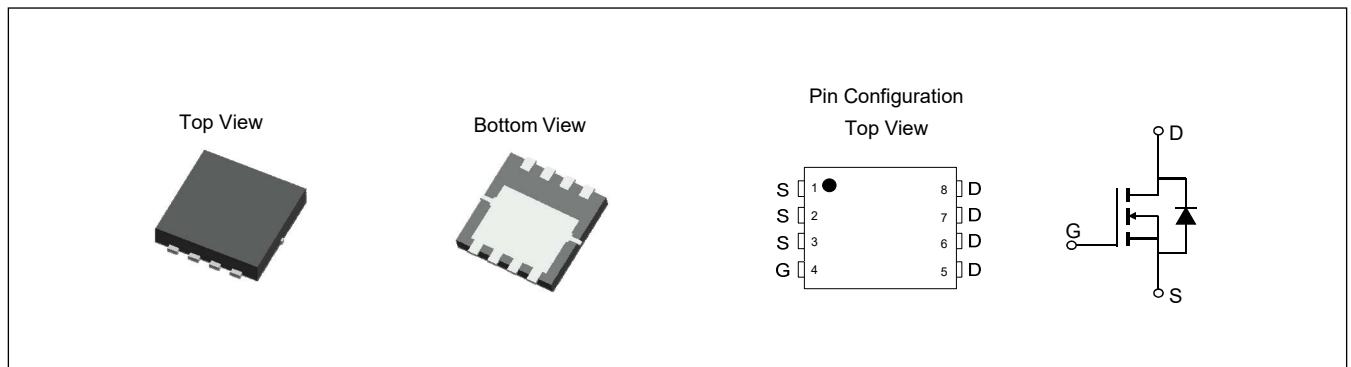
Feature

- ✧ Ultra-low $R_{DS(ON)}$
- ✧ Low Gate Charge
- ✧ High current Capability
- ✧ Enhanced body diode performance.
- ✧ Green product (RoHS compliant); 100% lead free
- ✧ 100% UIS Tested, 100% Rg Tested
- ✧ AEC-Q101 qualified

Product Summary

V_{DS}	40	V
$R_{DS(ON)_{Typ}}$ (at $V_{GS} = 10V$)	4.5	m Ω
$R_{DS(ON)_{Typ}}$ (at $V_{GS} = 4.5V$)	5.9	m Ω
I_D (at $V_{GS} = 10V$) ⁽¹⁾	55	A

Type	Package	Marking	Outline	Media	Quantity (pcs)
SDM56AG04LV	PDFN3.3x3.3-8L	SL0406A	Tape	13-inch Reel	5000



Absolute Maximum Ratings (Rating at $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ⁽¹⁾	I_D	$T_C=25^\circ C$	55
		$T_C=100^\circ C$	35
Pulsed Drain Current ⁽²⁾	I_{DM}	190	A
Avalanche Current ⁽³⁾	I_{AS}	27	A
Avalanche Energy ⁽³⁾	E_{AS}	36	mJ
Power Dissipation ⁽⁴⁾	P_D	$T_C=25^\circ C$	28
		$T_C=100^\circ C$	11.1
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Electrical Characteristics (Rating at $T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$T_J=55^\circ\text{C}$	-	-	5	
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.2	1.7	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	-	4.5	5.6	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=15\text{A}$	-	5.9	7.8	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$	-	74	-	S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$	-	0.69	1.0	V
I_S	Maximum Body-Diode Continuous Current		-	-	28	A
DYNAMIC PARAMETERS ⁽⁵⁾						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$	-	1203	-	pF
C_{oss}	Output Capacitance		-	535	-	pF
C_{rss}	Reverse Transfer Capacitance		-	51	-	pF
R_g	Gate Resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	-	1.8	-	Ω
SWITCHING PARAMETERS ⁽⁵⁾						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=0\sim 10\text{V}$, $V_{DS}=20\text{V}$, $I_D=20\text{A}$	-	17.5	-	nC
$Q_g(4.5\text{V})$	Total Gate Charge		-	9.3	-	nC
Q_{gs}	Gate Source Charge		-	3.1	-	nC
Q_{gd}	Gate Drain Charge		-	4.3	-	nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=1.0\Omega$, $R_{GEN}=6\Omega$	-	4.7	-	ns
t_r	Turn-On Rise Time		-	8.3	-	ns
$t_{D(off)}$	Turn-Off Delay Time		-	25	-	ns
t_f	Turn-Off Fall Time		-	15.3	-	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	51	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	41	-	nC

Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal resistance from junction to case	3.5	4.5	$^{\circ}\text{C} / \text{W}$
$R_{\theta JA}$	Thermal resistance from junction to ambient	55	70	$^{\circ}\text{C} / \text{W}$

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under $T_{J_Max}=150^{\circ}\text{C}$.
3. This single-pulse measurement was taken under the following condition [$L=100\mu\text{H}$, $V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$] while its value is limited by $T_{J_Max}=150^{\circ}\text{C}$.
4. The power dissipation P_D is based on $T_{J_Max}=150^{\circ}\text{C}$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics

Figure 1: Saturation Characteristics **Figure 2: Transfer Characteristics**

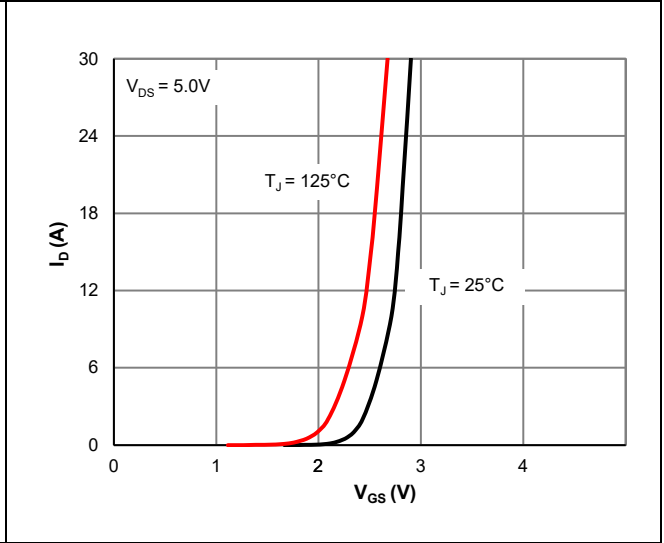
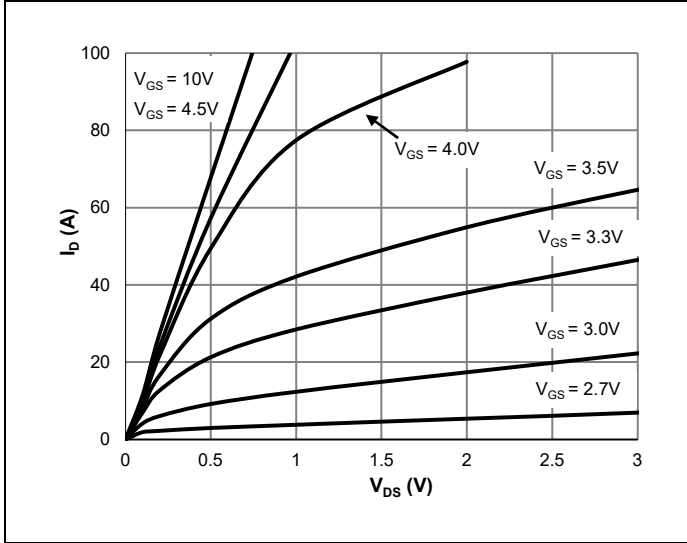


Figure 3: $R_{DS(ON)}$ vs. Drain Current

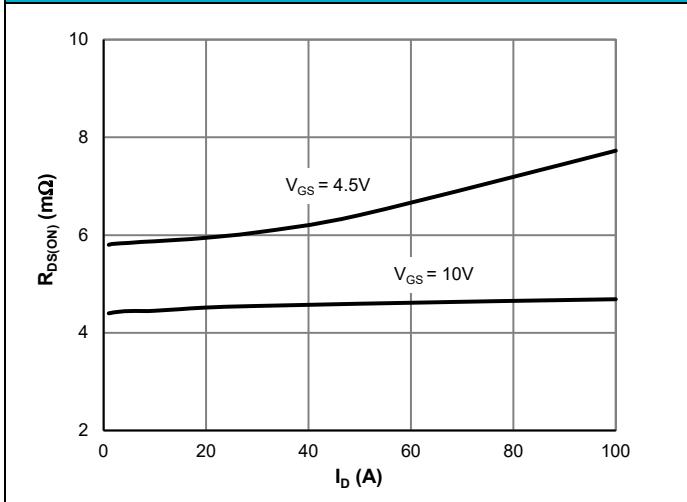


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

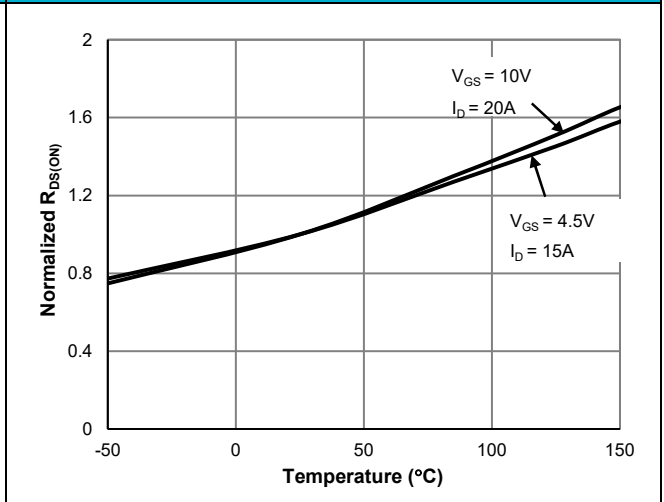


Figure 5: Body-Diode Characteristics

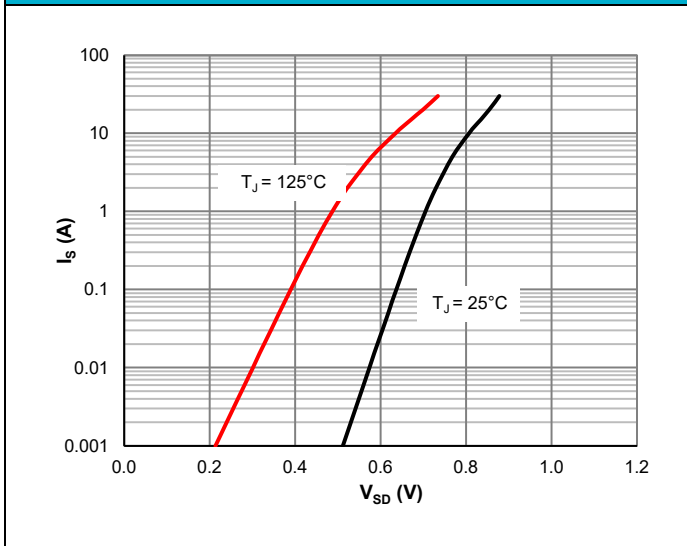
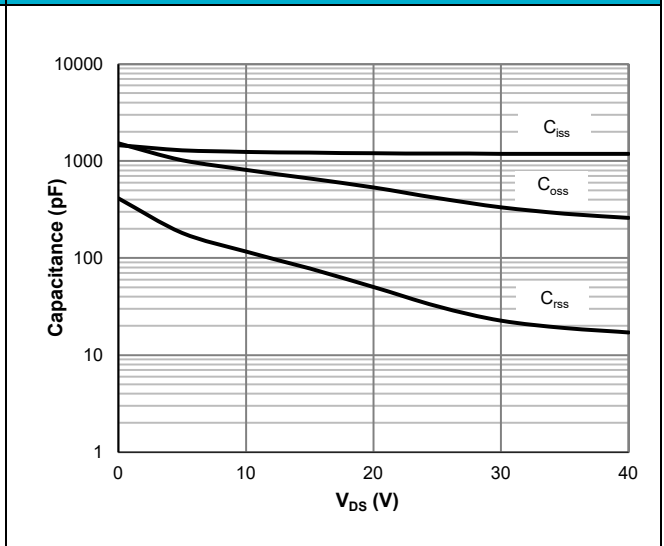


Figure 6: Capacitance characteristics



Typical Electrical and Thermal Characteristics

Figure 7: Current De-rating

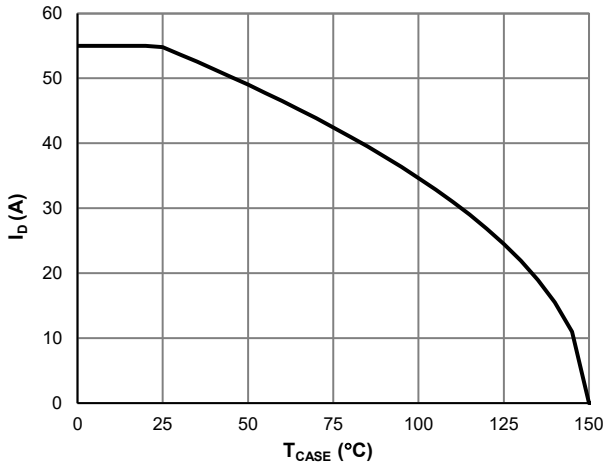


Figure 8: Power De-rating

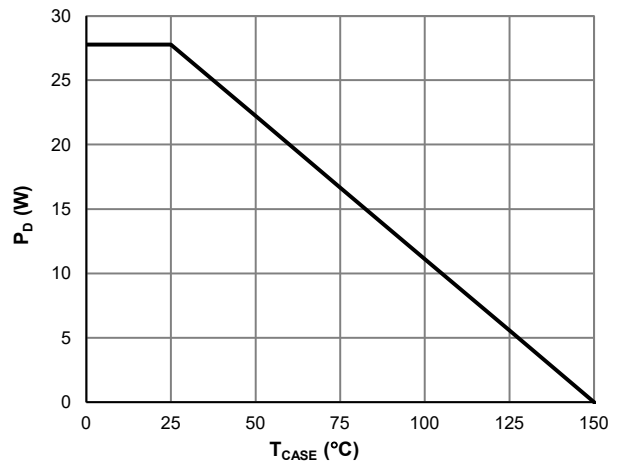


Figure 9: Maximum Safe Operating Area

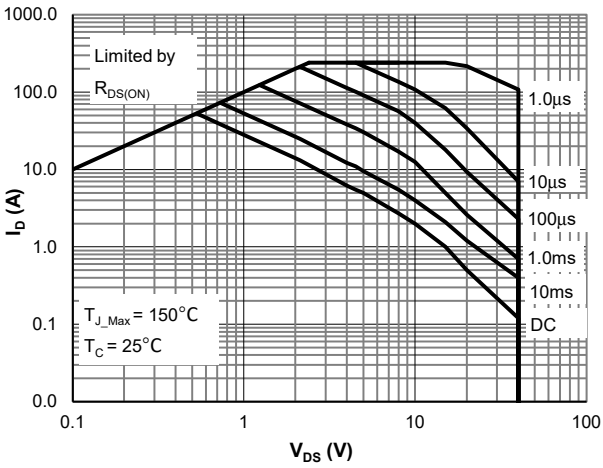


Figure 10: Single Pulse Power Rating, Junction-to-Case

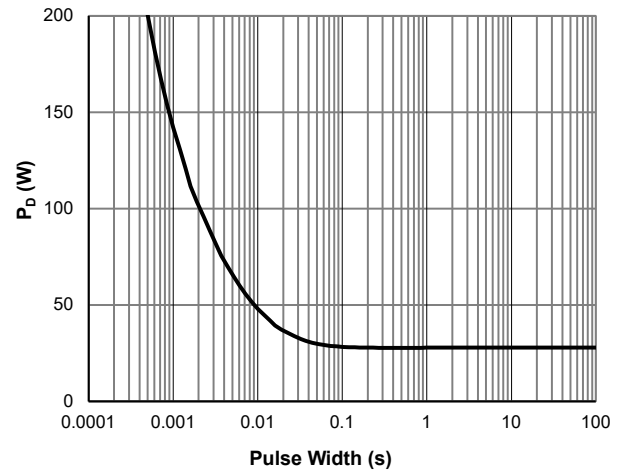


Figure 11: R_{DS(ON)} vs. Gate-Source Voltage

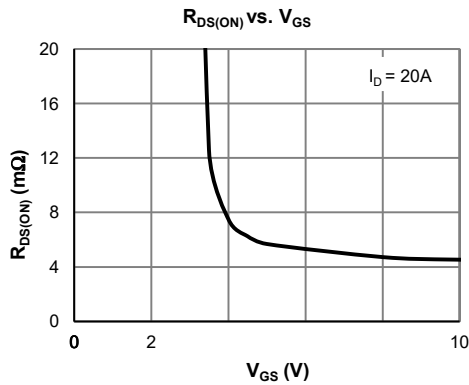
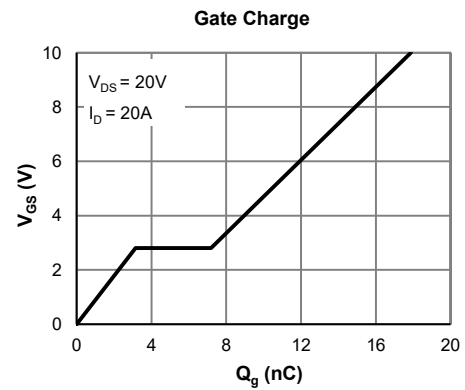
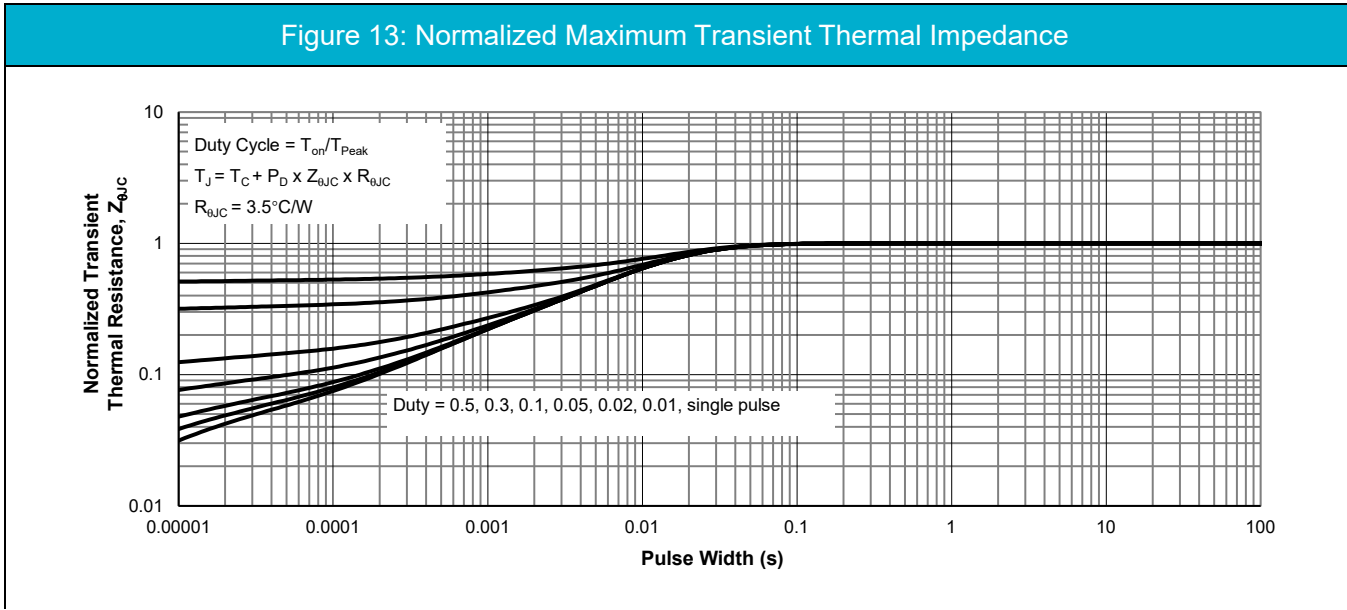


Figure 12: Gate-Charge characteristics



Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance



Test Circuit

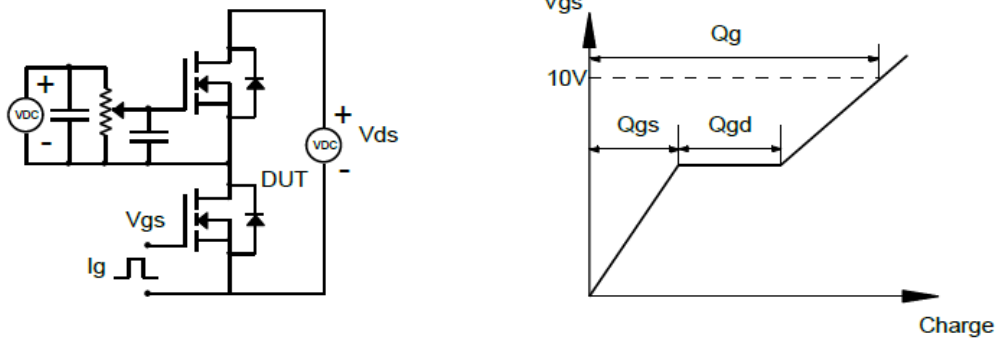


Figure1: Gate Charge Test Circuit & Waveforms

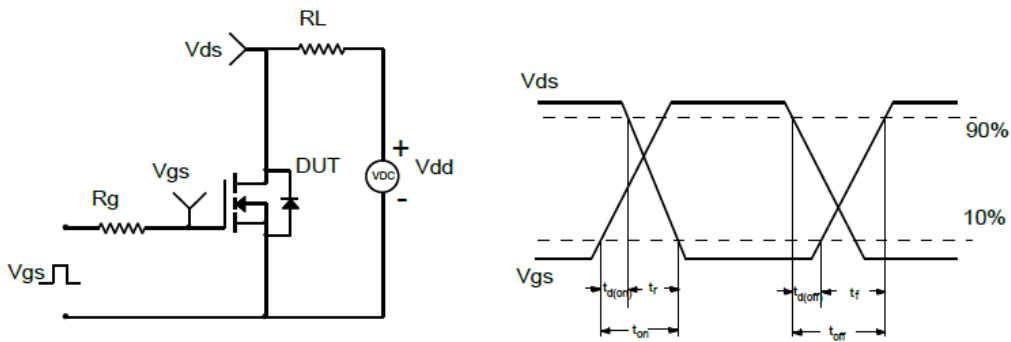


Figure2: Resistive Switching Test Circuit & Waveforms

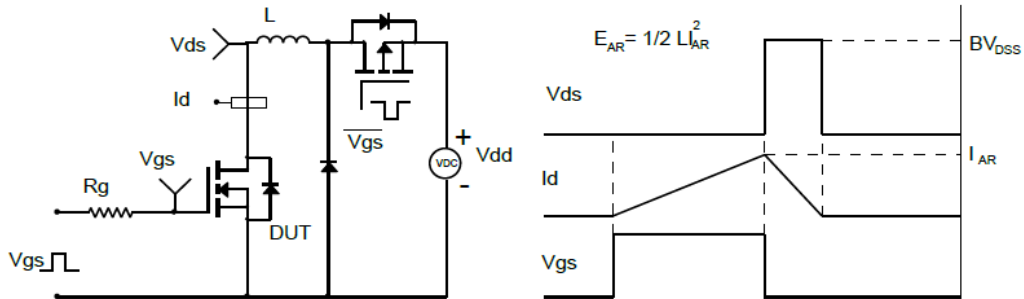


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

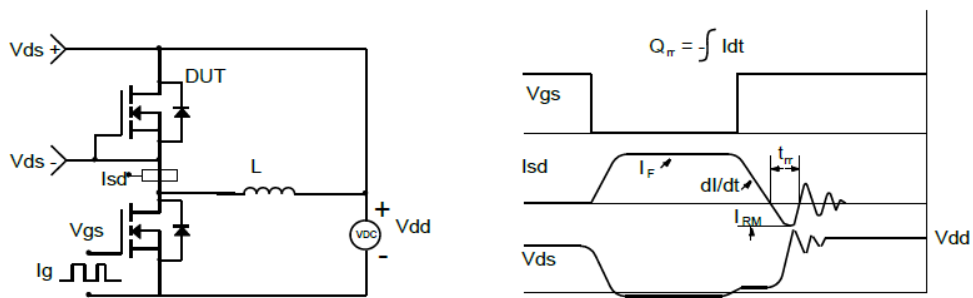
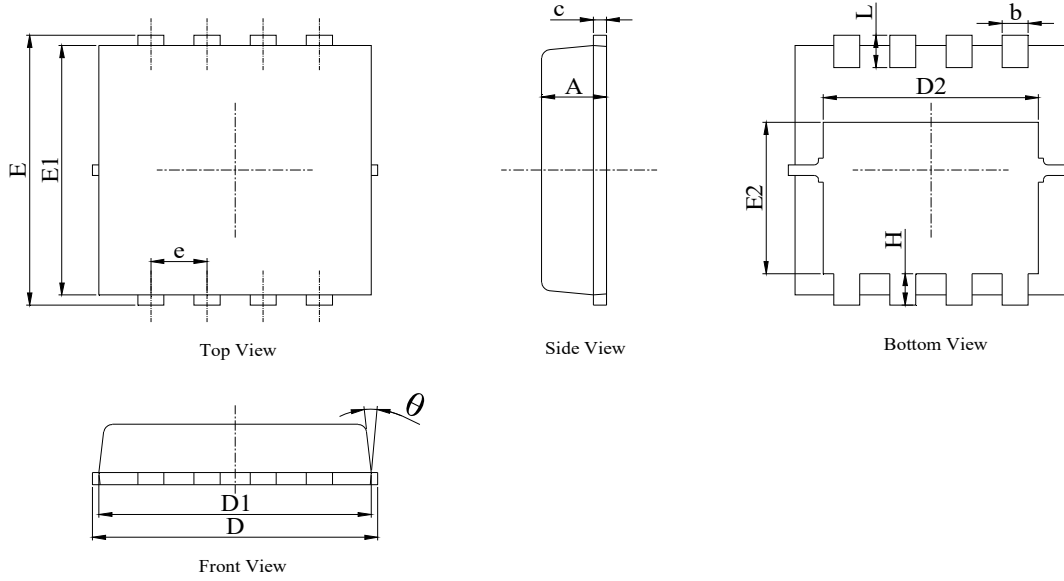


Figure4: Diode Recovery Test Circuit & Waveforms

PDFN3.3x3.3-8L Package Information

Package Outline

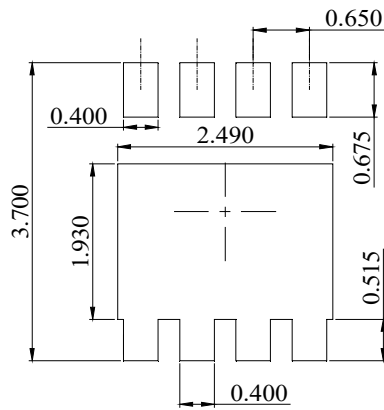


NOTES:

1. Dimension and tolerance per ASME Y14.5M, 1994.
2. All dimensions in millimeter (angle in degree).
3. Dimensions D1 and E1 do not include mold flash protrusions or gate burrs.

DIM.	MILLIMETER	
	MIN.	MAX.
A	0.70	0.85
b	0.25	0.35
c	0.10	0.25
D	3.15	3.40
D1	3.00	3.25
D2	2.25	2.59
E	3.20	3.45
E1	3.00	3.22
E2	1.48	1.98
e	0.65 BSC	
H	0.30	0.58
L	0.25	0.50
θ	---	15°

Recommend Footprint



DIMENSIONS: MILLIMETERS

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