

SE1003

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

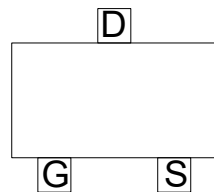
Features

For a single MOSFET

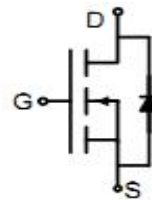
- $V_{DS} = 100V$
- $R_{DS(ON)} = 230m\Omega @ V_{GS}=10V$

Pin configurations

See Diagram below



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Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	Continuous	3	A
	Pulsed	20	
Total Power Dissipation	@ $T_A=25^\circ C$	1.5	W
Operating Junction Temperature Range	T_J	-55 to 175	$^\circ C$

Thermal Resistance

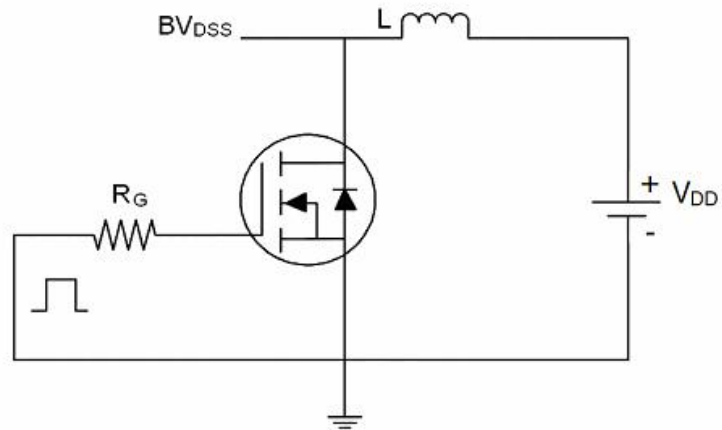
Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	-	100	$^\circ C/W$

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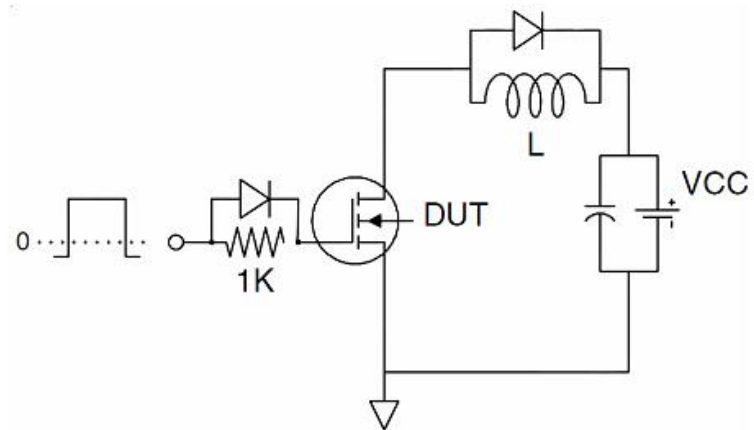
Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	100			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} =100V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	1.2	1.8	2.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =1A	-	230	250	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz		650		pF
C _{oss}	Output Capacitance			24		pF
C _{rss}	Reverse Transfer Capacitance			20		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =10V, V _{DS} =50V, I _D =3A		20		nC
Q _{gs}	Gate Source Charge			2.1		nC
Q _{gd}	Gate Drain Charge			3.3		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =50V, R _{GEN} =3Ω		6		ns
t _{d(off)}	Turn-Off Delay Time			20		ns
t _{d(r)}	Turn-On Rise Time			4		ns
t _{d(f)}	Turn-Off Fall Time			4		ns

Test Circuits and Waveform

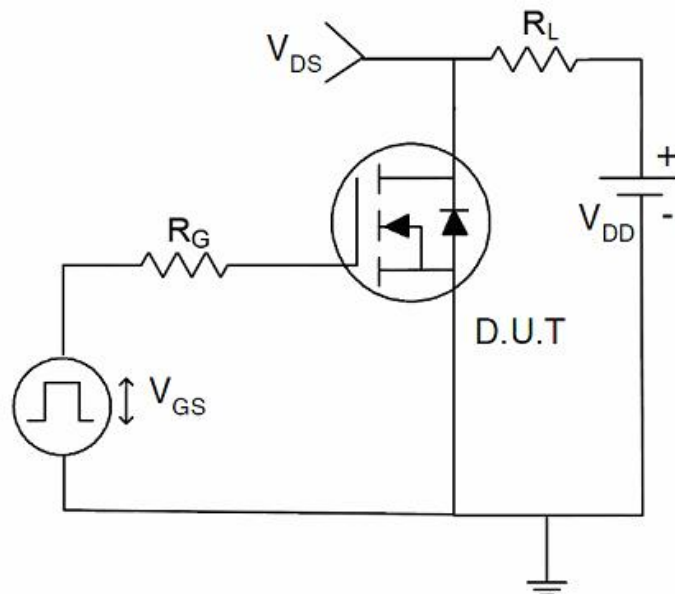
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Characteristics

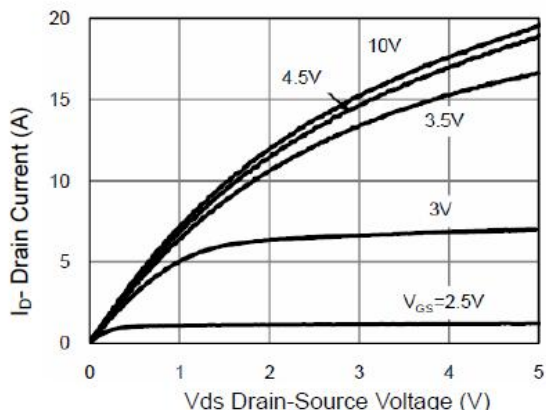


Figure 1 Output Characteristics

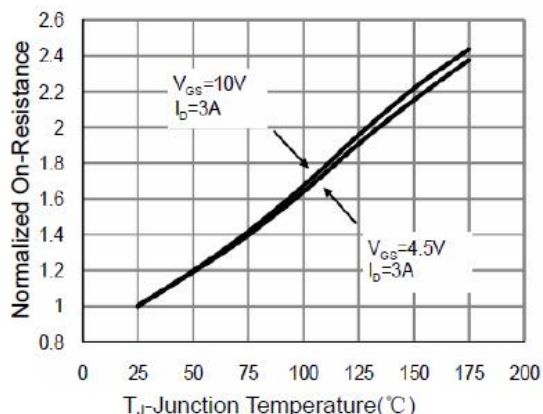


Figure 4 Rds(on)-Junction Temperature

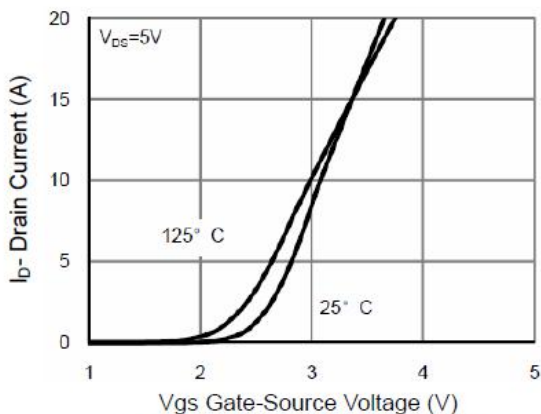


Figure 2 Transfer Characteristics

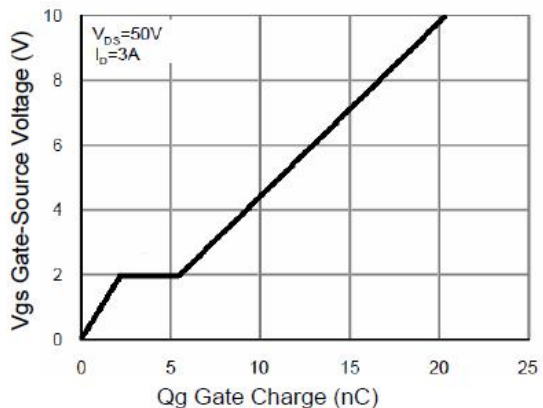


Figure 5 Gate Charge

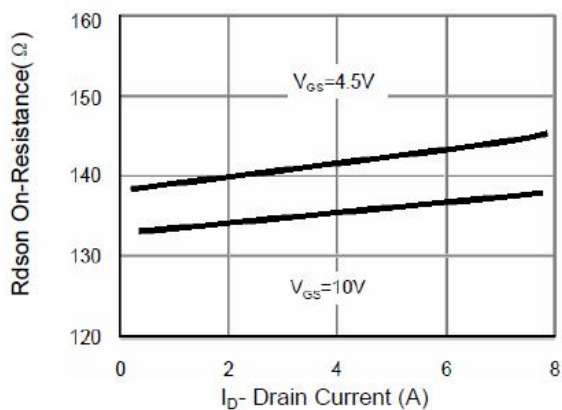


Figure 3 Rds(on)- Drain Current

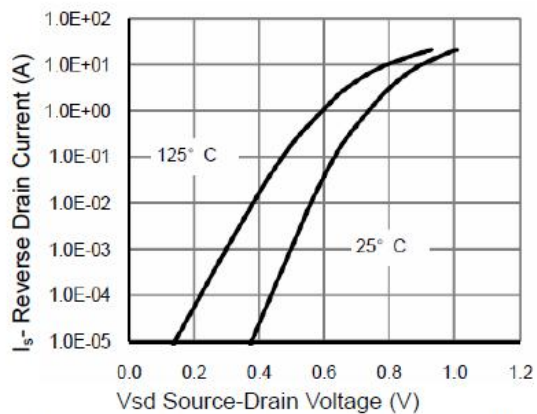


Figure 6 Source- Drain Diode Forward

Typical Characteristics

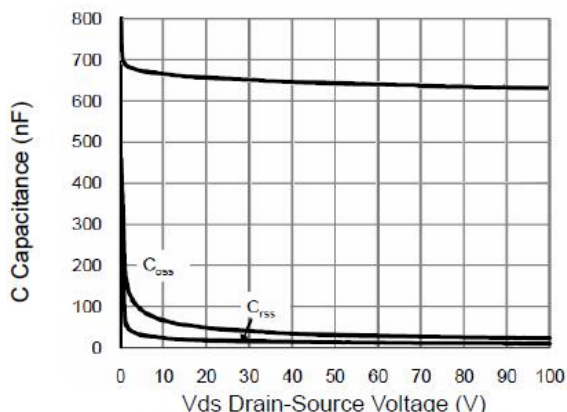


Figure 7 Capacitance vs Vds

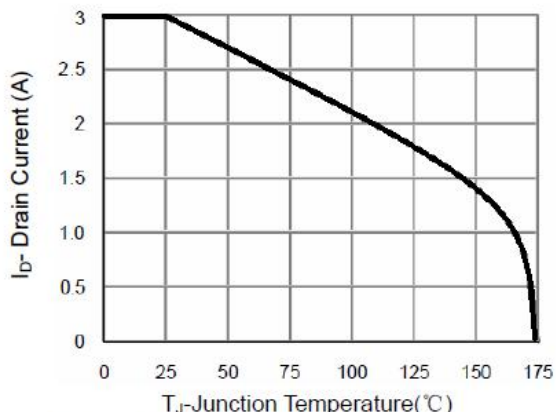


Figure 9 BV_{DSS} vs Junction Temperature

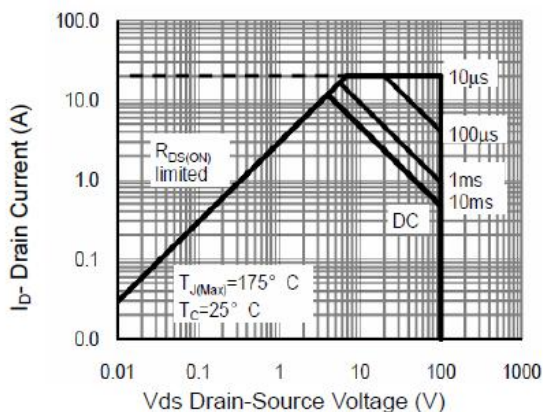


Figure 8 Safe Operation Area

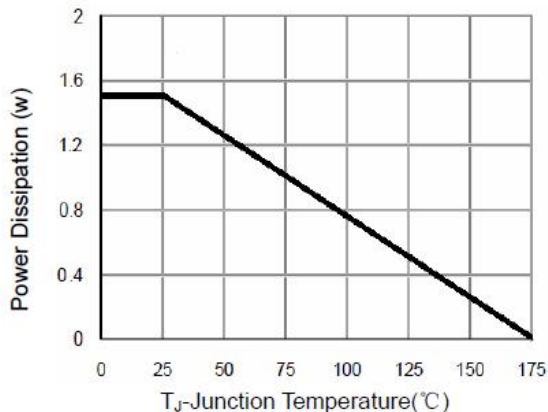


Figure 10 Power De-rating

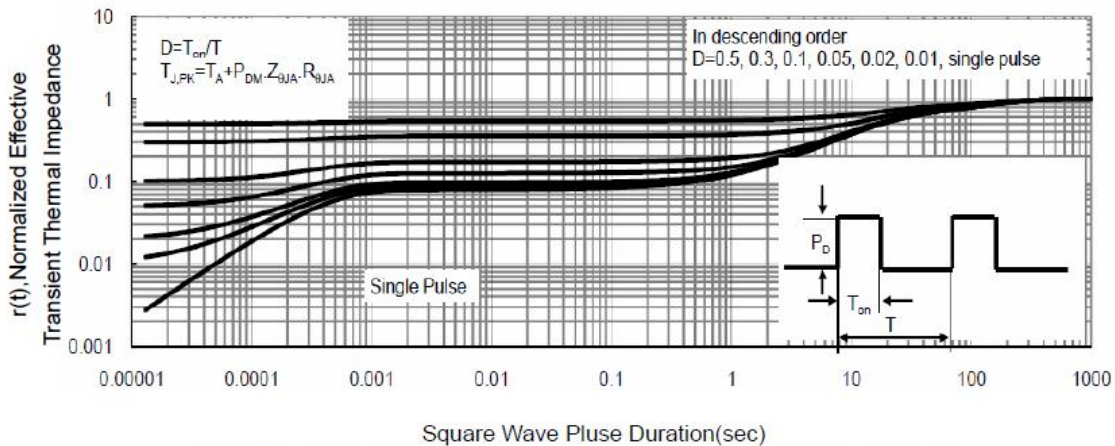
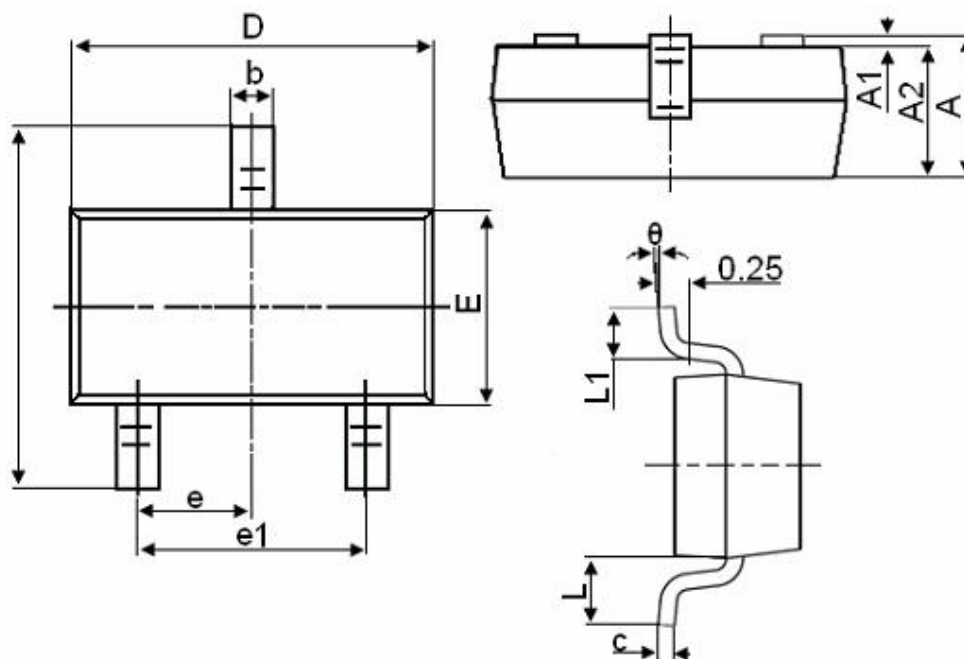


Figure 11 Normalized Maximum Transient Thermal Impedance

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Package Outline Dimension

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Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.

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