SHANGHAI SINO-IC
MICROELECTRONICS CO., LTD.

May 2015

SE20N110
N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
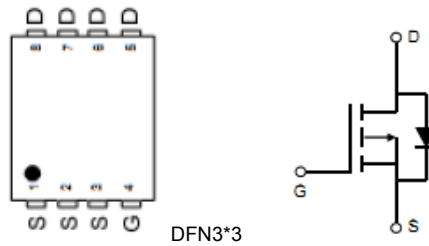- Small Package Outline
- Surface Mount Device

Features

For a single MOSFET

- V_{DS} = 20V
- $R_{DS(ON)}$ = 3.9mΩ @ V_{GS}=4.5V

Pin configurations

See Diagram below

DFN3*3

Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	110	A
	Pulsed		340	
Total Power Dissipation	@TA=25℃	P_D	90	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

SE20N110

Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0 V	20			V
I_{DSS}	Drain to Source Leakage Current	V_{DS}= 24V, V_{GS}=0V			1	µA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20 V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250µA	0.5	0.7	1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance [2]	V_{GS}=4.5V, I_D=20A	-	3.9	5.5	mΩ
		V_{GS}=2.5V, I_D=15A		6	9	
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		7032		pF
C_{oss}	Output Capacitance			898		pF
C_{rss}	Reverse Transfer Capacitance			743		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge [2]	V_{GS}=10V, V_{DS}=15V, I_D=30A		80		nC
Q_{gs}	Gate Source Charge			19		nC
Q_{gd}	Gate Drain Charge			38		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=15V, R_{GEN}=1Ω I_D=1A		20		ns
$t_{d(off)}$	Turn-Off Delay Time			80		ns
$t_{d(r)}$	Turn-On Rise Time			36		ns
$t_{d(f)}$	Turn-Off Fall Time			33		ns
Thermal Resistance						

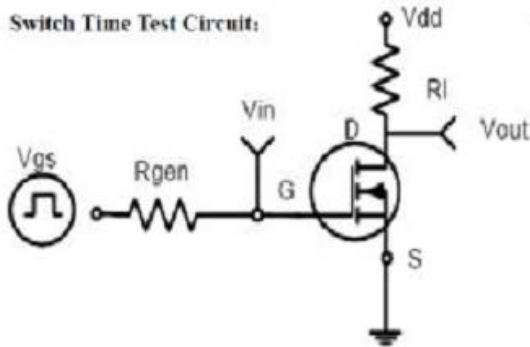| Symbol	Parameter	Typ	Max	Units
$R_{θJC}$	Junction to Case	-	2	℃/W
$R_{θJA}$	Junction to Ambient (t≦10s)	-	50	℃/W

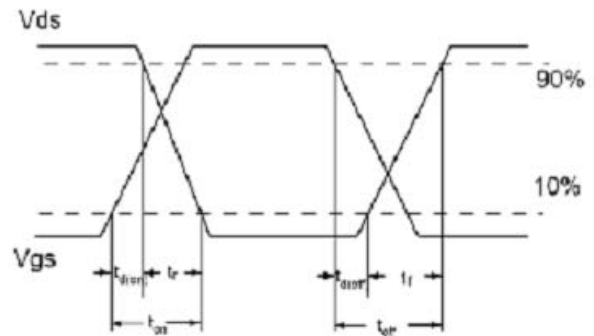## Test Circuits and Waveform

EAS test circuits:
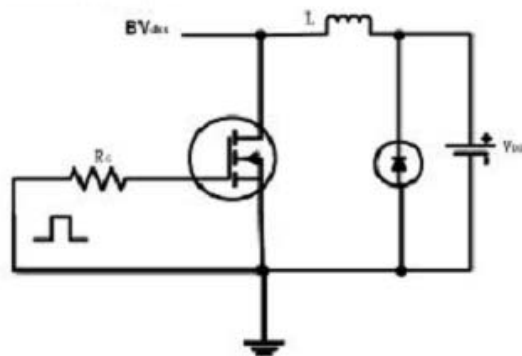
Gate charge test circuit:
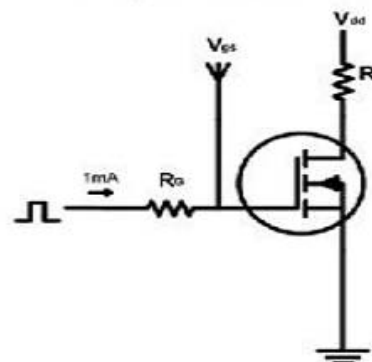
Switch Time Test Circuit:

Waveforms:
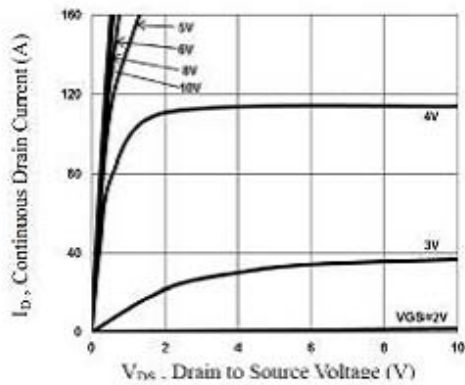
Typical Characteristics
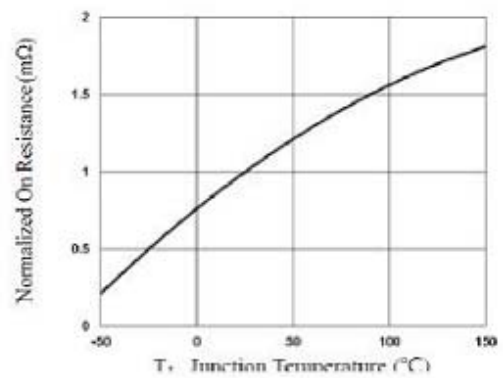

Figure 1: Typical Output Characteristics

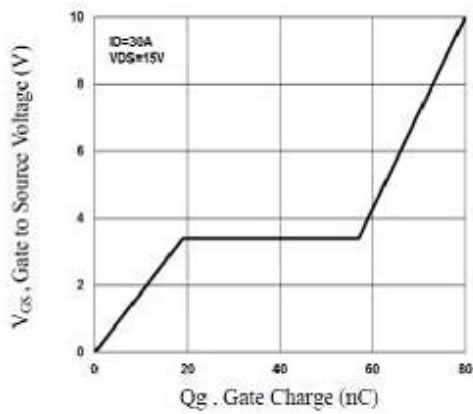Figure 2: Normalized RDSON vs. TJ
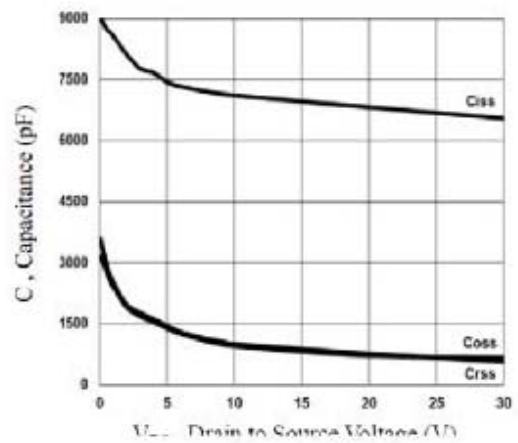

Figure 3: Gate-Charge Characteristics

Figure 4: Capacitance Characteristics

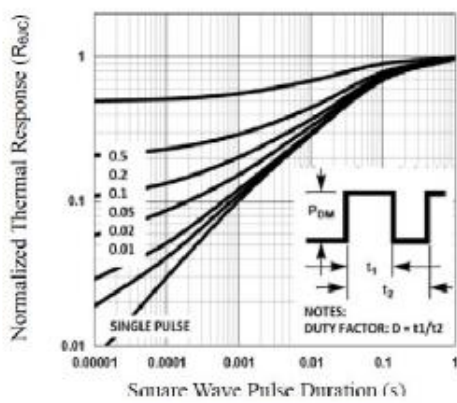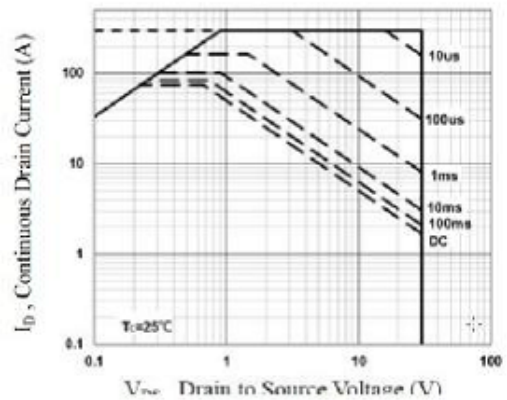

Figure 5: Normalized Thermal transient Impedance Curve

Figure 6: Maximum Safe Operation Area

Package Outline Dimension

DFN3 × 3
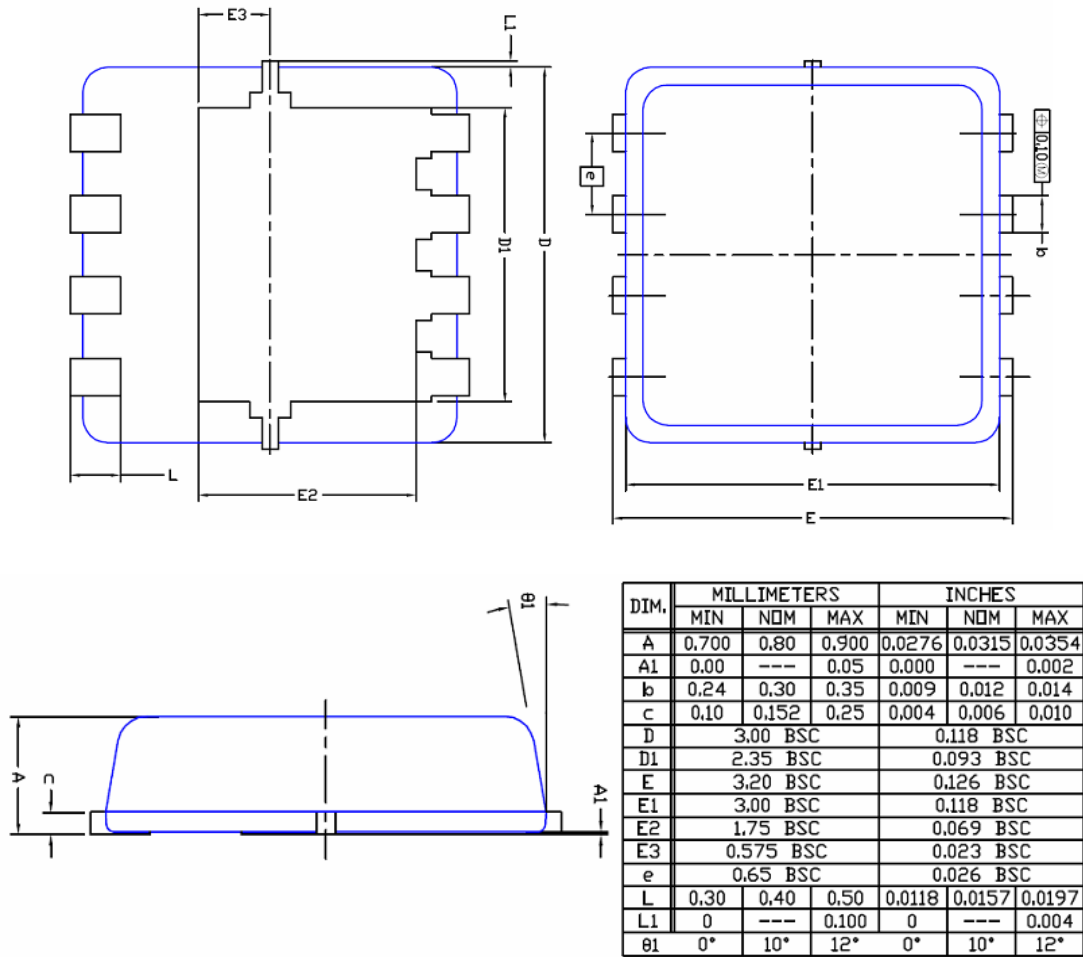
DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°

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