

SE30150A

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

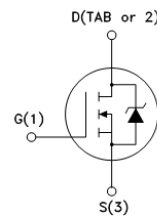
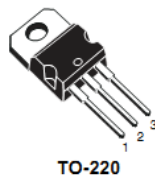
Features

For a single MOSFET

- $V_{DS} = 30V$
- $R_{DS(ON)} = 2.1m\Omega @ V_{GS}=10V$

Pin configurations

See Diagram below



Absolute Maximum Ratings

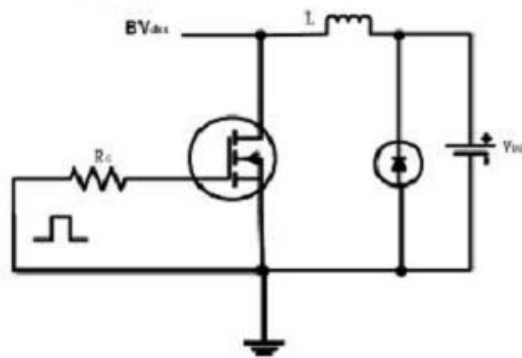
Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	150	A
	Pulsed		340	
Total Power Dissipation	@TA=25°C	P_D	90	W
Operating Junction Temperature Range		T_J	-55 to 150	°C

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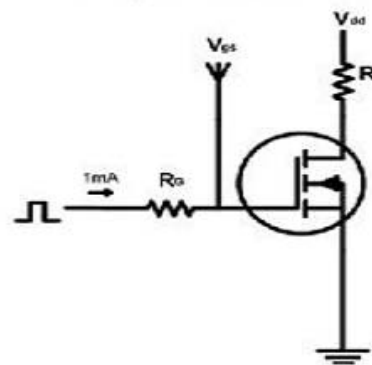
Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	30			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 24V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =20 V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	1	1.7	3.0	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A		2.1	3.2	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		7032		pF
C _{oss}	Output Capacitance			898		pF
C _{rss}	Reverse Transfer Capacitance			743		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =10V, V _{DS} =15V, I _D =30A		80		nC
Q _{gs}	Gate Source Charge			19		nC
Q _{gd}	Gate Drain Charge			38		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =15V, R _{GEN} =1Ω I _D =1A		20		ns
t _{d(off)}	Turn-Off Delay Time			80		ns
t _{d(r)}	Turn-On Rise Time			36		ns
t _{d(f)}	Turn-Off Fall Time			33		ns
Thermal Resistance						
Symbol	Parameter	Typ	Max	Units		
R _{θJC}	Junction to Case	-	2	°C/W		
R _{θJA}	Junction to Ambient (t ≤ 10s)	-	50	°C/W		

Test Circuits and Waveform

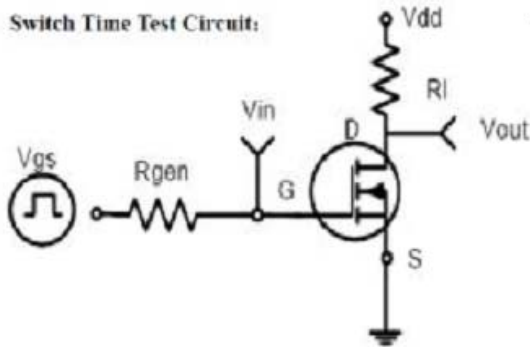
EAS test circuits:



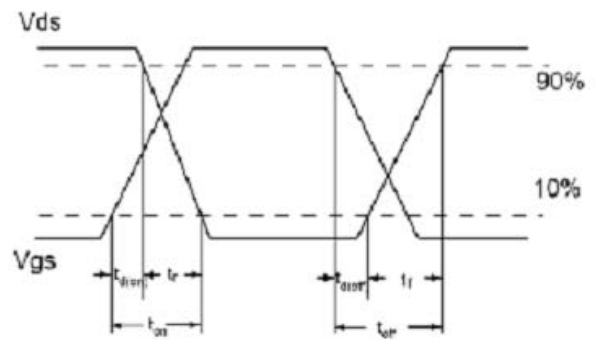
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Typical Characteristics

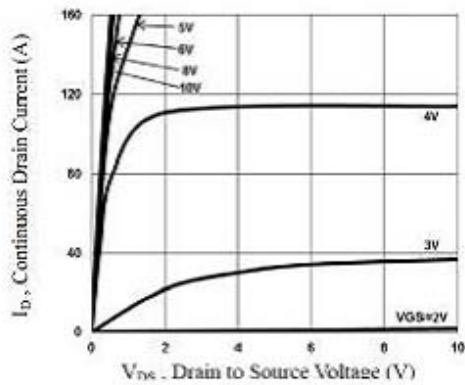


Figure 1: Typical Output Characteristics

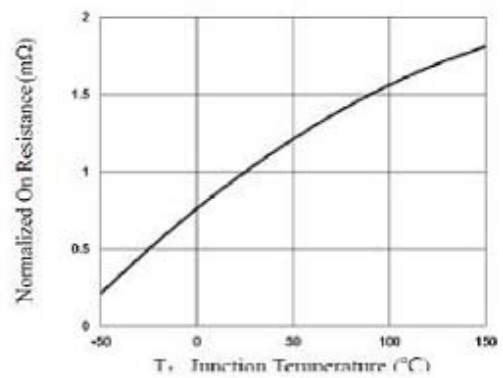


Figure 2: Normalized $R_{DS(on)}$ vs. T_J

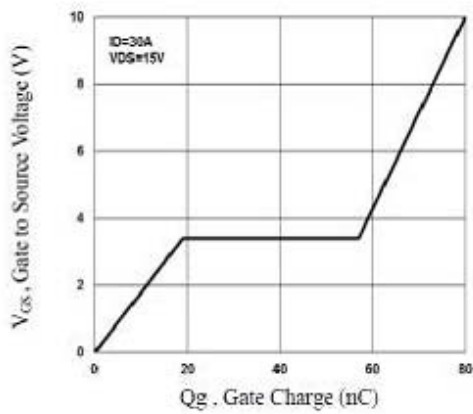


Figure 3: Gate-Charge Characteristics

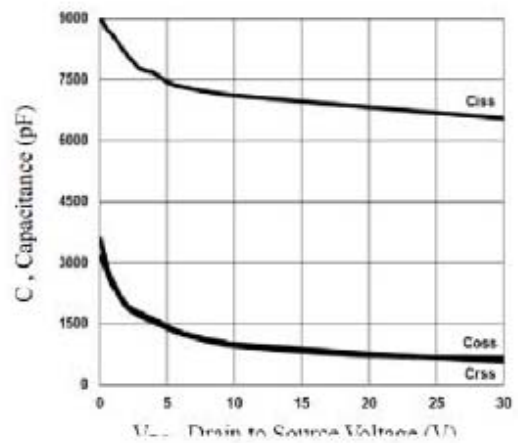


Figure 4: Capacitance Characteristics

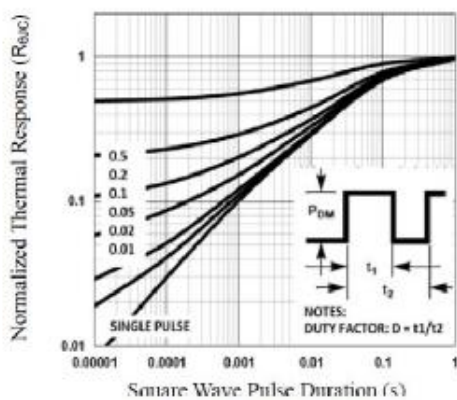


Figure 5: Normalized Thermal transient Impedance Curve

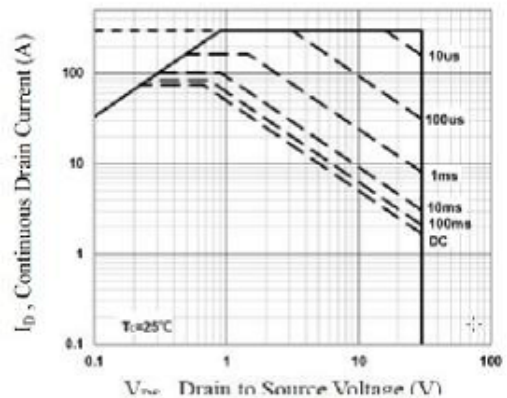
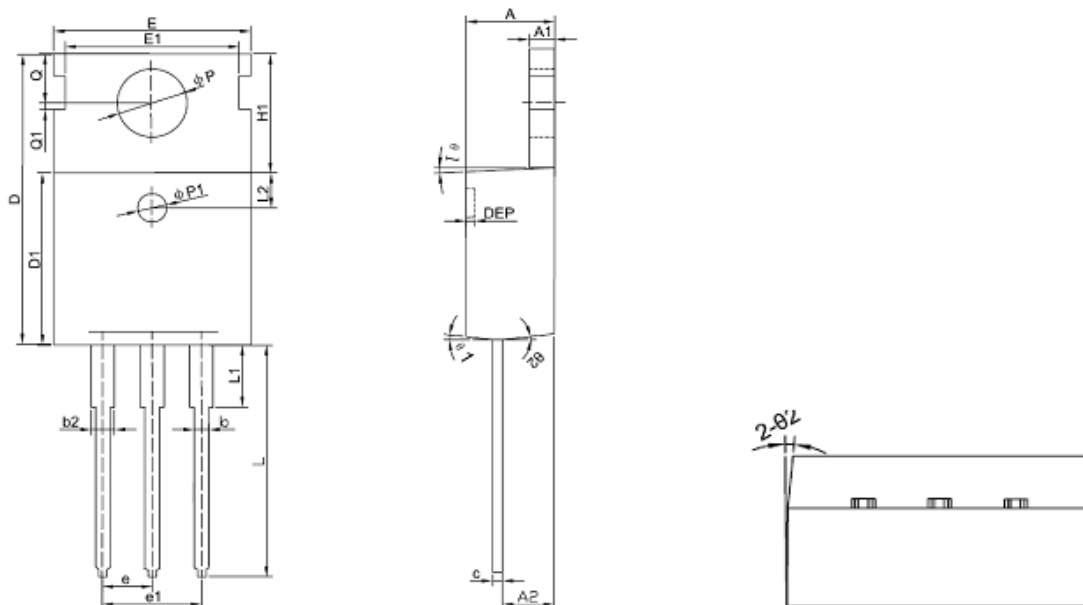


Figure 6: Maximum Safe Operation Area

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Package Outline Dimension

TO-220



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.590	2.690	2.790	0.102	0.106	0.110
b	0.770	-	0.900	0.030	-	0.035
b2	1.230	-	1.360	0.048	-	0.054
c	0.480	0.500	0.520	0.019	0.020	0.020
D	15.100	15.400	15.700	-	0.606	-
D1	9.000	9.100	9.200	0.354	0.358	0.362
DEP	0.050	0.285	0.520	0.002	0.011	0.020
E	10.060	10.160	10.260	0.396	0.400	0.404
E1	-	8.700	-	-	0.343	-
ΦP1	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.100	6.300	6.500	0.240	0.248	0.256
L	12.750	12.960	13.170	0.502	0.510	0.519
L1	-	-	3.950	-	-	0.156
L2	1.85REF			0.073REF		
ΦP	3.570	3.600	3.630	0.141	0.142	0.143
Q	2.730	2.800	2.870	0.107	0.110	0.113
Q1	-	0.200	-	-	0.008	-
Θ1	5°	7°	9°	5°	7°	9°
Θ2	1°	3°	5°	1°	3°	5°

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