

SE30P50B

**P-Channel Enhancement-Mode MOSFET**

Revision: A

**General Description**

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

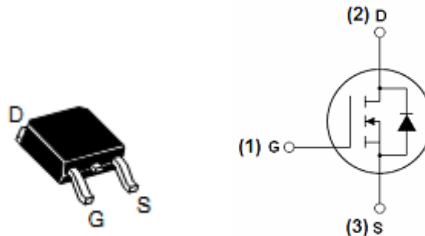
**Features**

For a single MOSFET

- $V_{DS} = -30V$
- $R_{DS(ON)} = 5.8m\Omega @ V_{GS}=-10$

**Pin configurations**

See Diagram below



**Absolute Maximum Ratings**

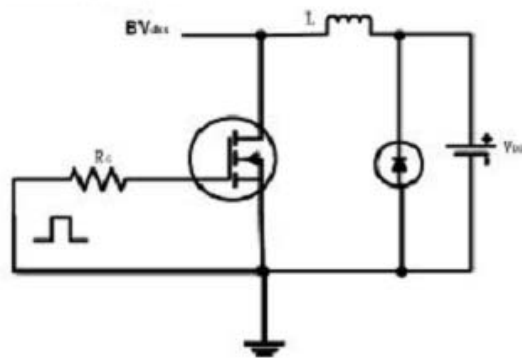
Parameter		Symbol	Rating	Units
Drain-Source Voltage		$V_{DS}$	-30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	Continuous	$I_D$	-50	A
	Pulsed		-120	
Total Power Dissipation	@TA=25°C	$P_D$	90	W
Operating Junction Temperature Range		$T_J$	-55 to 150	°C

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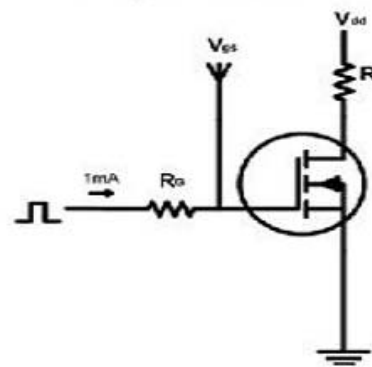
Electrical Characteristics (T <sub>J</sub> =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS (Note 2)</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0 V	-30			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>DS</sub> = -30V, V <sub>GS</sub> =0V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =20 V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	-0.4	-1.5	-2.2	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	-	5.8	7	mΩ
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		7032		pF
C <sub>oss</sub>	Output Capacitance			898		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			743		pF
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =30A		80		nC
Q <sub>gs</sub>	Gate Source Charge			19		nC
Q <sub>gd</sub>	Gate Drain Charge			38		nC
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>GEN</sub> =1Ω I <sub>D</sub> =1A		20		ns
t <sub>d(off)</sub>	Turn-Off Delay Time			80		ns
t <sub>d(r)</sub>	Turn-On Rise Time			36		ns
t <sub>d(f)</sub>	Turn-Off Fall Time			33		ns
<b>Thermal Resistance</b>						
Symbol	Parameter		Typ	Max		Units
R <sub>θJC</sub>	Junction to Case		-	2		°C/W
R <sub>θJA</sub>	Junction to Ambient (t ≤ 10s)		-	50		°C/W

Test Circuits and Waveform

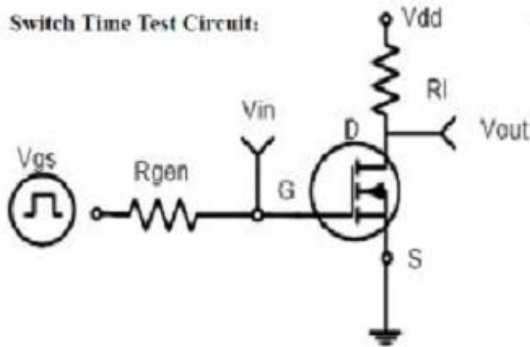
EAS test circuits:



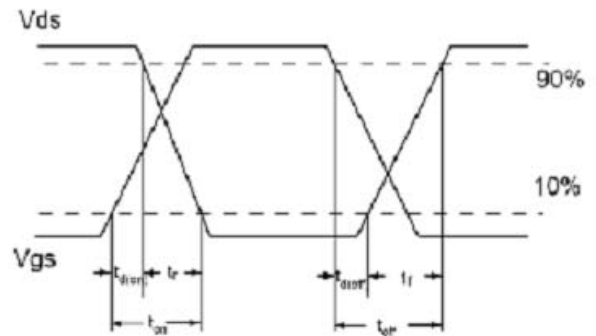
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Typical Characteristics

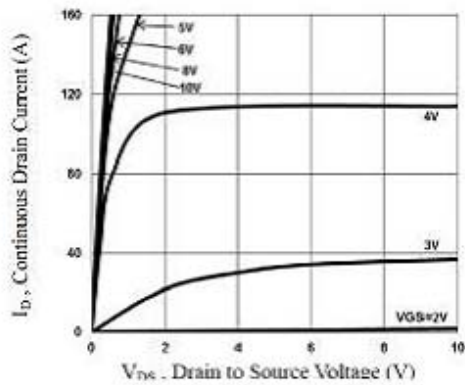


Figure 1: Typical Output Characteristics

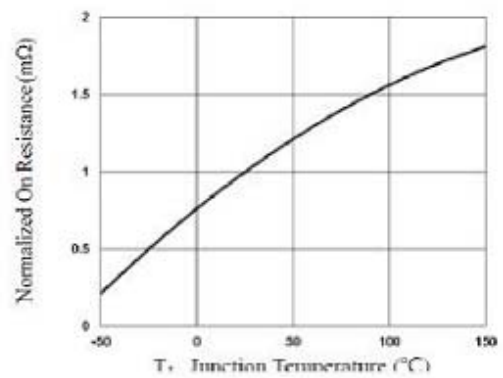


Figure 2: Normalized RDS(on) vs. TJ

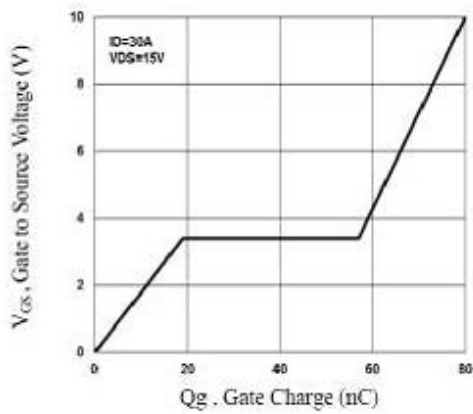


Figure 3: Gate-Charge Characteristics

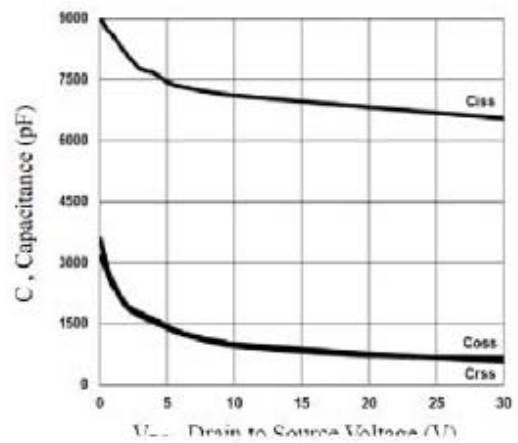


Figure 4: Capacitance Characteristics

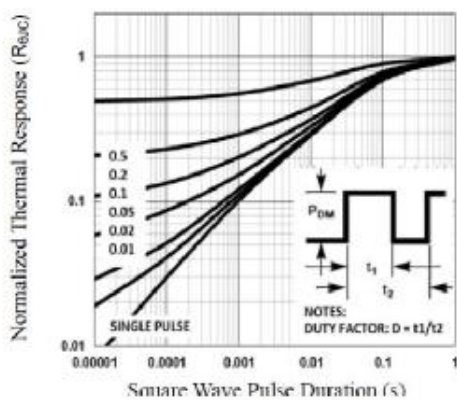


Figure 5: Normalized Thermal transient Impedance Curve

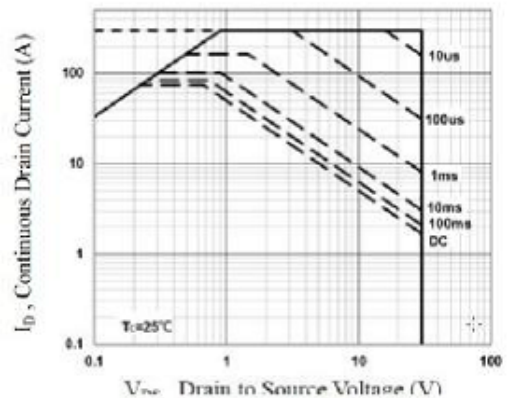
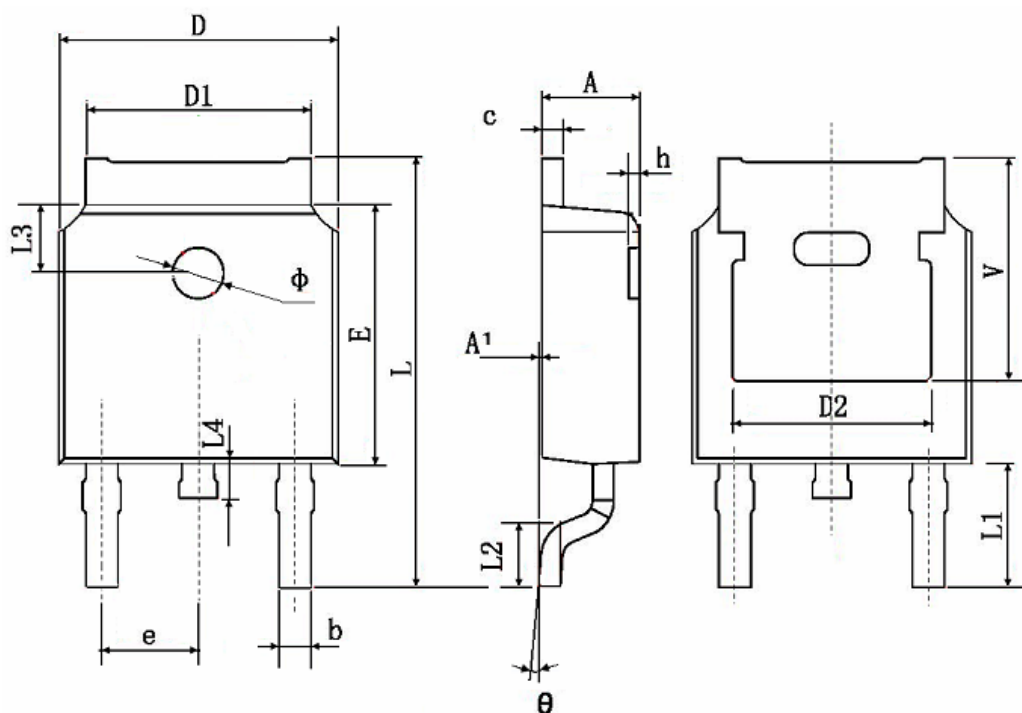


Figure 6: Maximum Safe Operation Area

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## Package Outline Dimension

### TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

**SE30P50B**

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