

SED14N65G

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

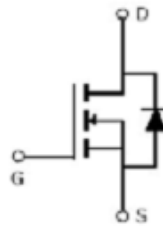
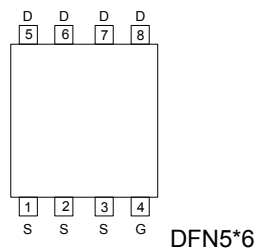
Features

For a single MOSFET

- $V_{DS} = 650V$
- $R_{DS(ON)} = 300m\Omega @ V_{GS}=10V$

Pin configurations

See Diagram below



Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain Current	Continuous	I_D	14	A
	Pulsed		30	
Single Pulse Avalanche Engergy		E_{AS}	226	mJ
Total Power Dissipation	@TA=25°C	P_D	156	W
Operating Junction Temperature Range		T_J	-55 to 150	°C

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Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	650			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 650V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =30V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	2		4	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =1A		300	360	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		1224		pF
C _{oss}	Output Capacitance			65		pF
C _{rss}	Reverse Transfer Capacitance			4		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =10V, V _{DS} =520V, I _D =6A		35	70	nC
Q _{gs}	Gate Source Charge			9		nC
Q _{gd}	Gate Drain Charge			16		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =520V, R _{GEN} =9.1Ω I _D =6A		16	32	ns
t _{d(off)}	Turn-Off Delay Time			35	70	ns
t _{d(r)}	Turn-On Rise Time			19	38	ns
t _{d(f)}	Turn-Off Fall Time			18	36	ns
Thermal Resistance						
Symbol	Parameter		Typ	Max		Units
R _{θJC}	Junction to Case		-	0.8		°C/W
R _{θJA}	Junction to Ambient (t ≤ 10s)		-	62		°C/W

Typical Characteristics

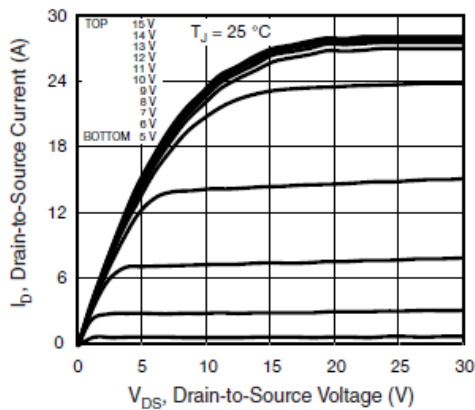


Fig. 1 - Typical Output Characteristics

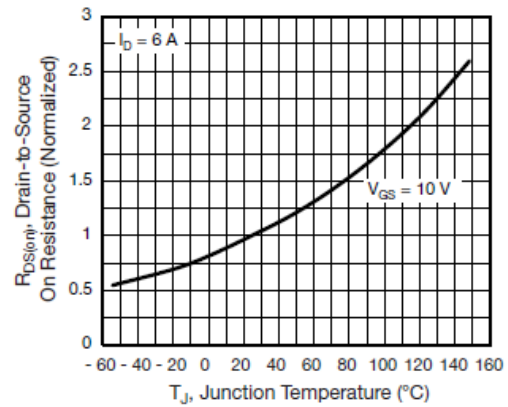


Fig. 4 - Normalized On-Resistance vs. Temperature

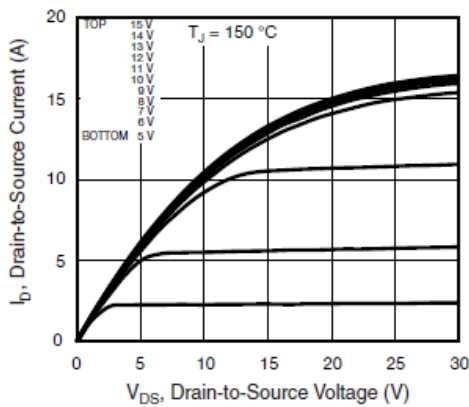


Fig. 2 - Typical Output Characteristics

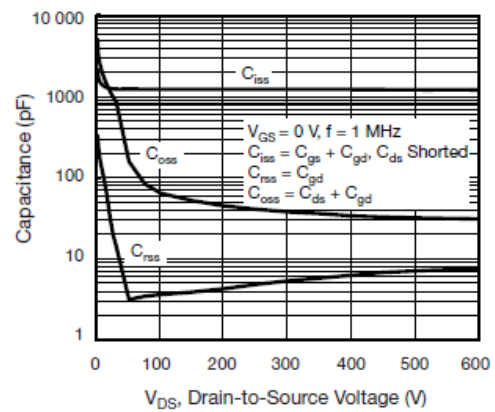


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

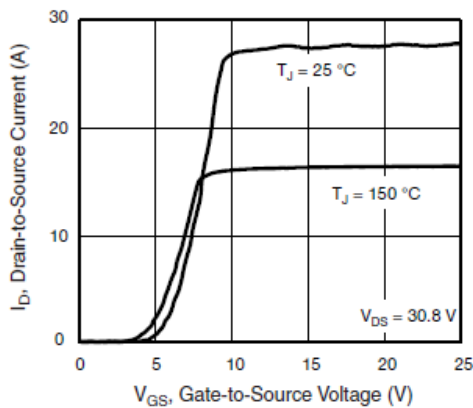


Fig. 3 - Typical Transfer Characteristics

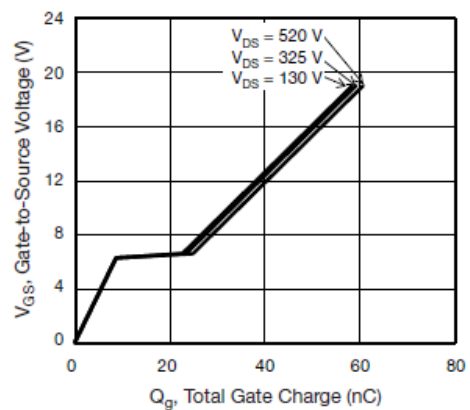


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

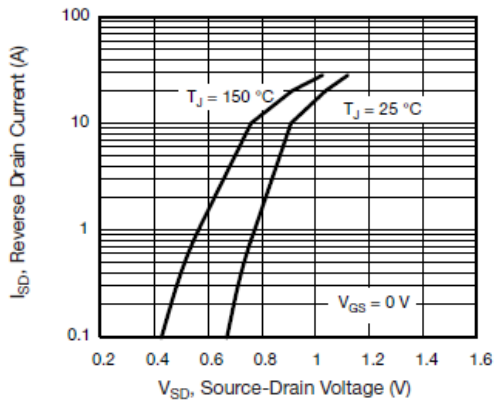


Fig. 7 - Typical Source-Drain Diode Forward Voltage

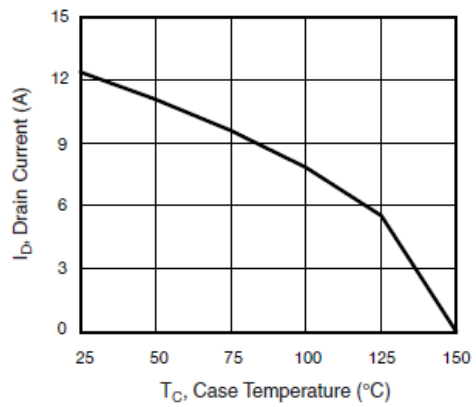


Fig. 9 - Maximum Drain Current vs. Case Temperature

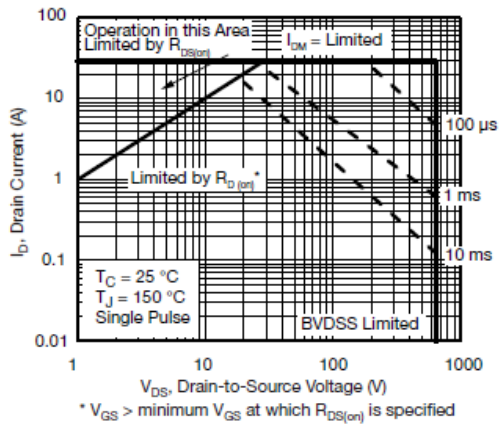


Fig. 8 - Maximum Safe Operating Area

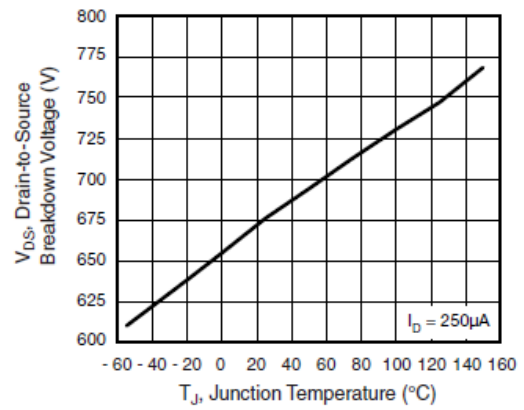


Fig. 10 - Temperature vs. Drain-to-Source Voltage

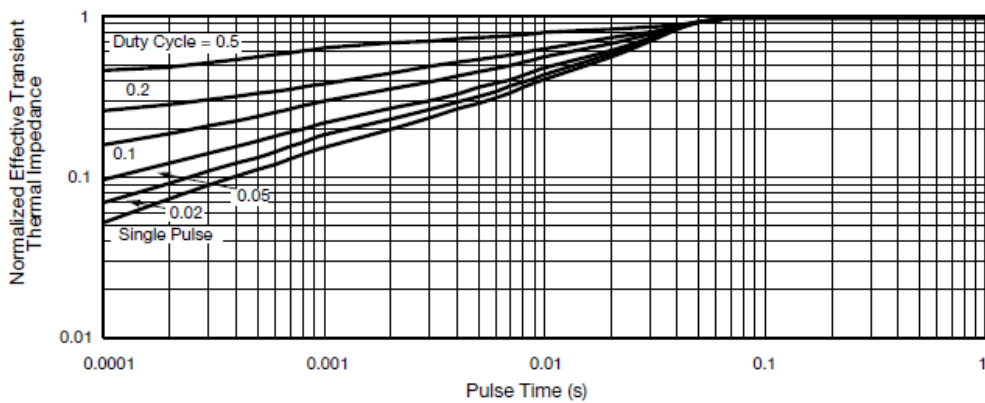
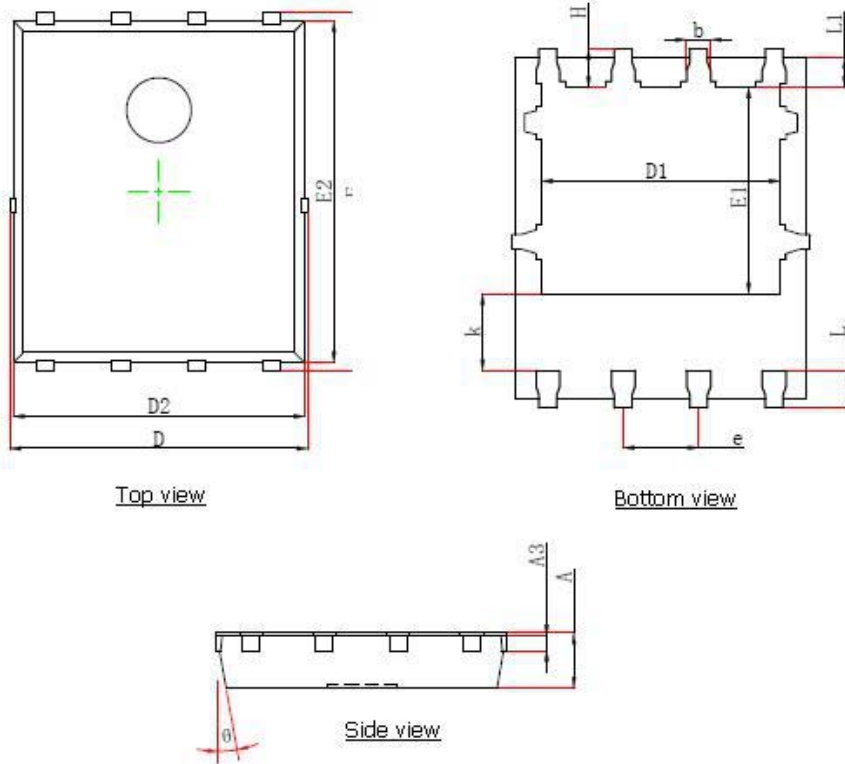


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

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Package Outline Dimension

DFN5 × 6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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