

# SiT5711

1 to 60 MHz Emerald Platform™ Stratum 3E OCXO



## Description

The SiT5711 is the industry's smallest Stratum 3E OCXO (9 mm x 7 mm) with  $\pm 5$  ppb over-temp stability and  $\pm 0.04$  ppb/ $^{\circ}\text{C}$  typical frequency slope (dF/dT). Leveraging SiTime's unique DualMEMS® and TurboCompensation® temperature sensing technology, it delivers excellent stability in the presence of environmental stressors – airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The SiT5711's environmental robustness enables unmatched ease-of-use and reduces system manufacturing overhead:

- Highly flexible location on the PCB
- Minimal shielding for thermal isolation

SiT5711 can be factory-programmed to any frequency between 1 MHz and 60 MHz. The SiT5711 is supported by the SiT6731 evaluation board.

## Features

- Any frequency between 1 MHz and 60 MHz, in 1 Hz steps
- $\pm 0.04$  ppb/ $^{\circ}\text{C}$  frequency slope typical dF/dT
- $\pm 5$  ppb frequency stability over temperature
- Up to  $85^{\circ}\text{C}$  operating temperature range
- $1.4\text{E}-11$  ADEV at 10 second averaging time
- Exceptional dynamic stability under airflow and rapid temperature changes
- Excellent Holdover over a wide range of conditions
- Integrated regulators for on-chip power-supply noise filtering and excellent PSNR
- GR-1244 Stratum 3E compliant
- Resistant to shock and vibration
- 3.3 V supply voltage
- LVCMOS and Clipped Sinewave outputs

## Applications

- 4G/5G radio
- Base Stations
- Digital Switching
- Time and Frequency Measurement
- IEEE 1588
- Test and measurement

### 9 mm x 7 mm Package



Figure 1. Top and bottom view

### Package Pinout

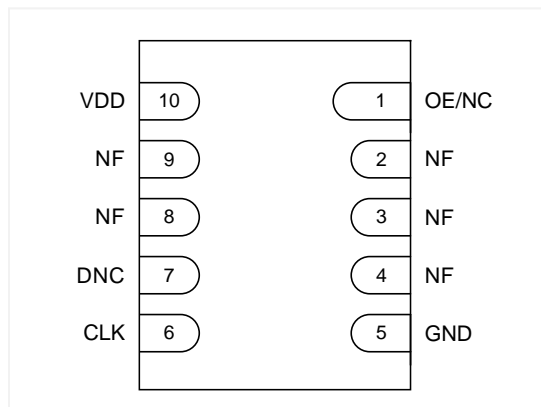
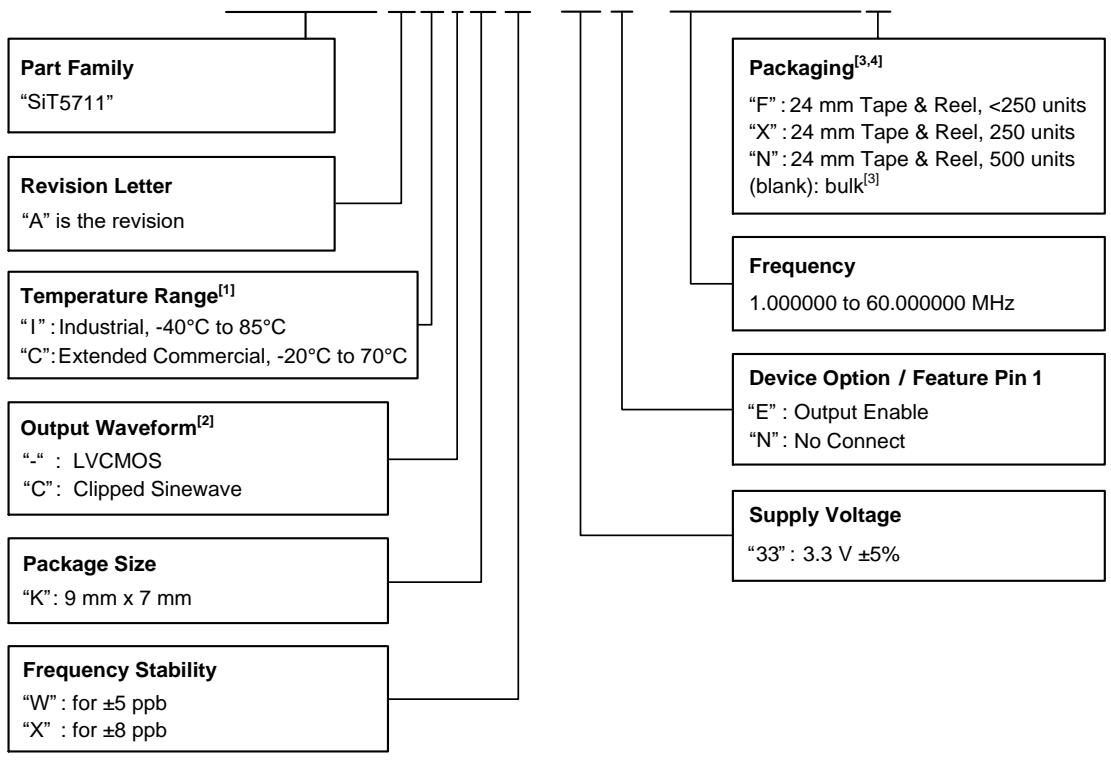


Figure 2. Pin Assignments (Bottom view)

Ordering Information

SiT5711 AC-KW-33E - 19.123456X



Notes:

1. Contact SiTime for other temperature range options.
2. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 2 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI.
3. Bulk is available for sampling only.

Table 1. Ordering Codes for Supported Tape & Reel Packaging Method<sup>[4]</sup>

Device Size	24 mm T&R (<250 units)	24 mm T&R (250 units)	24 mm T&R (500 units)
9 mm x 7 mm	F	X	N

Notes:

4. 10 unit minimum order quantity for tape and reel packaging.

## Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage. Typical values are at 25°C and 3.3 V VDD. All measurements are specified with 15 pF load unless otherwise stated.

**Table 2. Output Characteristics**

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Coverage</b>						
Output Frequency Range	F	1	–	60	MHz	
<b>Frequency Stability</b>						
Frequency Stability over Temperature	F_stab	-5	–	+5	ppb	Referenced to (fmax + fmin)/2 over the specified temperature range. <a href="#">Contact SiTime</a> for ±3 ppb or tighter frequency stability. Measured after 48 hours of operation.
		-8	–	+8	ppb	
Frequency vs. Temperature Slope	dF/dT	-0.12	±0.04	+0.12	ppb/°C	Steady airflow <3 m/s, 1°C/min ramp rate
Dynamic Frequency Change to Temperature Ramp	F_dynamic	-0.002	±0.0007	+0.002	ppb/s	Steady airflow <3 m/s, 1°C/min ramp rate
Initial Tolerance	F_init	-300	–	+300	ppb	Offset from nominal frequency (F) after 2 reflows, measured at 25°C
Hysteresis Over Temperature	F_Hys	-0.8	±0.11	+0.8	ppb	Over -40 to 85°C, measured as maximum frequency deviation from center of hysteresis eye, 1°C/min ramp rate
One-day Aging	F_1d	–	±0.7	±1.6	ppb	After 60-days operation, 50°C
One-month Aging	F_1m	–	±32	±57	ppb	After 30-days operation, 50°C
One-year Aging	F_1y	–	±110	±230	ppb	After 30-days operation, 50°C
Ten-year Aging	F_10y	–	±220	±394	ppb	After 30-days operation, 50°C
Total Stability – 20 years	F_20y_stab	-1	–	+1	ppm	Better than Stratum 3E stability of ±4.6 ppm over 20 years per GR-1244-CORE. Inclusive of initial tolerance, frequency stability over temperature, 20-year Aging, and variations to supply voltage and output load. Typically called free running accuracy
Supply Voltage Sensitivity	F_vdd	–	±0.3	–	ppb	V <sub>DD</sub> ±5%
Output Load Sensitivity	F_load	–	±0.2	–	ppb	LVC MOS output, 15 pF ±10%
		–	±0.1	–	ppb	Clipped sinewave output, 10 kΩ    10 pF ±10%
<b>Start-up Characteristics</b>						
Start-up Time	T_start	–	2.5	3.5	ms	Time to first pulse
OE Time	OE_Tstart	–		680	ns	Time to first pulse after OE pin reaches 70% of V <sub>DD</sub> , 10 MHz
Warm-up Time	T_warmup	–	20	150	s	Time to within ±10 ppb of final frequency. Final frequency measured at one hour. Device powered on for 48 hours then powered off for 1 hour prior to measurement.
		–	–	45	ms	Time to within ±200 ppb of final frequency. Final frequency measured at one hour. Device powered on for 48 hours then powered off for 1 hour prior to measurement.
<b>LVC MOS Output Characteristics</b>						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	tr, tf	–	2.2	3	ns	10% - 90% V <sub>DD</sub>
Output Voltage High	V <sub>OH</sub>	90%	–	–	V <sub>DD</sub>	I <sub>OH</sub> = ±3 mA, (V <sub>DD</sub> = 3.3 V)
Output Voltage Low	V <sub>OL</sub>	–	–	10%	V <sub>DD</sub>	I <sub>OL</sub> = ±3 mA, (V <sub>DD</sub> = 3.3 V)
<b>Clipped Sinewave Output Characteristics</b>						
Output Voltage Level	V <sub>OUT</sub>	0.8	–	1.2	V	Measured peak-to-peak swing at any V <sub>DD</sub> – 10 kΩ    10 pF ±10%
Rise/Fall Time	tr, tf	–	3.9	4.6	ns	20%–80% V <sub>OUT</sub>

Table 3. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Supply Voltage</b>						
Supply Voltage	V <sub>DD</sub>	3.14	3.3	3.47	V	Contact SiTime for other voltage options
<b>Power Consumption</b>						
Power Consumption – Warm-up	Pwr_warmup	–	–	2.3	W	
Power Consumption – Steady State	Pwr_steady	–	0.95	1.1	W	At +25°C
<b>Temperature Range</b>						
Operating Temperature Range	T <sub>use</sub>	-20	–	+70	°C	Extended commercial
		-40	–	+85	°C	Industrial. Contact SiTime for -55°C and 95°C support

Table 4. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Input Characteristics – OE Pin</b>						
Input Impedance	Z <sub>in</sub>	75	–	–	kΩ	Internal pull up to V <sub>DD</sub>
Input High Voltage	V <sub>IH</sub>	70	–	–	%	
Input Low Voltage	V <sub>IL</sub>	–	–	30	%	

Table 5. Jitter &amp; Phase Noise

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Jitter</b>						
RMS Period Jitter	T <sub>jitt</sub>	–	1	1.3	ps	F = 10 MHz, population 10 k
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.4	0.55	ps	F = 10.3 MHz, Integration bandwidth = 12 kHz to 5 MHz
<b>Allan Deviation</b>						
$\tau = 1 \text{ second}$	AD_1s	–	1.6E-11	–		Measured after 48 hours operation.
$\tau = 10 \text{ seconds}$	AD_10s	–	1.4E-11	–		
$\tau = 100 \text{ seconds}$	AD_100s	–	1.6E-11	–		
$\tau = 1,000 \text{ seconds}$	AD_1000s	–	2.5E-11	–		
$\tau = 10,000 \text{ seconds}$	AD_10000s	–	1.4E-10	–		
<b>Phase Noise</b>						
1 Hz offset		–	-81	-78	dBc/Hz	Reference f = 10.3 MHz
10 Hz offset		–	-109	-106	dBc/Hz	
100 Hz offset		–	-128	-125	dBc/Hz	
1 kHz offset		–	-147	-145	dBc/Hz	
10 kHz offset		–	-152	-149	dBc/Hz	
100 kHz offset		–	-152	-149	dBc/Hz	
1 MHz offset		–	-164	-161	dBc/Hz	
5 MHz offset		–	-165	-160	dBc/Hz	

Table 6. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-55	105	°C
V <sub>DD</sub>	-0.5	4	V
Soldering Temperature (follow standard Pb-free soldering guidelines)	–	260	°C

**Table 7. Thermal Considerations**

Package	$\theta_{JA}^{[5]}$ (°C/W)
Stacked-PCB 9.0 mm x 7.0 mm	110

General guidelines for the thermal design of the PCB are the following:

- 1) The power and ground planes should be continuous in the 9 x 7 mm area directly under the device.
  - 2) Thermal vias should not be added to 9 x 7 mm area directly under the device.
  - 3) The thermal properties of the PCB should be designed such that the steady state device power is limited to 1.6 W at -40°C.
- For more details on recommendations for thermal design [Contact SiTime](#).

**Table 8. Environmental Compliance<sup>[6]</sup>**

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method2007, Condition A JEDEC JESD22-B103, Condition 1
Temperature Cycle	JESD22, MethodA104
Solderability	MIL-STD-883F, Method2003
Moisture Sensitivity Level	MSL3
Washability	Non-Washable

**Notes:**

5. The presented  $\theta_{JA}$  is for a device on a JESD51-7 2s2p compliant board in still air.  $\theta_{JA}$  is a function of board design and ambient environments.
6. This device is RoHS and REACH compliant Pb-free and is Halogen-free and Antimony-free.

## Pin-out Bottom View

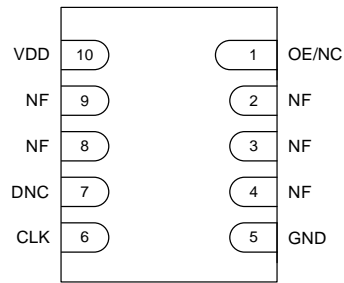


Figure 3. Size 9 mm x 7 mm

Table 9. Pin Assignments

Package Size	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
9 mm x 7 mm	OE/NC	NF	NF	NF	GND	CLK	DNC	NF	NF	VDD

Table 10. Pin Description

Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
OE/NC	OE – Input	100 kΩ Pull-Up	H <sup>[7]</sup> : specified frequency output L: output is high impedance. Only output driver is disabled
	NC – No Connect	-	H or L or Open: No effect on output frequency or other device functions <sup>[8]</sup>
NF	No Function	-	Solder to pads. Connect to VDD <sup>[9]</sup>
GND	Ground	-	Connect to ground <sup>[10]</sup>
DNC	Do Not Connect	-	Solder to pads. Do not connect <sup>[11]</sup>
CLK	Output	-	LVC MOS, or clipped sinewave oscillator output
VDD	Power	-	Connect to VDD

### Notes:

- In OE mode, a pull-up resistor of 100 kΩ or less is recommended if Pin 1 is not externally driven. If Pin 1 needs to be left floating, use the NC option.
- Pin 1 voltage should not exceed device VDD or fall lower than device GND. Either of these conditions may lead to frequency shifts larger than specified limits.
- SiTime recommends electrical connection to VDD. Use narrow traces (e.g. 4 to 6 mil) to avoid significant heat dissipation through these pads.
- 0.1 μF capacitor in parallel with a 10 μF capacitor are required between VDD and GND.
- Connecting DNC pin to VDD or ground may cause the device to malfunction.

### Test Circuit Diagrams

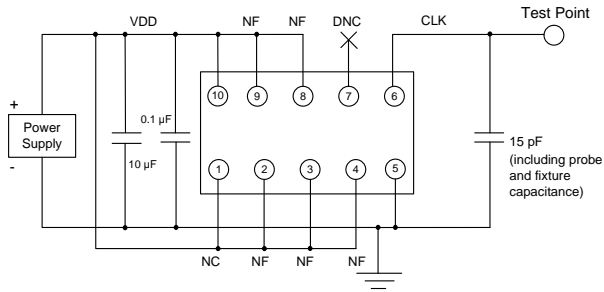


Figure 4. LVC MOS Test Circuit (NC Function)

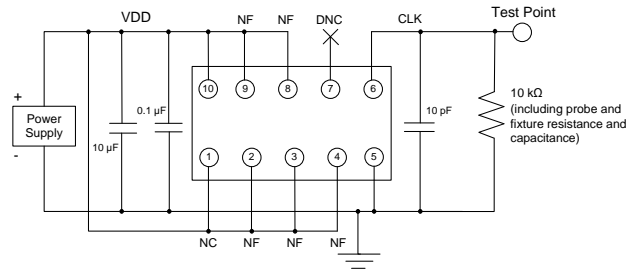


Figure 5. Clipped Sinewave Test Circuit (NC Function)

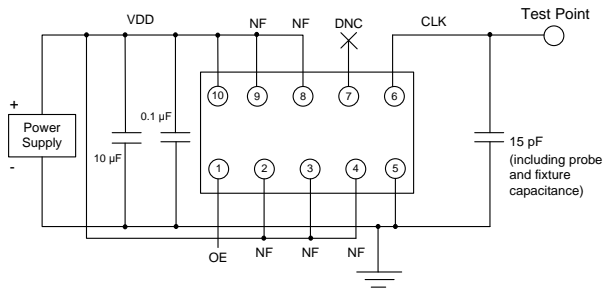


Figure 6. LVC MOS Test Circuit (OE Function)

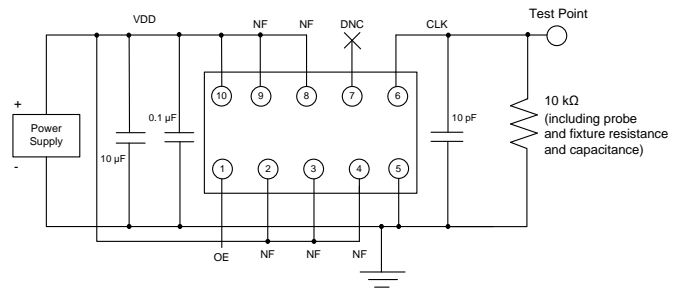


Figure 7. Clipped Sinewave Test Circuit (OE Function)

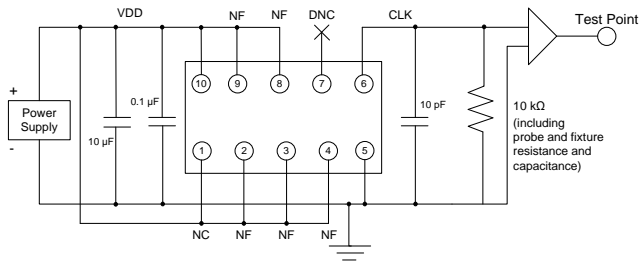


Figure 8. Phase Noise Clipped Sinewave Test Circuit (NC Function)

## Waveforms

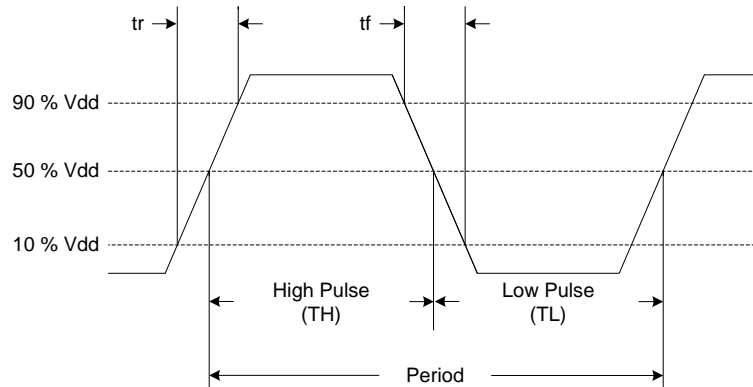


Figure 9. LVC MOS Waveform Diagram<sup>[12]</sup>

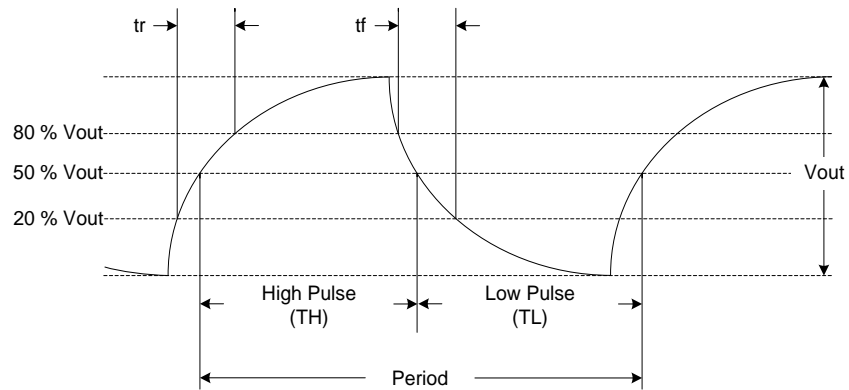


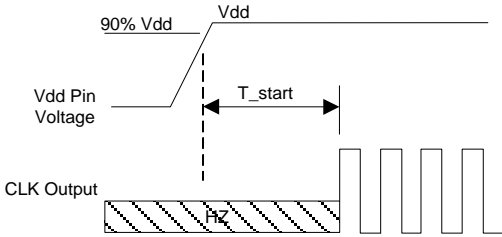
Figure 10. Clipped Sinewave Waveform Diagram<sup>[12]</sup>

**Note:**

- 12. Duty Cycle is computed as  $Duty\ Cycle = TH/Period$ .

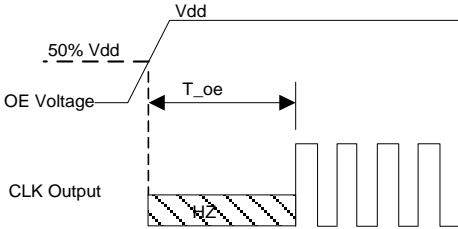


### Timing Diagrams



T\_start: Time to start from power-off

**Figure 11. Startup Timing**



T\_oe: Time to re-enable the clock output

**Figure 12. OE Enable Timing (OE Mode Only)**

Typical Performance Plots

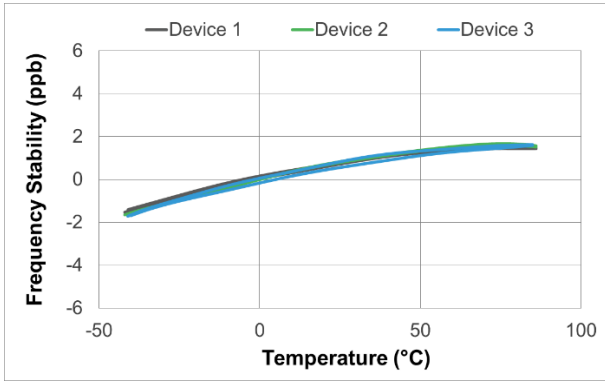


Figure 13. Frequency Stability

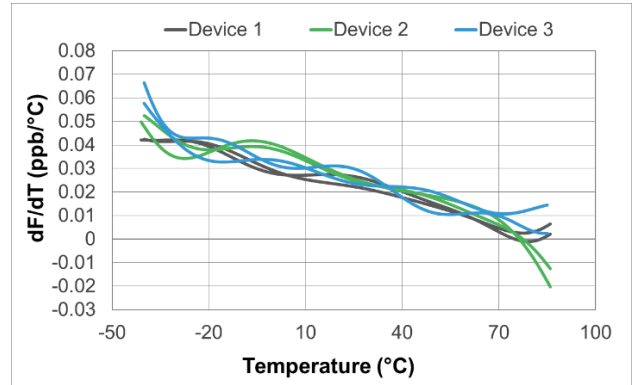


Figure 14. Frequency Slope

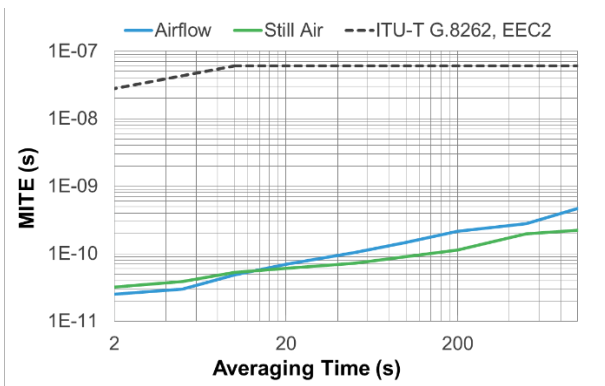


Figure 15. MTIE

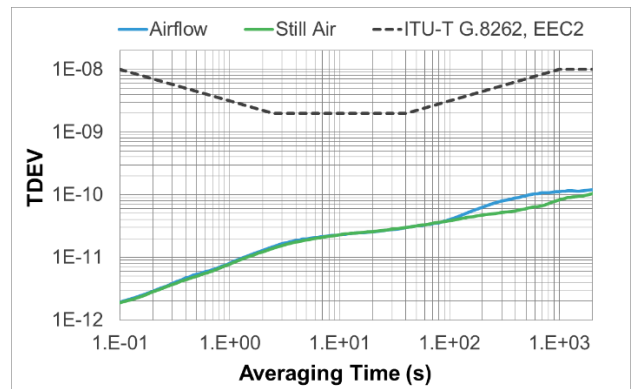


Figure 16. TDEV

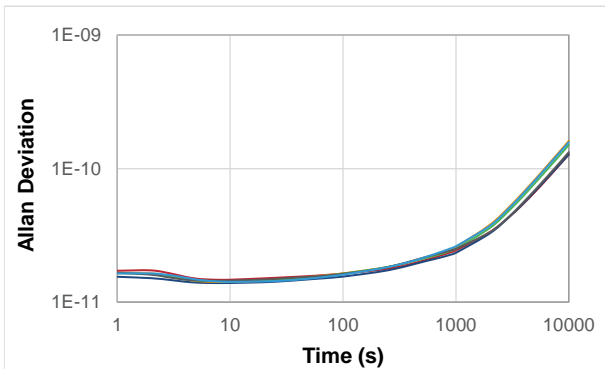


Figure 17. ADEV Still Air

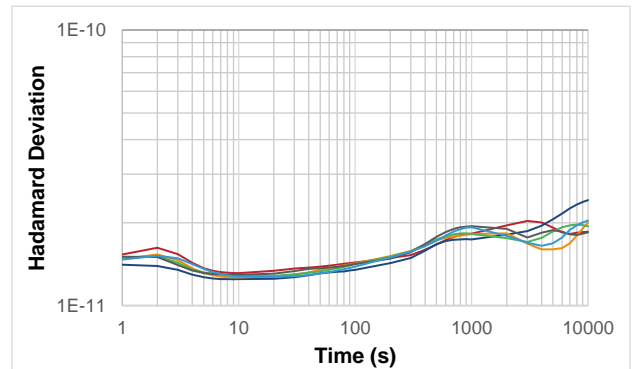


Figure 18. HDEV Still Air

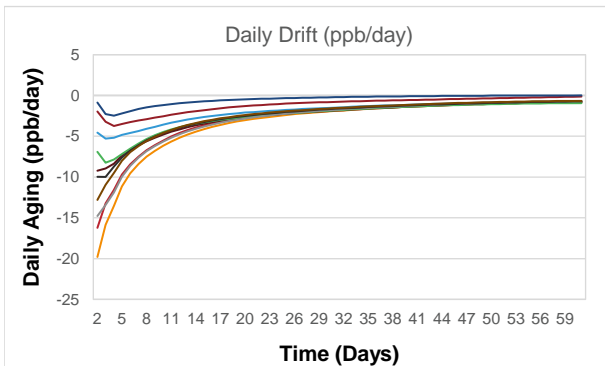
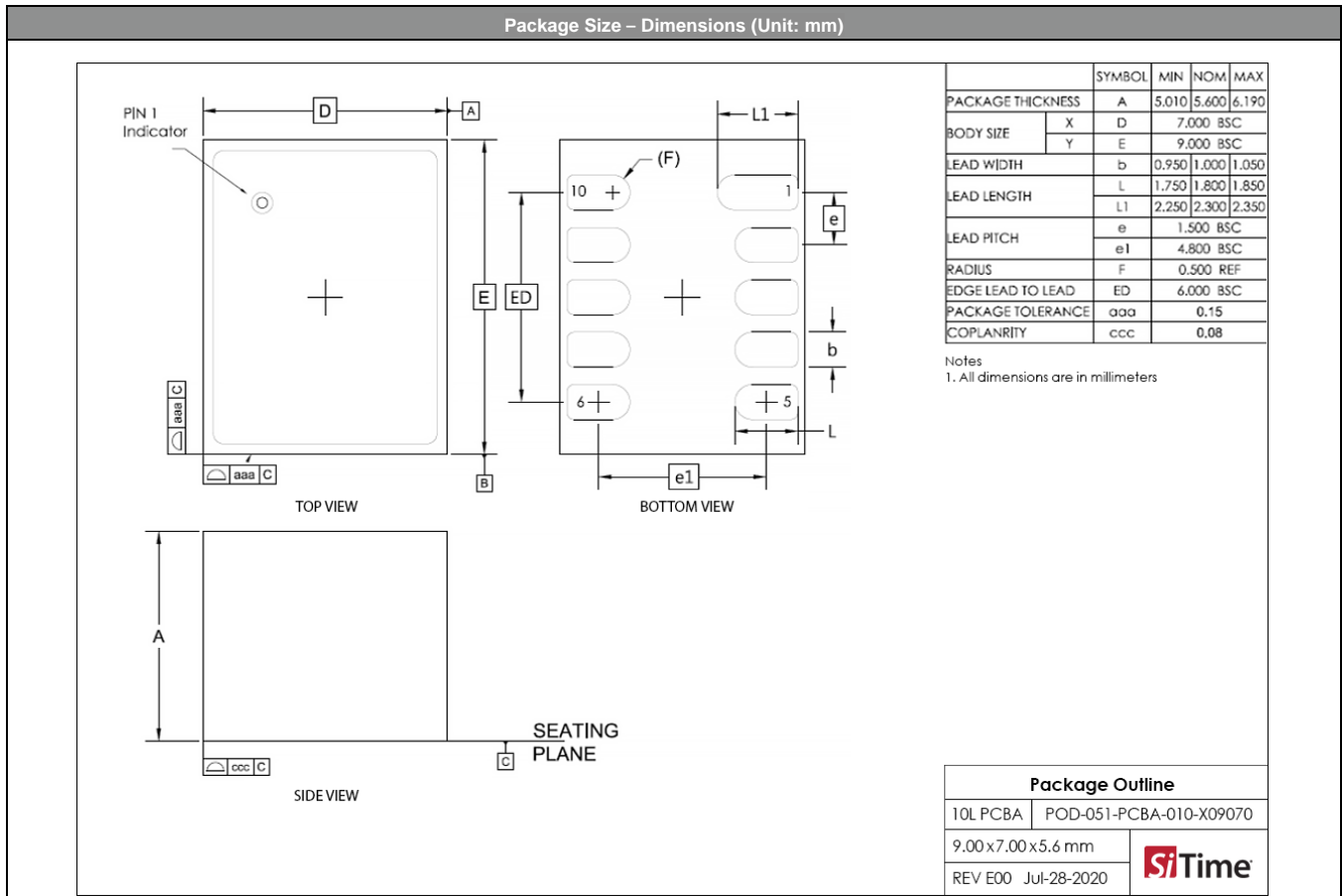
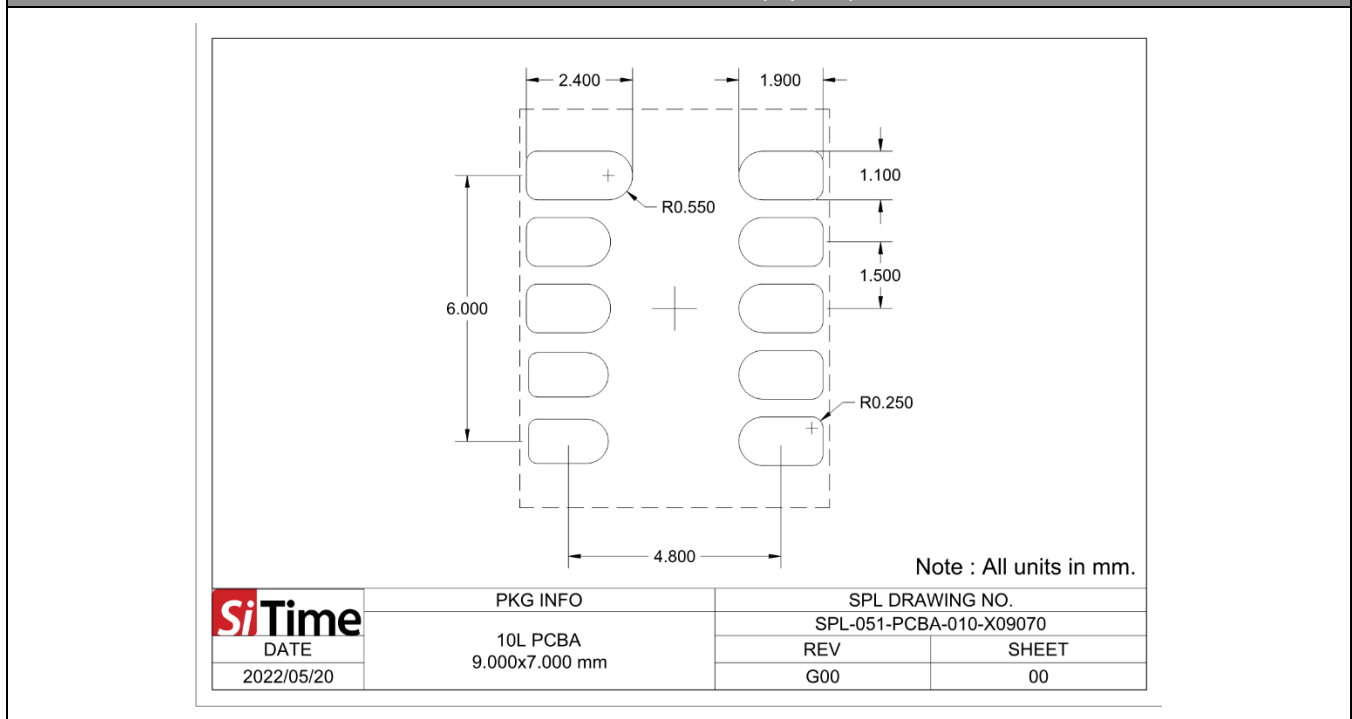


Figure 19. Daily Aging (50°C)

Dimensions and Patterns — 9 mm x 7 mm package



Recommended Land Pattern (Top View)



## Layout Guidelines

- SiT5711 uses internal regulators to minimize the impact of the power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1  $\mu$ F and 10  $\mu$ F). Place the bypass capacitors as close to the VDD pin as possible, typically within 1 to 2 mm. Ensure 0.1  $\mu$ F cap is placed closest to the device VDD and GND power pins.
- SiT5711 is engineered to have superior performance when compared to quartz OCXOs in the presence of ambient disturbers such as airflow and temperature transients. Therefore, the use of a metal cover typical for quartz OCXOs can often be avoided.
- For additional layout recommendations, refer to the [Best Design Layout Practices](#).

## Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the SiT5711 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- After the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, it is recommended to use “no clean” flux. Do not subject SiT5711 to liquid based cleaning processes.
- Reflow profile, per JESD22-A113D
- For additional manufacturing guidelines and marking/tape-reel instructions, refer to [SiTime Manufacturing Notes](#)

## Additional Information

**Table 11. Additional Information**

Document	Description
<b>ECCN #: EAR99</b>	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.
<b>HTS Classification Code: 8542.39.0000</b>	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.
<b>SiT6731 EVB</b>	Evaluation board, <a href="#">contact SiTime</a>
<b>Time Machine II</b>	<a href="#">MEMS oscillator programmer</a>
<b>Field Programmable Oscillators</b>	<a href="#">Devices that can be programmable in the field by Time Machine II</a>
<b>Manufacturing Notes</b>	<a href="#">Tape &amp; Reel dimension, reflow profile and other manufacturing related info</a>
<b>Qualification Reports</b>	<a href="#">RoHS report, Reliability reports, Composition reports</a>
<b>Performance Reports</b>	<a href="#">Additional performance data such as phase noise, current consumption, and jitter for selected frequencies</a>
<b>Termination Techniques</b>	<a href="#">Termination design recommendations</a>
<b>Layout Techniques</b>	<a href="#">Layout recommendations</a>
<b>Other Quality Documents</b>	<a href="#">ISO certificate, materials declarations, environmental policy, warranty on date code</a>

Table 12. Revision History

Version	Release Date	Change Summary
0.1	17-Jul-2018	First release, advanced information
0.11	27-Jul-2018	Changed Pin 2 and Pin 7 to Rsvd (reserved)
0.12	8-Aug-2018	Added 9x7 mm package option in the ordering code Added 9x7 mm package pad layout recommendation Misc. corrections
0.13	9-Aug-2018	Removed 10 mm x 10 mm package Misc. formatting changes
0.14	27-Aug-2018	Added $\pm 3$ ppb support Added 14.0 x 9.0 mm, 20.0 x 13.0 mm, 25.0 x 22.0 mm packages Updated Table 2 and Ordering information Added Package Drawing section
0.8	1-Nov-2018	Update frequency slope to $\pm 0.15$ ppb $^{\circ}$ /C Misc. corrections
0.81	15-Feb-2019	Updated Ordering information Added Typical Performance Plots section Rearranged sections Added Pin Outs for 14x9 mm, 20x13 mm and 25x22 mm Updated Layout Guidelines Added T&R options Added factory option note to the Typical Plots Labeled package Top Views Other minor corrections
0.82	15-Mar-2019	Updated drawings for 14x9, 20x13 and 25x22 mm packages
0.83	10-Oct-2019	Updated Phase Noise ( <i>typical</i> ) in Table 5 Updated Packages Pinout, added Washability and additional information
0.84	3-Dec-2019	Changed Rise/Fall time condition for Clipped Sinewave Output Characteristics
0.85	2-Mar-2020	Package Drawings edits
0.91	20-Apr-2020	Updated various specifications and conditions after characterization Updated package drawings and pinouts view
0.92	5-Jun-2020	Updated Typical Performance Plots Cycle to Cycle Jitter Removed Hysteresis Specification Updated Manufacturing Notes Updated
0.93	7-Dec-2020	Updated pin description and package drawings Updated conditions for initial tolerance Updated minimum and maximum storage Updated dimensions and patterns Updated layout guidelines
0.94	24-Aug-2021	Updated various electrical specifications after further characterization Updated minimum order quantity for tape and reel packing Added thermal considerations Updated recommended land pattern
1.0	7-Jun-2022	Updated the product description Changed the name of pin 7 to "DNC" for added clarity Updated the aging, Allan deviation, and phase noise specifications with the latest characterization data Updated the typical rise/fall time specification with the latest characterization data Updated the thermal considerations and guidelines Added test circuit and waveform diagrams Added Allan deviation, Hadamard deviation, and daily aging performance plots

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[10.000MHz-SW](#) [AOCJY3A-10.000MHz](#) [AOC2012XAJC-10.0000C](#) [AOC2012XAJC-12.8000C](#) [AOC2012XAJC-25.0000C](#)  
[AOC2522BVAUC-20.0000](#) [AOC2522BVAUC-12.8000](#) [AOC2522BVAUC-38.8800](#) [AOCJY-10.000MHz](#) [AOCJY-10.000MHz-F](#) [AOCJY1-](#)  
[10.000MHZ](#) [AOCJY1-40.000MHz-E](#) [AOCJY1A-100.000MHz](#) [AOCJY1A-10.000MHz](#) [AOCJY-20.000MHz](#) [AOCJY-20.000MHZ-F](#)  
[AOCJY2-100.000MHz-F-SW](#) [AOCJY2-10.000MHZ-E](#) [AOCJY2-100.000MHZ-E](#) [AOCJY2-100.000MHZ-E-SW](#) [AOCJY-38.880MHz](#)  
[AOCJY3B-10.000MHz-E](#) [AOCJY5-10.000MHz](#) [AOCJY6-10.000MHz-1](#) [AOCJYR-10.000MHz-M5625LF](#) [AOCJYR-10.000MHz-M5625LF-](#)  
[T](#) [AOCJY1A-100.000MHZ-E](#) [AOCJY2-10.000MHZ-E-SW](#) [AOCJY3A-100.000MHZ-F](#) [ECOC-2522-100.000-3FC](#) [ECOC-2522-10.000-3FC](#)  
[ECOC-2522-38.880-3FC](#) [LFOCXO063800BULK](#) [LFOCXO063801BULK](#) [LFOCXO063804BULK](#) [LFOCXO063815BULK](#)