

Features, Benefits and Applications

- MEMS oscillator with LVCMOS/LVTTL compatible output
- 1-110 MHz frequency range
- Frequency stability as low as ±20 PPM
- Typical current consumption of 6.1 mA in active mode
- Standby or output enable modes
- 1.8V, 2.5V 3.3V supply voltage
- SoftEdgeTM configurable rise/fall time for driving higher loads or EMI reduction.
- Four industry-standard packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm
- All-silicon device with outstanding reliability of 2 FIT, 10x improvement over quartz-based devices
- Ultra short lead time
- Ideal for consumer electronics: video, set top boxes, HDTV, DVR, scanners, printers, IP camera, etc.
- Ideal for high-speed serial protocols: Ethernet, USB, SATA, SAS, Fibre Channel, Firewire, PCI Express

Specifications

Electrical Characteristics^[1]

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
Output Frequency Range	f	1	-	110	MHz		
Frequency Stability	F_stab	-20	-	+20	PPM	Inclusive of: Initial stability, operating temperature, rated po	
	-	-25	-	+25	PPM	supply voltage change, load change, shock and vibration.	
		-30	-	+30	PPM	± 20 PPM available in extended commercial	
		-50	-	+50	PPM	temperature only	
Aging	Ag	-1.0	-	1.0	PPM	1st year at 25°C	
Operating Temperature Range	T_use	-20	-	+70	°C	Extended Commercial	
	_	-40	-	+85	°C	Industrial	
Supply Voltage	Vdd	1.71	1.8	1.89	V	Any voltage between 2.5V and 3.3V is supported with 1 decim	
		2.25	2.5	2.75	V	point resolution.	
		2.52	2.8	3.08	V		
		2.97	3.3	3.63	V		
Current Consumption	ldd	-	6.7	7.5	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V	
·		_	6.1	6.7	mA	No load condition, f = 20 MHz, Vdd = 1.8 V	
Standby Current	I_std	-	2.4	4.3	μA	ST = GND, Vdd = 3.3 V, Output is Weakly Pulled Down	
-	_	-	1.2	2.2	μA	ST = GND, Vdd = 2.5 or 2.8 V, Output is Weakly Pulled Down	
		-	0.4	0.8	μA	ST = GND, Vdd = 1.8 V, Output is Weakly Pulled Down	
Duty Cycle	DC	45	50	55	%	All Vdds. f <= 75 MHz	
		40	50	60	%	All Vdds. f > 75 MHz	
Rise/Fall Time	Tr, Tf	-	1	2	ns	15pF load, 20% - 80% Vdd=2.5V, 2.8V or 3.3V	
		-	1.3	2.5	ns	15pF load, 20% - 80% Vdd=1.8V	
		-	1.9	2.6	ns	30pF load, 20% - 80% Vdd=2.5V, 2.8V or 3.3V	
		-	2.3	3.3	ns	30pF load, 20% - 80% Vdd=1.8V	
		-	2.9	3.9	ns	45pF load, 20% - 80% Vdd=2.5V, 2.8V or 3.3V	
		_	3.4	4.6	ns	45pF load, 20% - 80% Vdd=1.8V	
Output Voltage High	VOH	90%	-	-	Vdd	IOH = -4 mA (Vdd = 3.3 V)	
Output Voltage Low	VOL	-	-	10%	Vdd	IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V)	
Input Voltage High	VIH	70%	-	_	Vdd	Pin 1, OE or ST	
Input Voltage Low	VIL	_	-	30%	Vdd	Pin 1, OE or ST	
Startup Time	T_start	-	-	10	ms	Measured from the time Vdd reaches its rated minimum value	
Resume Time	 T_resume	-	3.0	4	ms	Measured from the time ST pin crosses 50% threshold	
RMS Period Jitter		-	-	4.0	ps	f = 75 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V	
		_	-	6.5	ps	f = 75 MHz, Vdd = 1.8 V	
RMS Phase Jitter (random)	T_phj	-	0.6	-	ps	f = 75 MHz @ BW: 900 kHz to 7.5 MHz, VDD = 2.5 V to 3.3 V	
		-	0.8	-	ps	f = 75 MHz @ BW: 900 kHz to 7.5 MHz, VDD = 1.8 V	

Note:

1. All electrical specifications in the above table are measured with 15pF output load, unless stated otherwise in the Condition. For more information about SoftEdgeTM rise/fall time for driving higher output load or reducing EMI, download <u>http://www.sitime.com/support2/documents/AN10022-rise-and-fall-time-rev1.1.pdf</u>.

SiT8103 High Performance 1-110 MHz Oscillator



Pin Description Tables

Pin #1 Functionality				
OE				
H or Open ^[2] : specified frequency output				
L: output is high impedance				
ST				
H or Open: specified frequency output				
L: output is low level (weak pull down). Oscillation stops				

Pin Map				
Pin	Connection			
1	OE/ST			
2	GND			
3	CLK			
4	VDD			

Absolute Maximum Table

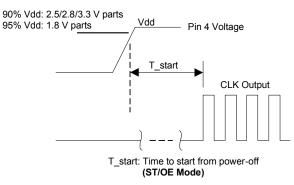
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

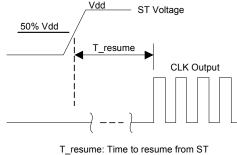
Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	-	6000	V
Theta JA (with copper plane on VDD and GND)	-	75	°C/W
Theta JC (with PCB traces of 0.010 inch to all pins)	-	24	°C/W
Soldering Temperature (follow standard Pb free soldering guidelines)	-	260	°C
Number of Program Writes	-	1	NA
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65 V)	1,000+	-	years

Environmental Compliance

Parameter	Condition/Test Method		
Mechanical Shock	MIL-STD-883F, Method 2002		
Mechanical Vibration	MIL-STD-883F, Method 2007		
Temperature Cycle	JESD22, Method A104		
Solderability	MIL-STD-883F, Method 2003		
Moisture Sensitivity Level	MSL1 @ 260°C		

Startup and Resume Timing Diagram





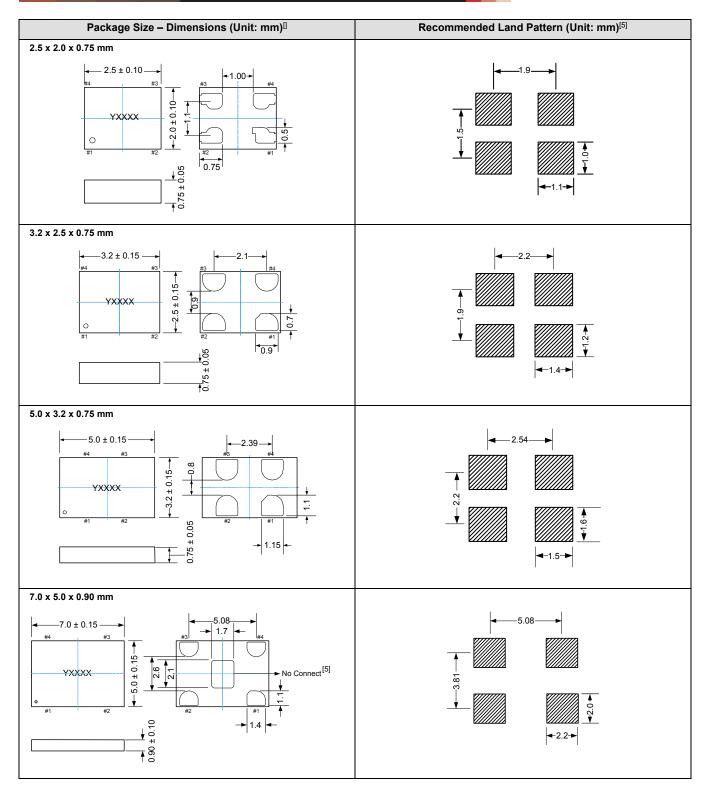
_resume: Time to resume from S (ST Mode Only)

Note:

2. In 1.8 V mode, a resistor of <100 k Ω between OE pin and VDD is required.

Dimensions and Land Patterns





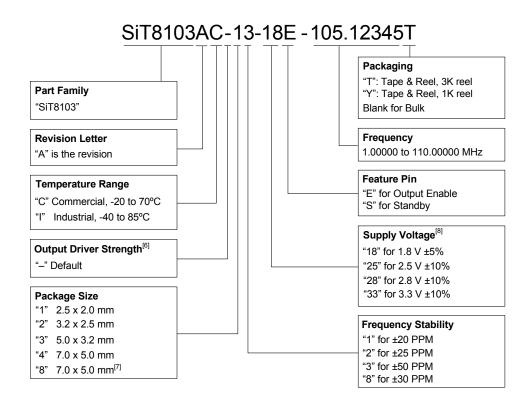
Notes:

- Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device
 A capacitor of value 0.1 μF between Vdd and GND is recommended.
 The 7050 package with part number designation "-8" has NO center pad.



Part No. Guide - How to Order

The Part No. Guide is for reference only. For real-time customization and exact part number, use the SiTime Part Number Generator.



Notes:

Contact SiTime for different drive strength options for driving loads with faster rise/fall time spec than those shown in the electrical table, or reducing EMI.
 Without Center Pad.

8. Supply voltage can be configured to any voltage up to 1 decimal place between 2.5V and 3.3V.

Frequency Stability vs. Temperature Range Options

Frequency	Temperature	Supply Voltage				
Stability (PPM)	Range	1.8 V	2.5 V	2.8 V	3.3 V	
±20	C (-20 to +70°C)	\checkmark	\checkmark	\checkmark	\checkmark	
	l (-40 to +85°C)	-	-	_	-	
±25	C (-20 to +70°C) I (-40 to +85°C)	\checkmark	\checkmark	\checkmark	\checkmark	
±30	C (-20 to +70°C) I (-40 to +85°C)	\checkmark	\checkmark	\checkmark	\checkmark	
±50	C (-20 to +70°C) I (-40 to +85°C)	\checkmark	\checkmark	\checkmark	\checkmark	

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