SiT8944B

1 – 110 MHz, -55 to 125°C, Endura™ Series Oscillator



Features

- Best acceleration sensitivity of 0.1 ppb/g
- Any frequencies between 1 MHz and 110 MHz accurate to 6 decimal places
- Extended temperature range (-55°C to 125°C)
- Excellent total frequency stability as low as ±20 ppm
- Supply voltage of 1.8V or 2.25V to 3.63V
- Low power consumption of 3.8 mA typical at 1.8V
- Standby mode for longer battery life
- LVCMOS/LVTTL compatible output
- AEC-Q100 qualified
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- Contact SiTime for up-screening and LAT programs

Applications

- Avionics systems
- Field communication systems
- Telemetry applications

Electrical Characteristics

Table 1. Electrical Characteristics^[1,2]

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Тур.	Max.	Unit	Condition
				Frequency	Range	
Output Frequency Range	f	1	_	110	MHz	Refer to Tables 13 to 15 for a list supported frequencies
			Frequ	uency Stabil	ity and Agi	ing
Frequency Stability	F_stab	-20	-	+20	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C,
		-25	-	+25	ppm	and variations over operating temperature, rated power supply voltage and load (15 pF ± 10%)
		-30	-	+30	ppm	
		-50	-	+50	ppm	
			Oper	ating Tempe	erature Ran	ge
Operating Temperature	T_use	-40	-	+85	°C	AEC-Q100 Grade 3
Range (ambient)		-40	_	+105	°C	AEC-Q100 Grade 2
		-40	-	+125	°C	AEC-Q100 Grade 1
		-55	-	+125	°C	Extended cold AEC-Q100 Grade1
			Ri	ugged Chara	acteristics	
Acceleration (g) sensitivity, Gamma Vector	F_g	-	_	0.1	ppb/g	Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
			Supply Vol	tage and Cu	rrent Cons	umption
Supply Voltage	Vdd	1.62	1.8	1.98	V	All voltages between 2.25V and 3.63V including 2.5V, 2.8V, 3.0V
		2.25	-	3.63	V	and 3.3V are supported
Current Consumption	ldd	-	4.0	4.8	mA	No load condition, f = 20 MHz, Vdd = 2.25V to 3.63V
		-	3.8	4.5	mA	No load condition, f = 20 MHz, Vdd = 1.8V
OE Disable Current	l_od	-	-	4.5	mA	Vdd = 2.5V to 3.3V, OE = Low, Output in high Z state
		-	-	4.3	mA	Vdd = 1.8V, OE = Low, Output in high Zstate
Standby Current	I_std	-	2.6	-	μА	Vdd = 2.8V to 3.3V, \overline{ST} = Low, Output is weakly pulled down
		-	1.4	-	μΑ	Vdd = 2.5V, ST = Low, Output is weakly pulled down
		-	0.6	-	μА	Vdd = 1.8V, ST = Low, Output is weakly pulled down



Table 1. Electrical Characteristics^[1,2] (continued)

Parameters	Symbol	Min.	Тур.	Max.	Unit	Condition		
			LVCM	OS Output C	Characteris	tics		
Duty Cycle	DC	45	-	55	%	All Vdd levels		
Rise/Fall Time	Tr, Tf	_	1.5	3	ns	Vdd = 2.25V - 3.63V, 20% - 80%		
		-	1.3	2.5	ns	Vdd = 1.8V, 20% - 80%		
Output High Voltage	VOH	90%	-	-	Vdd	IOH = -4 mA (Vdd = 3.0V or 3.3V) IOH = -3 mA (Vdd = 2.8V and Vdd = 2.5V) IOH = -2 mA (Vdd = 1.8V)		
Output Low Voltage	VOL	-	-	10%	Vdd	IOL = 4 mA (Vdd = 3.0V or 3.3V) IOL = 3 mA (Vdd = 2.8V and Vdd = 2.5V) IOL = 2 mA (Vdd = 1.8V)		
				Input Chara	cteristics			
Input High Voltage	VIH	70%	-	-	Vdd	Pin 1, OE or ST		
Input Low Voltage	VIL	1	-	30%	Vdd	Pin 1, OE or ST		
Input Pull-up Impedance	Z_in	-	100	-	kΩ	Pin 1, OE logic high or logic low, or \$\overline{ST}\$logic high		
		2	-	-	МΩ	Pin 1, ST logic low		
			Sta	rtup and Re	sume Timir	ng		
Startup Time	T_start	_	_	5.5	ms	Measured from the time Vdd reaches its rated minimum value		
Enable/Disable Time	T_oe	-	-	130	ns	f = 110 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles		
Resume Time	T_resume	-	_	5	ms	Measured from the time \overline{ST} pin crosses 50%threshold		
				Jitte	er			
RMS Period Jitter	T_jitt	_	1.6	2.5	ps	f = 75 MHz, 2.25V to 3.63V		
		-	1.9	3.0	ps	f = 75 MHz, 1.8V		
RMS Phase Jitter (random)	T_phj	_	0.5	_	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz		
		-	1.3	_	ps	f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz		

Notes:

- 1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.
- 2. The typical value of any parameter in the Electrical Characteristic table is specified for the nominal value of the highest voltage option for that parameter and at 25°C temperature.

Table 2. Pin Description

Pin	Symbol		Functionality
		Output Enable	H ^[3] : specified frequency output L: output is high impedance. Only output driver is disabled.
1	OE/ST/NC	Standby	H ^[3] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
	No Connect		Any voltage between 0 and Vdd or Open ^[3] : Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground ^[4]
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage ^[4]

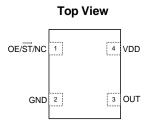


Figure 1. Pin Assignments

Notes:

- 3. In OE or \overline{ST} mode, a pull-up resistor of 10 k Ω or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
- 4. A capacitor of value 0.1 μF or higher between Vdd and GND is required.



Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	-	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	-	260	°C
Junction Temperature ^[5]	_	150	°C

Table 4. Thermal Consideration^[6]

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	142	273	30
5032	97	199	24
3225	109	212	27
2520	117	222	26
2016	152	252	36

Table 5. Maximum Operating Junction Temperature^[7]

Max Operating Temperature(ambient)	Maximum Operating Junction Temperature		
85°C	95°C		
105°C	115°C		
125°C	135°C		

Note:
7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
	,
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

^{5.} Exceeding this temperature for extended period of time may damage the device.

^{6.} Refer to JESD51 for θ JA and θ JC definitions, and reference layout used to determine the θ JA and θ JC values in the above table.



Test Circuit and Waveform

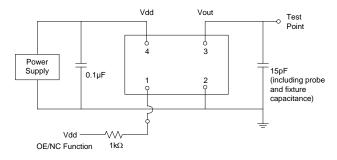
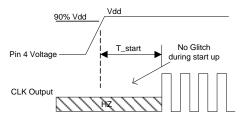


Figure 2. Test Circuit^[8]

Note:

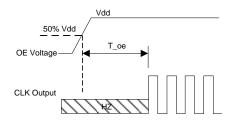
Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams



T_start: Time to start from power-off

Figure 4. Startup Timing (OE/ ST Mode)[9]



T_oe: Time to re-enable the clock output

Figure 6. OE Enable Timing (OE Mode Only)

Note:

9. SiT8944 has "no runt" pulses and "no glitch" output during startup or resume.

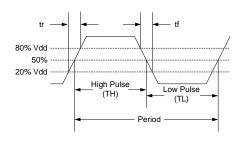
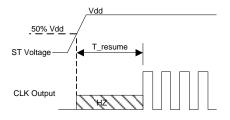
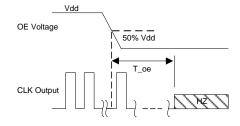


Figure 3. Waveform^[8]



T_resume: Time to resume from ST

Figure 5. Standby Resume Timing (ST Mode Only)

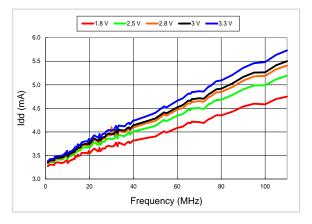


T_oe: Time to put the output in High Z mode

Figure 7. OE Disable Timing (OE Mode Only)



Performance Plots[10]



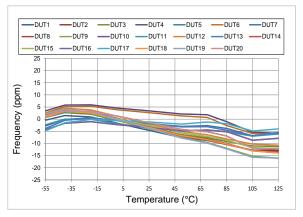
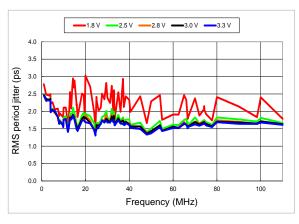


Figure 8. Idd vs Frequency

Figure 9. Frequency vs Temperature



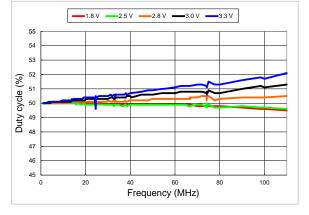
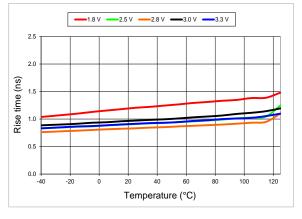


Figure 10. RMS Period Jitter vs Frequency

Figure 11. Duty Cycle vs Frequency



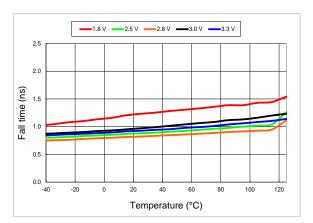
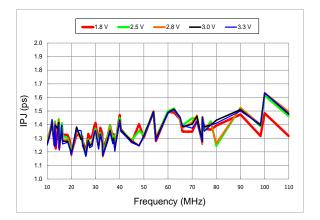


Figure 12. 20%-80% Rise Time vs Temperature

Figure 13. 20%-80% Fall Time vs Temperature



Performance Plots[10]



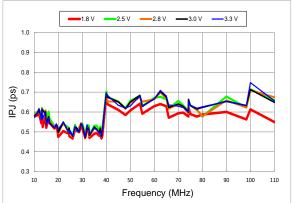


Figure 14. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency^[11]

Figure 15. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency[11]

Notes:

- 10. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
 11. Phase noise plots are measured with Agilent E5052B signal source analyzer. Integration range is up to 5 MHz for carrier frequencies up to 40 MHz.



Programmable Drive Strength

The SiT8944 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section.

EMI Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

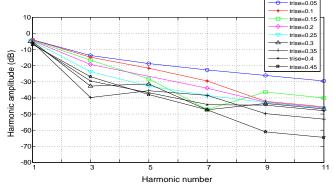


Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V SiT8944 device with default drive strength setting, the typical rise/fall time is 1 ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.83 ns by then increasing the drive strength setting on the SiT8944.

The SiT8944 can support up to 60 pF in maximum capacitive loads with drive strength settings. Refer to the Rise/Tall Time Tables (Table 7 to Table 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

SiT8944 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

- 1. Select the table that matches the SiT8944 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
- 2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
- Under the capacitive load column, select the desired rise/fall times.
- **4.** The left-most column represents the part number code for the corresponding drive strength.
- Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature can be calculated as follows:

Max Frequency =
$$\frac{1}{5 \text{ x Trf}_20/80}$$

where $Trf_{20/80}$ is the typical value for 20%-80% rise/fall time.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 1.8V (Table 7)
- Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns
 (rise/fall time part number code = E)

Part number for the above example:

SiT8944BME12-18EA66.666660



Drive strength code is inserted here. Default setting is "-"



Rise/Fall Time (20% to 80%) vs CLOAD Tables

Table 7. Vdd = 1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)								
Drive Strength \C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF			
L	6.16	11.61	22.00	31.27	39.91			
Α	3.19	6.35	11.00	16.01	21.52			
R	2.11	4.31	7.65	10.77	14.47			
В	1.65	3.23	5.79	8.18	11.08			
Т	0.93	1.91	3.32	4.66	6.48			
E	0.78	1.66	2.94	4.09	5.74			
U	0.70	1.48	2.64	3.68	5.09			
F or "-": default	0.65	1.30	2.40	3.35	4.56			

Table 9. Vdd = 2.8V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)							
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF		
L	3.77	7.54	12.28	19.57	25.27		
Α	1.94	3.90	7.03	10.24	13.34		
R	1.29	2.57	4.72	7.01	9.06		
В	0.97	2.00	3.54	5.43	6.93		
Т	0.55	1.12	2.08	3.22	4.08		
E or "-": default	0.44	1.00	1.83	2.82	3.67		
U	0.34	0.88	1.64	2.52	3.30		
F	0.29	0.81	1.48	2.29	2.99		

Table 11. Vdd = 3.3V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)							
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF		
L	3.39	6.88	11.63	17.56	23.59		
А	1.74	3.50	6.38	8.98	12.19		
R	1.16	2.33	4.29	6.04	8.34		
В	0.81	1.82	3.22	4.52	6.33		
T or "-": default	0.46	1.00	1.86	2.60	3.84		
E	0.33	0.87	1.64	2.30	3.35		
U	0.28	0.79	1.46	2.05	2.93		
F	0.25	0.72	1.31	1.83	2.61		

Table 8. Vdd = 2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)							
Drive Strength \C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF		
L	4.13	8.25	12.82	21.45	27.79		
Α	2.11	4.27	7.64	11.20	14.49		
R	1.45	2.81	5.16	7.65	9.88		
В	1.09	2.20	3.88	5.86	7.57		
T	0.62	1.28	2.27	3.51	4.45		
E or "-": default	0.54	1.00	2.01	3.10	4.01		
U	0.43	0.96	1.81	2.79	3.65		
F	0.34	0.88	1.64	2.54	3.32		

Table 10. Vdd = 3.0V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)							
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF		
L	3.60	7.21	11.97	18.74	24.30		
Α	1.84	3.71	6.72	9.86	12.68		
R	1.22	2.46	4.54	6.76	8.62		
В	0.89	1.92	3.39	5.20	6.64		
T or "-": default	0.51	1.00	1.97	3.07	3.90		
E	0.38	0.92	1.72	2.71	3.51		
U	0.30	0.83	1.55	2.40	3.13		
F	0.27	0.76	1.39	2.16	2.85		



Pin 1 Configuration Options (OE, \overline{ST} , or NC)

Pin 1 of the SiT8944 can be factory-programmed to support three modes: Output enable (OE), standby ST or No Connect (NC). These modes can also be programmed with the Time Machine II using Field Programmable Oscillators.

Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in $<1\mu$ s.

Standby (ST) Mode

In the \overline{ST} mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few μA . When \overline{ST} is pulled High, the device goes through the "resume" process, which can take up to 5 ms.

No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and output the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE, \overline{ST} , or NC mode.

Table 12. OE vs. ST vs. NC

	OE	ST	NC
Active current 20 MHz (max, 1.8V)	4.5 mA	4.5 mA	4.5 mA
OE disable current (max. 1.8V)	4.3 mA	N/A	N/A
Standby current (typical 1.8V)	N/A	0.6 uA	N/A
OE enable time at 110 MHz (max)	130 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/standby mode	High Z	Weak pull-down	N/A

Output on Startup and OE Enable

The SiT8944 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or when the output driver is enabled.

In addition, the SiT8944 supports "no runt" pulses and "no glitch" output during startup or when the device output driver is enabled as shown in the waveform captures in Figure 17 and Figure 18.



Figure 17. Startup Waveform vs. Vdd

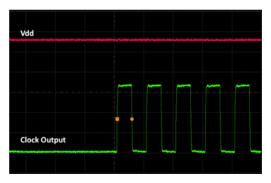
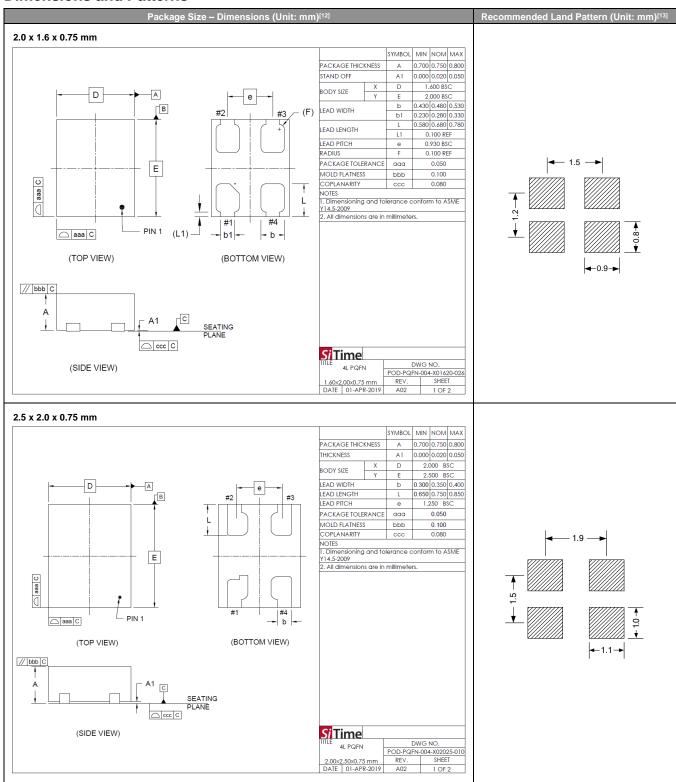


Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)

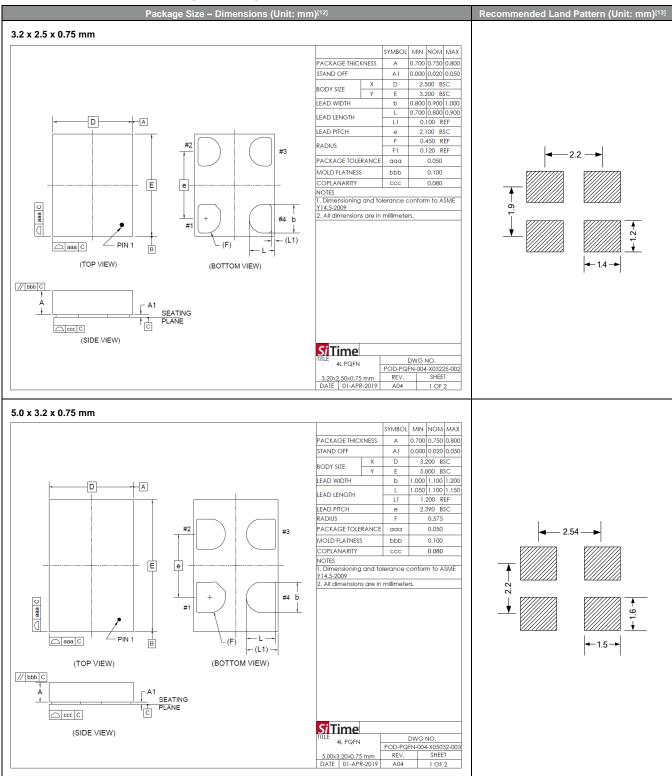


Dimensions and Patterns



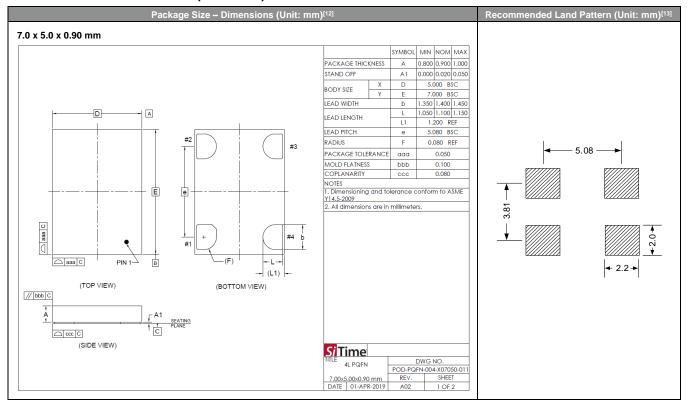


Dimensions and Patterns (continued)





Dimensions and Patterns (continued)



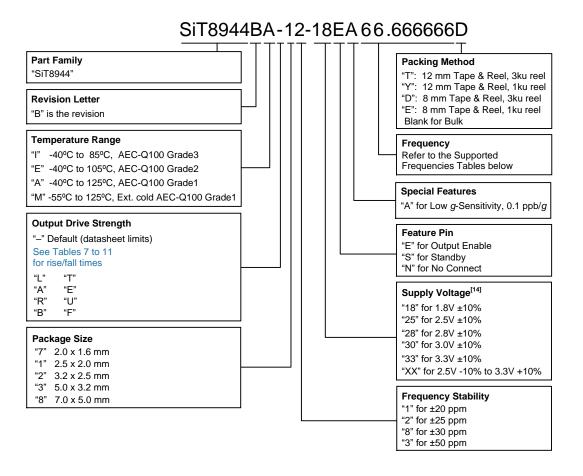
Notes:

- 12. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- 13. A capacitor of value 0.1 µF or higher between Vdd and GND is required.



Ordering Information

The following part number guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.



Note:

^{14.} The voltage portion of the SiT8944 part number consists of two characters that denote the specific supply voltage of the device. The SiT8944 supports either 1.8V ±10% or any voltage between 2.25V and 3.62V. In the 1.8V mode, one can simply insert 18 in the part number. In the 2.5V to 3.3V mode, two digits such as 18, 25 or 33 can be used in the part number to reflect the desired voltage. Alternatively, "XX" can be used to indicate the entire operating voltage range from 2.25V to 3.63V.



Table 13. Supported Frequencies (-40°C to +85°C)^[15]

Frequency Range		
Min.	Max.	
1.000000 MHz	110.000000 MHz	

Table 14. Supported Frequencies (-40°C to +105°C or -40°C to +125°C)^[15, 16]

Frequency Range			
Min.	Max.		
1.000000 MHz	61.222999 MHz		
61.974001 MHz	69.795999 MHz		
70.485001 MHz	79.062999 MHz		
79.162001 MHz	81.427999 MHz		
82.232001 MHz	91.833999 MHz		
92.155001 MHz	94.248999 MHz		
94.430001 MHz	94.874999 MHz		
94.994001 MHz	97.713999 MHz		
98.679001 MHz	110.000000 MHz		

Table 15. Supported Frequencies (-55°C to +125°C)^[15, 16]

Frequency Range			
Min.	Max.		
1.000000 MHz	61.222999 MHz		
61.974001 MHz	69.239999 MHz		
70.827001 MHz	78.714999 MHz		
79.561001 MHz	80.159999 MHz		
80.174001 MHz	80.779999 MHz		
82.632001 MHz	91.833999 MHz		
95.474001 MHz	96.191999 MHz		
96.209001 MHz	96.935999 MHz		
99.158001 MHz	110.000000 MHz		

- Notes:
 15. Any frequency within the min and max values in the above tables are supported with 6 decimal places of accuracy.
 16. Please contact SiTime for frequencies that are not listed in the tables above.

Table 16. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	16 mm T&R (3ku)	16 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	8 mm T&R (3ku)	8 mm T&R (1ku)
2.0 x 1.6	-	ı	-	-	D	E
2.5 x 2.0	-	ı	-	-	D	E
3.2 x 2.5	-	-	-	-	D	Е
5.0 x 3.2	-	-	Т	Υ	-	-
7.0 x 5.0	Т	Y	_	_		_



Table 17. Revision History

Revision	Release Date	Change Summary
0.5	07/22/2019	First release
1.00	07/24/2020	Final release

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone**: +1-408-328-4400 | **Fax**: +1-408-328-4439

© SiTime Corporation 2020. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. Products sold by SiTime are not suitable or intended to be used in a life support application or component, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY

BUYER AGREES NOT TO USE SITIME'S PRODUCTS FOR ANY APPLICATION OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Standard Clock Oscillators category:

Click to view products by SiTime manufacturer:

Other Similar products are found below:

601252 F335-25 F535L-33.333 F535L-50 ASV-20.000MHZ-LR-T ECS-2018-160-BN-TR MXO45HS-2C-66.6666MHZ SiT1602BI-22-33E-50.000000E SiT8209AI-32-33E-125.000000 SIT8918AA-11-33S-50.000000G SM4420TEV-40.0M-T1K F335-24 F335-40 F535L-10 F535L-12 F535L-16 F535L-24 F535L-27 F535L-48 PE7744DW-100.0M CSX-750FCC14745600T ASF1-3.686MHZ-N-K-S XO57CTECNA3M6864 ECS-2100A-147.4 601251 EP16E7E2H26.000MTR SIT8918AA-11-33S-16.000000G XO3003 9120AC-2D2-33E212.500000 9102AI-243N25E100.00000 8208AC-82-18E-25.00000 ASDK2-32.768KHZ-LR-T3 8008AI-72-XXE-24.545454E 8004AC-13-33E-133.33000X AS-4.9152-16-SMD-TR ASFL1-48.000MHZ-LC-T SIT8920AM-31-33E-25.0000 DSC1028DI2-019.2000 9121AC-2C3-25E100.00000 9102AI-233N33E100.00000X 9102AI-233N25E200.00000 9102AI-233N25E200.00000 9102AI-233S-40.00000Y 1602BI-13-33S-19.200000E