

Features

- 31 standard frequencies from 25 MHz to 212.5 MHz
- LVPECL and LVDS output signaling types
- 0.6 ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ± 10 ppm
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 3.2 x 2.5, 5.0 x 3.2 and 7.0 x 5.0 mm x mm
- For any other frequencies between 1 to 625 MHz, refer to [SiT9121](#) and [SiT9122](#) datasheet

Applications

- 10GB Ethernet, SONET, SATA, SAS, Fibre Channel, PCI-Express
- Telecom, networking, instrumentation, storage, server



Electrical Characteristics

Table 1. Electrical Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---------------------------------|----------------------|------|----------------------|-----------------|--|
| LVPECL and LVDS, Common Electrical Characteristics | | | | | | |
| Supply Voltage | V _{dd} | 2.97 | 3.3 | 3.63 | V | |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 2.25 | – | 3.63 | V | Termination schemes in Figures 1 and 2 - XX ordering code |
| Output Frequency Range | f | 25 | – | 212.5 | MHz | See list of standard frequencies |
| Frequency Stability | F _{stab} | -10 | – | +10 | ppm | Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations |
| | | -20 | – | +20 | ppm | |
| | | -25 | – | +25 | ppm | |
| | | -50 | – | +50 | ppm | |
| First Year Aging | F _{aging1} | -2 | – | +2 | ppm | 25°C |
| 10-year Aging | F _{aging10} | -5 | – | +5 | ppm | 25°C |
| Operating Temperature Range | T _{use} | -40 | – | +85 | °C | Industrial |
| | | -20 | – | +70 | °C | Extended Commercial |
| Input Voltage High | V _{IH} | 70% | – | – | V _{dd} | Pin 1, OE or \overline{ST} |
| Input Voltage Low | V _{IL} | – | – | 30% | V _{dd} | Pin 1, OE or \overline{ST} |
| Input Pull-up Impedance | Z _{in} | – | 100 | 250 | k Ω | Pin 1, OE logic high or logic low, or \overline{ST} logic high |
| | | 2 | – | – | M Ω | Pin 1, \overline{ST} logic low |
| Start-up Time | T _{start} | – | 6 | 10 | ms | Measured from the time V _{dd} reaches its rated minimum value. |
| Resume Time | T _{resume} | – | 6 | 10 | ms | In Standby mode, measured from the time \overline{ST} pin crosses 50% threshold. |
| Duty Cycle | DC | 45 | – | 55 | % | Contact SiTime for tighter duty cycle |
| LVPECL, DC and AC Characteristics | | | | | | |
| Current Consumption | I _{dd} | – | 61 | 69 | mA | Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V |
| OE Disable Supply Current | I _{OE} | – | – | 35 | mA | OE = Low |
| Output Disable Leakage Current | I _{leak} | – | – | 1 | μ A | OE = Low |
| Standby Current | I _{std} | – | – | 100 | μ A | \overline{ST} = Low, for all V _{dds} |
| Maximum Output Current | I _{driver} | – | – | 30 | mA | Maximum average current drawn from OUT+ or OUT- |
| Output High Voltage | V _{OH} | V _{dd} -1.1 | – | V _{dd} -0.7 | V | See Figure 1(a) |
| Output Low Voltage | V _{OL} | V _{dd} -1.9 | – | V _{dd} -1.5 | V | See Figure 1(a) |
| Output Differential Voltage Swing | V _{Swing} | 1.2 | 1.6 | 2.0 | V | See Figure 1(b) |
| Rise/Fall Time | T _r , T _f | – | 300 | 500 | ps | 20% to 80%, see Figure 1(a) |
| OE Enable/Disable Time | T _{oe} | – | – | 115 | ns | f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period |
| RMS Period Jitter | T _{jitt} | – | 1.2 | 1.7 | ps | f = 100 MHz, V _{DD} = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 156.25 MHz, V _{DD} = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 212.5 MHz, V _{DD} = 3.3V or 2.5V |
| RMS Phase Jitter (random) | T _{phj} | – | 0.6 | 0.85 | ps | f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dds} |

Table 1. Electrical Characteristics (continued)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|---------------------------------|-------|------|-------|------|--|
| LVDS, DC and AC Characteristics | | | | | | |
| Current Consumption | I _{dd} | – | 47 | 55 | mA | Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V |
| OE Disable Supply Current | I _{OE} | – | – | 35 | mA | OE = Low |
| Differential Output Voltage | V _{OD} | 250 | 350 | 450 | mV | See Figure 2 |
| Output Disable Leakage Current | I _{leak} | – | – | 1 | μA | OE = Low |
| Standby Current | I _{std} | – | – | 100 | μA | \overline{ST} = Low, for all V _{dds} |
| VOD Magnitude Change | ΔV _{OD} | – | – | 50 | mV | See Figure 2 |
| Offset Voltage | V _{OS} | 1.125 | 1.2 | 1.375 | V | See Figure 2 |
| VOS Magnitude Change | ΔV _{OS} | – | – | 50 | mV | See Figure 2 |
| Rise/Fall Time | T _r , T _f | – | 495 | 600 | ps | 20% to 80%, see Figure 2 |
| OE Enable/Disable Time | T _{oe} | – | – | 115 | ns | f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period |
| RMS Period Jitter | T _{jitt} | – | 1.2 | 1.7 | ps | f = 100 MHz, VDD = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 156.25 MHz, VDD = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 212.5 MHz, VDD = 3.3V or 2.5V |
| RMS Phase Jitter (random) | T _{phj} | – | 0.6 | 0.85 | ps | f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dds} |

Table 2. Pin Description

| Pin | Map | Functionality |
|-----|-----------------|--|
| 1 | NC | NA No Connect; Leave it floating or connect to GND for better heat dissipation |
| | OE | Input H or Open: specified frequency output L: output is high impedance |
| | \overline{ST} | Input H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I _{std} . |
| 2 | NC | NA No Connect; Leave it floating or connect to GND for better heat dissipation |
| 3 | GND | Power VDD Power Supply Ground |
| 4 | OUT+ | Output Oscillator output |
| 5 | OUT- | Output Complementary oscillator output |
| 6 | VDD | Power Power supply voltage |

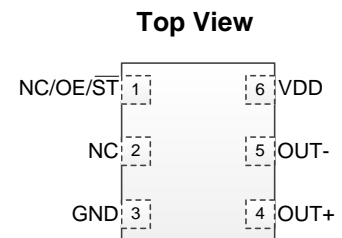


Figure 1. Pin Assignments

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|--|------|------|------|
| Storage Temperature | -65 | 150 | °C |
| VDD | -0.5 | 4 | V |
| Electrostatic Discharge (HBM) | – | 2000 | V |
| Soldering Temperature (follow standard Pb free soldering guidelines) | – | 260 | °C |

Table 4. Thermal Consideration^[1]

| Package | θ_{JA} , 4 Layer Board (°C/W) | θ_{JC} , Bottom (°C/W) |
|-------------|--------------------------------------|-------------------------------|
| 7050, 6-pin | 142 | 27 |
| 5032, 6-pin | 97 | 20 |
| 3225, 6-pin | 109 | 20 |

Note:

1. Refer to JESD51-7 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 5. Maximum Operating Junction Temperature^[2]

| Max Operating Temperature (ambient) | Maximum Operating Junction Temperature |
|-------------------------------------|--|
| 70°C | 90°C |
| 85°C | 105°C |

Note:

2. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

| Parameter | Condition/Test Method |
|----------------------------|---------------------------|
| Mechanical Shock | MIL-STD-883F, Method 2002 |
| Mechanical Vibration | MIL-STD-883F, Method 2007 |
| Temperature Cycle | JESD22, Method A104 |
| Solderability | MIL-STD-883F, Method 2003 |
| Moisture Sensitivity Level | MSL1 @ 260°C |

Waveform Diagrams

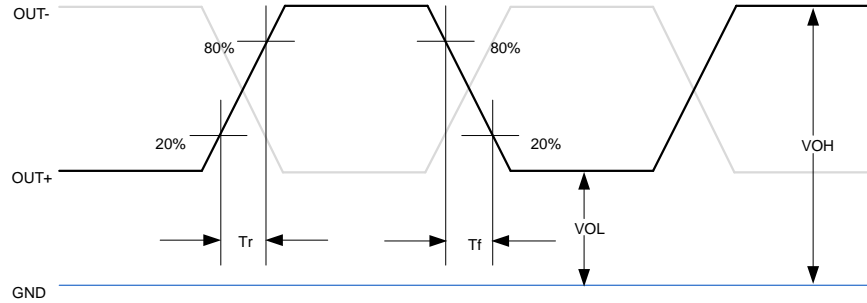


Figure 1(a). LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

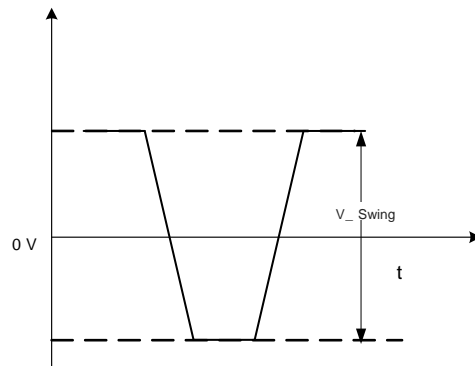


Figure 1(b). LVPECL Voltage Levels Across Differential Pair

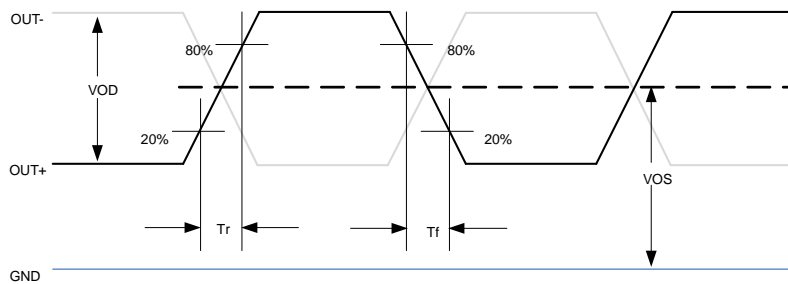


Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL

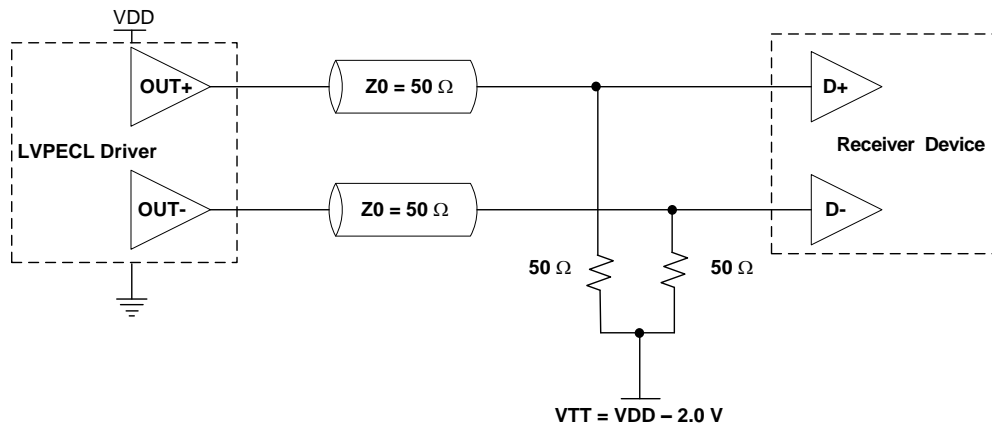


Figure 3. LVPECL Typical Termination

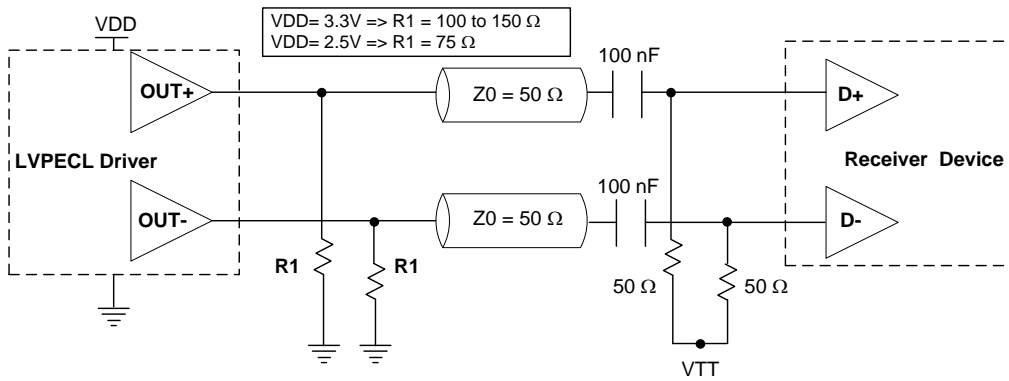


Figure 4. LVPECL AC Coupled Termination

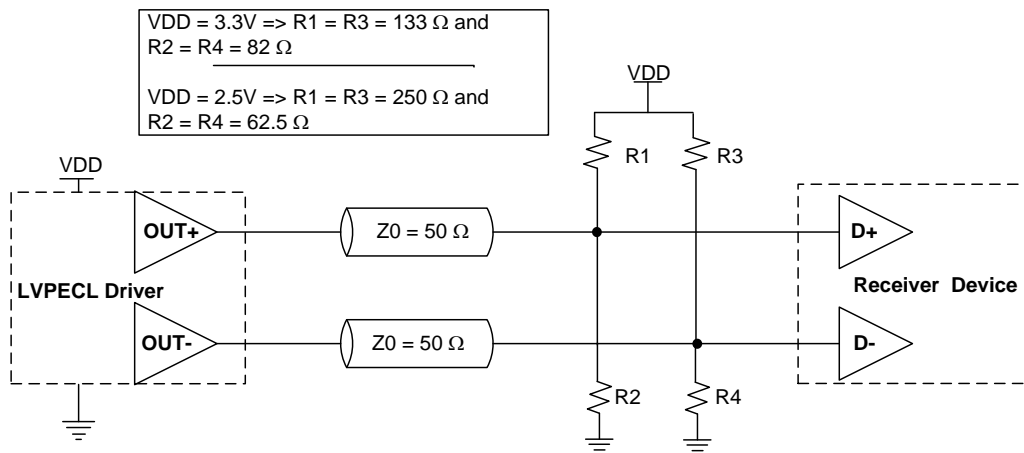


Figure 5. LVPECL with Thevenin Typical Termination

Termination Diagrams (continued)

LVDS

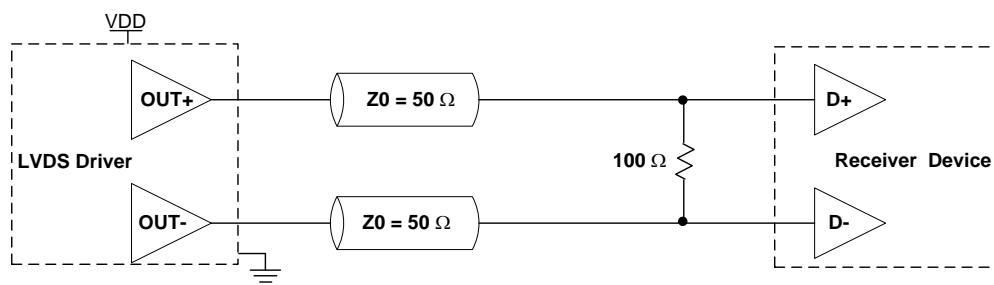


Figure 6. LVDS Single Termination (Load Terminated)

Dimensions and Patterns

| Package Size – Dimensions (Unit: mm) ⁽³⁾ | Recommended Land Pattern (Unit: mm) ⁽⁴⁾ |
|---|--|
| <p>3.2 x 2.5 x 0.75 mm</p> | |
| <p>5.0 x 3.2 x 0.75 mm</p> | |
| <p>7.0 x 5.0 x 0.90 mm</p> | |

Notes:

3. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
4. A capacitor of value 0.1 μ F between Vdd and GND is recommended.

Ordering Information

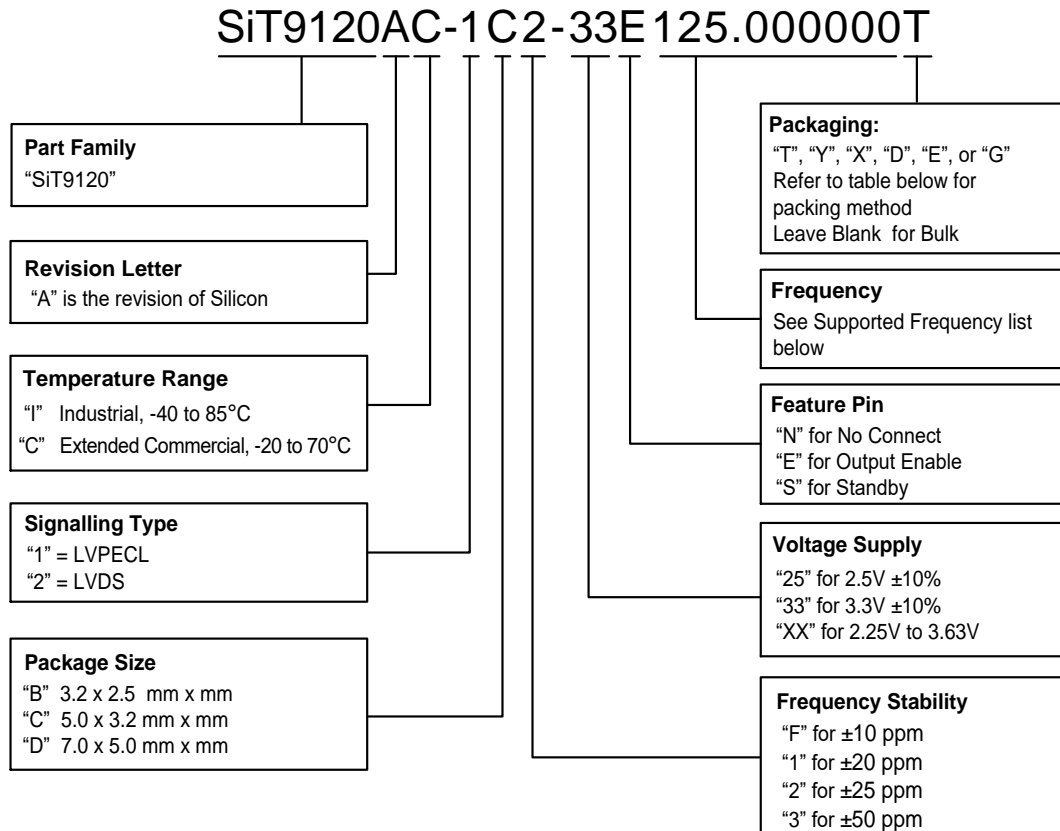


Table 7. List of Supported Frequencies

| | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 25.000000 MHz | 50.000000 MHz | 74.175824 MHz | 74.250000 MHz | 75.000000 MHz | 98.304000 MHz | 100.000000 MHz | 106.250000 MHz |
| 125.000000 MHz | 133.000000 MHz | 133.300000 MHz | 133.330000 MHz | 133.333000 MHz | 133.333300 MHz | 133.333330 MHz | 133.333333 MHz |
| 148.351648 MHz | 148.500000 MHz | 150.000000 MHz | 155.520000 MHz | 156.250000 MHz | 161.132800 MHz | 166.000000 MHz | 166.600000 MHz |
| 166.660000 MHz | 166.666000 MHz | 166.666600 MHz | 166.666660 MHz | 166.666666 MHz | 200.000000 MHz | 212.500000 MHz | |

Table 8. Ordering Codes for Supported Tape & Reel Packing Method

| Device Size | 8 mm T&R (3ku) | 8 mm T&R (1ku) | 8 mm T&R (250u) | 12 mm T&R (3ku) | 12 mm T&R (1ku) | 12 mm T&R (250u) | 16 mm T&R (3ku) | 16 mm T&R (1ku) | 16 mm T&R (250u) |
|--------------|----------------|----------------|-----------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|
| 7.0 x 5.0 mm | - | - | - | - | - | - | T | Y | X |
| 5.0 x 3.2 mm | - | - | - | T | Y | X | - | - | - |
| 3.2 x 2.5 mm | D | E | G | T | Y | X | - | - | - |

Table 9. Revision History

| Revisions | Release Date | Change Summary |
|-----------|--------------|--|
| 1.01 | 02/20/2013 | Original |
| 1.02 | 11/23/2013 | Added input specifications, LVPECL/LVDS waveforms, packaging T&R options |
| 1.03 | 02/06/2014 | Added 8mm T&R option |
| 1.04 | 03/03/2014 | Added ± 10 ppm |
| 1.05 | 07/23/2014 | Include Thermal Consideration Table |
| 1.06 | 10/03/2014 | Modified Thermal Consideration values |
| 1.07 | 01/09/2017 | Included Maximum Operating Junction Temperature Table Added Thermal Consideration Notes to Table Updated logo and company address, other page layout changes |
| 1.08 | 06/25/2019 | Added No Connect feature to Pin 1 |

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Supplemental Information

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Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

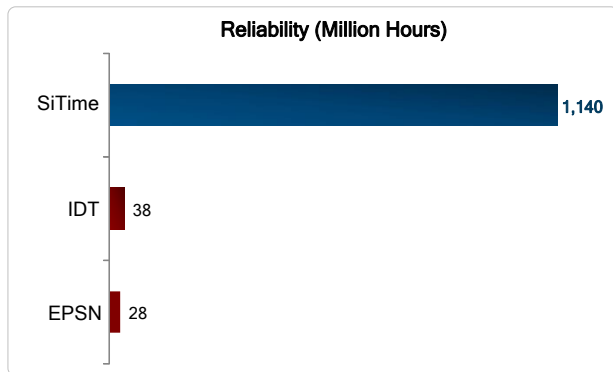


Figure 1. Reliability Comparison^[1]

Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

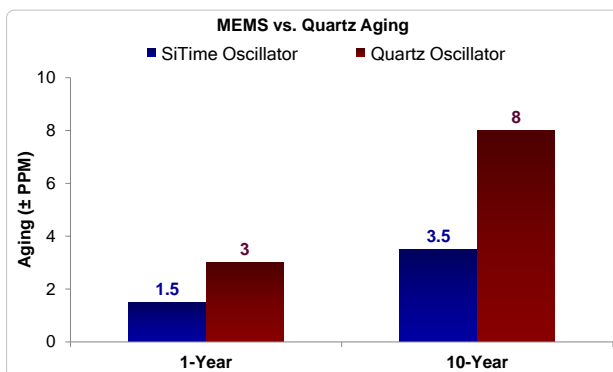


Figure 2. Aging Comparison^[2]

Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

Why is SiTime Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

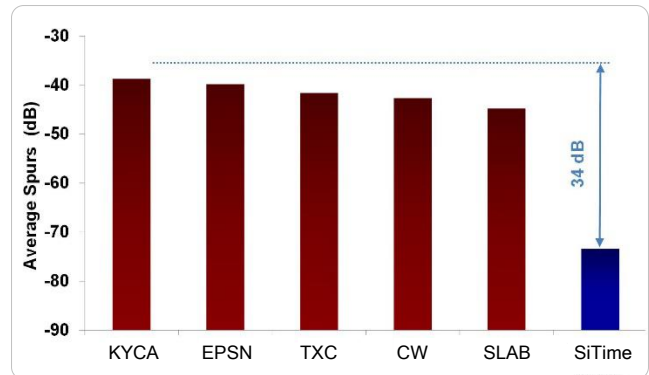


Figure 3. Electro Magnetic Susceptibility (EMS)^[3]

Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

Why is SiTime Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- MEMS resonator is paired with advanced analog CMOS IC

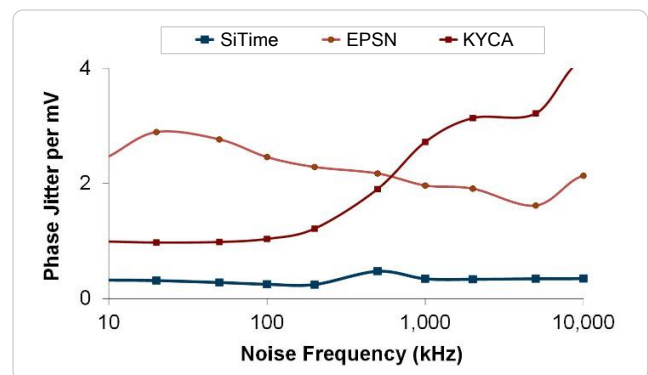


Figure 4. Power Supply Noise Rejection^[4]

Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

Why is SiTime Best in Class:

- The moving mass of SiTime’s MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

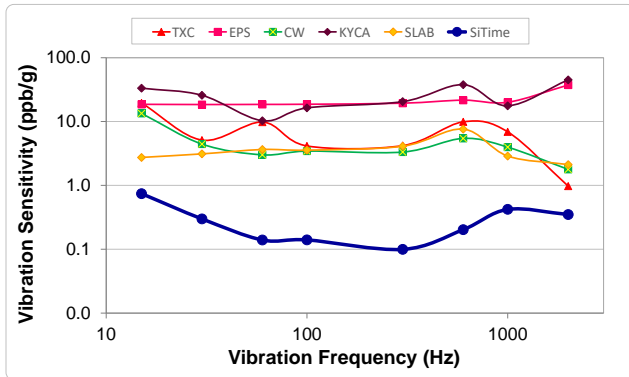


Figure 5. Vibration Robustness^[5]

Figure labels:

- TXC = TXC
- Epson = EPSN
- Connor Winfield = CW
- Kyocera = KYCA
- SiLabs = SLAB
- SiTime = EpiSeal MEMS

Best Shock Robustness

SiTime’s oscillators can withstand at least 50,000 g shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

Why is SiTime Best in Class:

- The moving mass of SiTime’s MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

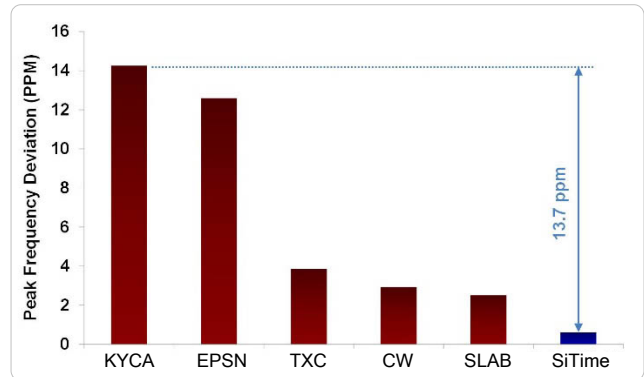


Figure 6. Shock Robustness^[6]

Notes:

1. Data source: Reliability documents of named companies.
2. Data source: SiTime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
 - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
 - Field strength: 3V/m
 - Radiated signal modulation: AM 1 kHz at 80% depth
 - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
 - Antenna polarization: Vertical
 - DUT position: Center aligned to antenna

Devices used in this test:

| Label | Manufacturer | Part Number | Technology |
|--------------|-----------------|-----------------------------|--|
| EpiSeal MEMS | SiTime | SiT9120AC-1D2-33E156.250000 | MEMS + PLL |
| EPSN | Epson | EG-2102CA156.2500M-PHPAL3 | Quartz, SAW |
| TXC | TXC | BB-156.250MBE-T | Quartz, 3 rd Overtone |
| CW | Conner Winfield | P123-156.25M | Quartz, 3 rd Overtone |
| KYCA | AVX Kyocera | KC7050T156.250P30E00 | Quartz, SAW |
| SLAB | SiLab | 590AB-BDG | Quartz, 3 rd Overtone + PLL |

4. 50 mV pk-pk Sinusoidal voltage.

Devices used in this test:

| Label | Manufacturer | Part Number | Technology |
|--------------|--------------|----------------------------|------------|
| EpiSeal MEMS | SiTime | SiT8208AI-33-33E-25.000000 | MEMS + PLL |
| NDK | NDK | NZ2523SB-25.6M | Quartz |
| KYCA | AVX Kyocera | KC2016B25M0C1GE00 | Quartz |
| EPSN | Epson | SG-310SCF-25M0-MB3 | Quartz |

5. Devices used in this test:
same as EMS test stated in Note 3.
6. Test conditions for shock test:
 - MIL-STD-883F Method 2002
 - Condition A: half sine wave shock pulse, 500-g, 1ms
 - Continuous frequency measurement in 100 μ s gate time for 10 seconds

Devices used in this test:

same as EMS test stated in Note 3.

7. Additional data, including setup and detailed results, is available upon request to qualified customer. Please contact productsupport@sitime.com.

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[33E212.500000](#) [9102AI-243N25E100.000000](#) [8208AC-82-18E-25.000000](#) [8008AI-72-XXE-24.545454E](#) [8004AC-13-33E-133.330000X](#) [AS-](#)
[4.9152-16-SMD-TR](#) [ASFL1-48.000MHZ-LC-T](#) [632L3I004M000000](#) [SIT8920AM-31-33E-25.000000](#) [DSC1028DI2-019.2000](#) [9121AC-2C3-](#)
[25E100.000000](#) [9102AI-233N33E100.000000X](#) [9102AI-233N25E200.000000](#) [9102AI-232H25S125.000000](#) [9102AI-133N25E200.000000](#) [9102AC-](#)
[283N25E200.000000](#) [9001AC-33-33E1-30.000000](#) [8103AC-13-33E-12.000000X](#) [3921AI-2CF-33NZ125.000000](#) [5730-1SF](#) [XUN736000.032768I](#)
[ASV-25.000MHZ-ECS-50-T](#) [EC3925ETTTS-100.000M TR](#) [SIT1602BC-83-33E-10.000000Y](#) [8003AI-12-33S-40.000000Y](#) [1602BI-13-33S-](#)
[19.200000E](#) [8208AI-2F-18E-25.000000X](#) [8103AI-83-33E-33.000000X](#) [8208AI-8F-33E-66.666666X](#)